

# **bq24292i I<sup>2</sup>C 控制型 4.5A 单节电池 USB/适配器充电器** **(具有窄 VDC 电源路径管理和 USB OTG)**

## 1 特性

- 高效的 4.5A 开关模式充电器
  - 电流为 2A 时，充电效率 92%，4A 时，充电效率 90%
  - 通过电池路径阻抗补偿缩短充电时间
- 借助 12mΩ 电池放电金属氧化物半导体场效应晶体管 (MOSFET) 的最高电池放电效率，放电电流高达 9A
- 单输入 USB 兼容/适配器充电器
  - 支持与 USB 电池充电器技术规格 1.2 兼容的 USB 检测
  - 输入电压和电流限制支持 USB2.0 和 USB3.0
  - 输入电流限值
    - : 100mA, 150mA, 500mA, 900mA, 1.2A, 1.5A, 2A 和 3A
- 3.9V-17V 输入工作电压范围
  - 支持含输入电压动态电源管理 (DPM) 调节的所有类型适配器
- 支持 USB On-The-Go 标准和 5V/1.3A 同步升压转换器运行
  - 5V/1A 时升压效率为 93%
  - 快速 OTG 启动 (典型值 22ms)
  - 断续模式过流保护
- 窄 VDC (NVDC) 电源路径管理
  - 与无电池或深度放电电池工作时可瞬时接通
  - 电池管理模式中的理想二极管运行
- 针对低尺寸电感器 1.5MHz 开关频率
- 具有或不具有主机管理的自主电池充电
  - 电池充电使能
  - 电池充电预调节
  - 充电终止和再充电
- 高精度 (0°C 至 125°C)
  - 充电电压调节范围为 ±0.5%
  - 充电电流调节范围为 ±7%
  - 输入电流调节范围为 ±7.5%
  - 升压模式下输出调节范围 ±2%
- 高集成
  - 电源路径管理
  - 同步开关 MOSFET
  - 集成电流感测

- 阴极负载二极管
- 内部环路补偿
- 安全性
  - 电池温度感测和充电安全定时器
  - 热调节和热关断
  - 输入系统过压保护
  - MOSFET 过流保护
- 针对 LED 或主机处理器的充电状态输出
- 低电池泄漏电流并支持关闭模式
- 4mm x 4mm VQFN-24 封装

## 2 应用范围

- 平板电脑
- 智能电话
- 便携式音频扬声器
- 便携式媒体播放器
- 互联网器件

## 3 说明

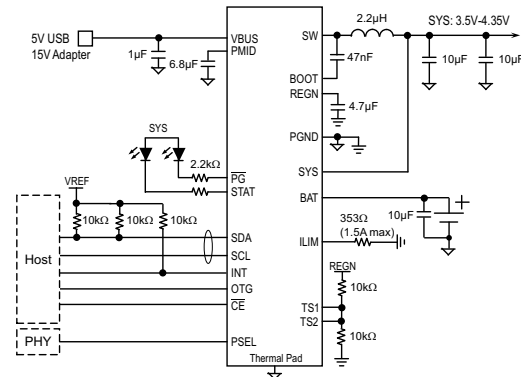
bq24292i 是一款高度集成的开关模式电池充电管理和系统电源路径管理器件，适用于各种智能手机、平板电脑和其他便携式设备中的单节锂离子和锂聚合物电池。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
bq24292i	VQFN (24)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

### bq24292i 与 PSEL、USB On-The-Go (OTG)，无热敏电阻连接



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## 4 修订历史记录

Changes from Revision A (April 2015) to Revision B	Page
• 已更改 VREF to $V_{\text{REGN}}$ in 图 15 .....	19
• 已更改 VREF to $V_{\text{REGN}}$ in 公式 2 .....	20
• 已添加 note to 图 36 .....	34
• 已添加 note to 图 37 .....	35
• 已更改 last paragraph in Output Capacitor section .....	36

Changes from Original (April 2013) to Revision A	Page
• 已添加 ESD 额定值表, 特性 描述 部分, 器件功能模式, 应用和实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分。 .....	1

## 5 说明（续）

它的低阻抗电源路径对开关模式运行效率进行了优化、减少了电池充电时间并延长了放电阶段的电池寿命。具有充电和系统设置的  $I^2C$  串行接口使得此器件成为一个真正地灵活解决方案。

此器件支持宽范围的输入源，其中包括标准 USB 主机端口，USB 充电端口和高功率 DC 适配器。为了设定缺省输入电流限值，该器件检测符合 USB 电池充电技术规格 1.2 的输入源，并从系统中（诸如 USB PHY 器件）的检测电路获取结果。该器件符合 USB 2.0 和 USB 3.0 电源规范，具有输入电流和电压调节功能。与此同时，该器件还具有快速启动功能并能够以高达 1.3A 的电流限值为 VBUS 提供 5V 电压，因此可支持 USB On-the-Go 运行。

电源路径管理将系统电压调节为稍稍高于电池电压，但是又不会下降到低于 3.5V 最小系统电压（可编程）。借助于这个特性，即使在电池电量完全耗尽或者电池被拆除时，系统也能保持运行。当达到输入电流限值或电压限值时，电源路径管理自动将充电电流减少为 0。随着系统负载持续增加，电源路径在满足系统电源需求之前将电池放电。这个补充模式运行防止输入源过载。

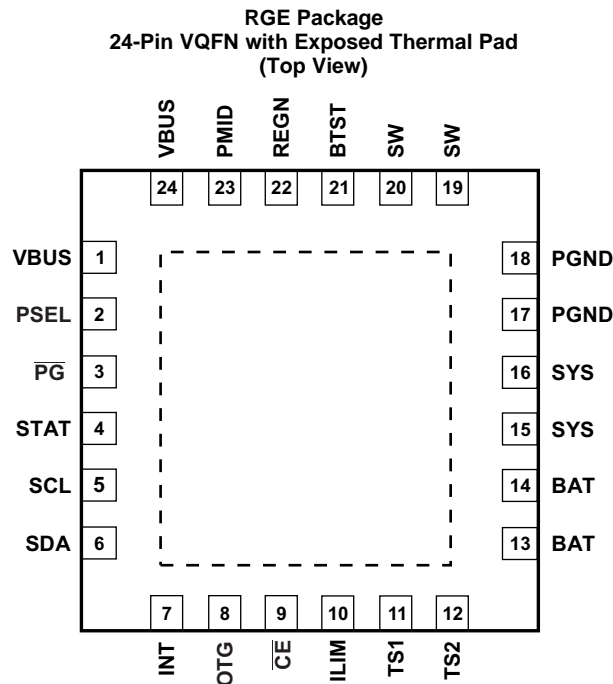
此器件在无需软件控制情况下启动并完成一个充电周期。它自动检测电池电压并通过三个阶段为电池充电：预充电、恒定电流和恒定电压。在充电周期的末尾，当充电电流低于在恒定电压阶段中预设定的限值时，充电器自动终止。当整个电池下降到低于再充电阈值时，充电器将自动启动另外一个充电周期。

此器件提供针对电池充电和系统运行的多种安全特性，其中包括两组负温度系数热敏电阻监视、充电安全计时器和过压、过流保护。当结温超过 120°C（可设定）时，热调节减少充电电流。

STAT 输出报告充电状态和任何故障条件。器件中的  $\overline{PG}$  输出指示电源是否正常。当故障发生时，INT 会立即通知主机。

该器件可提供 24 引脚 4x4 mm<sup>2</sup> 超薄 VQFN 封装。

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
VBUS	1,24	P	Charger Input Voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. (Refer to Application Information Section for details)
PSEL	2	I Digital	Power source selection input. High indicates a USB host source and Low indicates an adapter source.
$\overline{\text{PG}}$	3	O Digital	Open drain active low power good indicator. Connect to the pull up rail via 10kohm resistor. LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30mA.
STAT	4	O Digital	Open drain charge status output to indicate various charger operation. Connect to the pull up rail via 10kohm. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin has a 10kΩ resistor to ground.
SCL	5	I Digital	I <sup>2</sup> C Interface clock. Connect SCL to the logic rail through a 10kΩ resistor.
SDA	6	I/O Digital	I <sup>2</sup> C Interface data. Connect SDA to the logic rail through a 10kΩ resistor.
INT	7	O Digital	Open-drain Interrupt Output. Connect the INT to a logic rail via 10kΩ resistor. The INT pin sends active low, 256us pulse to host to report charger device status and fault.
OTG	8	I Digital	USB current limit selection pin during buck mode, and active high enable pin during boost mode. In buck mode with USB host (PSEL=High), when OTG = High, IIN limit = 500mA and when OTG = Low, IIN limit = 100mA. The boost mode is activated when the REG01[5:4]=10 and OTG pin is High.
$\overline{\text{CE}}$	9	I Digital	Active low Charge Enable pin. Battery charging is enabled when REG01[5:4]=01 and $\overline{\text{CE}}$ pin = Low. $\overline{\text{CE}}$ pin must be pulled high or low.
ILIM	10	I Analog	ILIM pin sets the maximum input current limit by regulating the ILIM voltage at 1V. A resistor is connected from ILIM pin to ground to set the maximum limit as $I_{\text{INMAX}} = (1V/R_{\text{ILIM}}) \times K_{\text{ILIM}}$ . The actual input current limit is the lower one set by ILIM and by I <sup>2</sup> C REG00[2:0]. The minimum input current programmed on ILIM pin is 500mA.
TS1	11	I Analog	Temperature qualification voltage input #1. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS1 to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor and do not add decoupling capacitor on TS1 pin.
TS2	12	I Analog	Temperature qualification voltage input #2. Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS1 to GND. Charge suspends when either TS pin is out of range. Recommend 103AT-2 thermistor and do not add decoupling capacitor on TS2 pin.

## Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
BAT	13,14	P	Battery connection point to the positive terminal of the battery pack. The internal BATFET is connected between BAT and SYS. Connect a 10uF closely to the BAT pin.
SYS	15,16	P	System connection point. The internal BATFET is connected between BAT and SYS. When the battery falls below the minimum system voltage, switch-mode converter keeps SYS above the minimum system voltage. (Refer to Application Information Section for inductor and capacitor selection)
PGND	17,18	P	Power ground connection for high-current power converter node. Internally, PGND is connected to the source of the n-channel LSFET. On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
SW	19,20	O Analog	Switching node connecting to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047uF bootstrap capacitor from SW to BTST.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the anode of the boost-strap diode. Connect the 0.047uF bootstrap capacitor from SW to BTST.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the boost-strap diode. For VBUS above 6V, connect 1-μF ceramic capacitor from REGN to analog GND. For VBUS below 6V, connect a 4.7-μF (10V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS1 and TS2 pins.
PMID	23	O Analog	Connected to the drain of the reverse blocking MOSFET and the drain of HSFET. Given the total input capacitance, connect a 1-μF capacitor on VBUS to PGND, and the rest all on PMID to PGND. (See the Application Information section for details)
Thermal Pad	–	P	Exposed pad beneath the IC for heat dissipation. Always solder thermal pad to the board, and have vias on the thermal pad plane star-connecting to PGND and ground plane for high-current power converter.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage range (with respect to GND)	VBUS	–2	20	V
	PMID, STAT, $\overline{\text{PG}}$	–0.3	20	V
	BTST	–0.3	26	V
	SW	–2	20	V
	BAT, SYS (converter not switching)	–0.3	6	V
	SDA, SCL, INT, OTG, ILIM, REGN, TS1, TS2, $\overline{\text{CE}}$ , PSEL	–0.3	7	V
	BTST TO SW	–0.3	7	V
	PGND to GND	–0.3	0.3	V
Output sink current	INT, STAT, $\overline{\text{PG}}$		6	mA
Junction temperature		–40	150	°C
Storage temperature, T <sub>stg</sub>		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{IN}$	Input voltage	3.9	17 <sup>(1)</sup>	V
$I_{IN}$	Input current		3	A
$I_{SYS}$	Output current (SYS)		4.5	A
$V_{BAT}$	Battery voltage		4.4	V
$I_{BAT}$	Fast charging current		4.5	A
	Discharging current with internal MOSFET		6 (continuous) 9 (peak) (up to 1 sec duration)	A
$T_A$	Operating free-air temperature range	–40	85	°C

- (1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either the BTST or SW pins. A tight layout minimizes switching noise.

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		bq24292i	UNIT
		RGE (VQFN)	
		24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.3	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	9.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.2	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

## 7.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values unless other noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>QUIESCENT CURRENTS</b>					
$I_{BAT}$	Battery discharge current (BAT, SW, SYS)	$V_{VBUS} < V_{UVLO}$ , $V_{BAT} = 4.2\text{ V}$ , leakage between BAT and VBUS			
				5	$\mu\text{A}$
		High-Z Mode, or no VBUS, BATFET disabled (REG07[5] = 1), $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$			
$I_{VBUS}$	Input supply current (VBUS)		12	20	$\mu\text{A}$
		High-Z Mode, or no VBUS, REG07[5] = 0, $T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$			
			32	55	$\mu\text{A}$
		$V_{VBUS} = 5\text{ V}$ , High-Z mode			
			15	30	$\mu\text{A}$
		$V_{VBUS} = 17\text{ V}$ , High-Z mode			
$I_{VBUS}$	Input supply current (VBUS)		30	50	$\mu\text{A}$
		$V_{VBUS} > V_{UVLO}$ , $V_{VBUS} > V_{BAT}$ , converter not switching			
			1.5	3	mA
		$V_{VBUS} > V_{UVLO}$ , $V_{VBUS} > V_{BAT}$ , converter switching, $V_{BAT}=3.2\text{ V}$ , $I_{SYS}=0\text{ A}$			
$I_{VBUS}$	Input supply current (VBUS)		4		mA
		$V_{VBUS} > V_{UVLO}$ , $V_{VBUS} > V_{BAT}$ , converter switching, $V_{BAT}=3.8\text{ V}$ , $I_{SYS}=0\text{ A}$			
$I_{VBUS}$	Input supply current (VBUS)		15		mA
		$V_{VBUS} > V_{UVLO}$ , $V_{VBUS} > V_{BAT}$ , converter switching, $V_{BAT}=3.8\text{ V}$ , $I_{SYS}=0\text{ A}$			
$I_{OTGBOOST}$	Battery Discharge Current in boost mode	$V_{BAT}=4.2\text{ V}$ , Boost mode, $I_{VBUS} = 0\text{ A}$ , converter switching			
			4		mA

## Electrical Characteristics (接下页)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VBUS/BAT POWER UP</b>						
$V_{VBUS\_OP}$	VBUS operating range		3.9		17	V
$V_{VBUS\_UVLOZ}$	VBUS for active I <sup>2</sup> C, no battery	$V_{VBUS}$ rising	3.6			V
$V_{SLEEP}$	Sleep mode falling threshold	$V_{VBUS}$ falling, $V_{VBUS}-V_{BAT}$	35	80	120	mV
$V_{SLEEPZ}$	Sleep mode rising threshold	$V_{VBUS}$ rising, $V_{VBUS}-V_{BAT}$	170	250	350	mV
$V_{ACOV}$	VBUS overvoltage rising threshold	$V_{VBUS}$ rising	17.4	18		V
$V_{ACOV\_HYST}$	VBUS Overvoltage Falling Hysteresis	$V_{VBUS}$ falling		700		mV
$V_{BAT\_UVLOZ}$	Battery for active I <sup>2</sup> C, no VBUS	$V_{BAT}$ rising	2.3			V
$V_{BAT\_DPL}$	Battery depletion threshold	$V_{BAT}$ falling		2.4	2.6	V
$V_{BAT\_DPL\_HY}$	Battery depletion rising hysteresis	$V_{BAT}$ rising		200	260	mV
$V_{VBUSMIN}$	Bad adapter detection threshold	$V_{VBUS}$ falling		3.8		V
$I_{BADSRC}$	Bad adapter detection current source			30		mA
<b>POWER PATH MANAGEMENT</b>						
$V_{SYS\_RANGE}$	Typical System regulation voltage	$I_{SYS} = 0\text{A}$ , Q4 off, $V_{BAT}$ up to 4.2 V, REG01[3:1]=101, $V_{SYSMIN} = 3.5\text{ V}$	3.5		4.35	V
$V_{SYS\_MIN}$	System voltage output	REG01[3:1]=101, $V_{SYSMIN} = 3.5\text{ V}$	3.55	3.65		V
$R_{ON(RBFET)}$	Internal top reverse blocking MOSFET on-resistance	Measured between VBUS and PMID		23	38	mΩ
$R_{ON(HSFET)}$	Internal top switching MOSFET on-resistance between PMID and SW	$T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$		27	35	mΩ
		$T_J = -40^{\circ}\text{C} - 125^{\circ}\text{C}$		27	45	
$R_{ON(LSFET)}$	Internal bottom switching MOSFET on-resistance between SW and PGND	$T_J = -40^{\circ}\text{C} - 85^{\circ}\text{C}$		32	45	mΩ
		$T_J = -40^{\circ}\text{C} - 125^{\circ}\text{C}$		32	48	
$V_{FWD}$	BATFET forward voltage in supplement mode	BAT discharge current 10mA		30		mV
$V_{SYS\_BAT}$	SYS/BAT Comparator	$V_{SYS}$ falling		90		mV
$V_{BATGD}$	Battery good comparator rising threshold	$V_{BAT}$ rising		3.55		V
$V_{BATGD\_HYST}$	Battery good comparator falling threshold	$V_{BAT}$ falling		100		mV
<b>BATTERY CHARGER</b>						
$V_{BAT\_REG\_ACC}$	Charge voltage regulation accuracy	$V_{BAT} = 4.112\text{V}$ and $4.208\text{V}$	-0.5%		0.5%	
$I_{CHG\_REG\_ACC}$	Fast charge current regulation accuracy	$V_{BAT} = 3.8\text{V}$ , $I_{CHG} = 1792\text{mA}$ , $T_J = 25^{\circ}\text{C}$	-4%		4%	
		$V_{BAT} = 3.8\text{V}$ , $I_{CHG} = 1792\text{mA}$ , $T_J = -20^{\circ}\text{C} - 125^{\circ}\text{C}$	-7%		7%	
$I_{CHG\_20pct}$	Charge current with 20% option on	$V_{BAT} = 3.1\text{V}$ , $I_{CHG} = 104\text{mA}$ , REG02=03		75	150	mA
$V_{BATLOWV}$	Battery LOWV falling threshold	Fast charge to precharge, REG04[1] = 1	2.6	2.8	2.9	V
$V_{BATLOWV\_RISE}$	Battery LOWV rising threshold	Precharge to fast charge, REG04[1] = 1	2.8	3.0	3.1	V
$I_{PRECHG\_ACC}$	Precharge current regulation accuracy	$V_{BAT} = 2.6\text{V}$ , $I_{CHG} = 256\text{mA}$	-20%		20%	
$I_{TERM\_ACC}$	Termination current accuracy	$I_{TERM} = 256\text{mA}$ , $I_{CHG} = 960\text{mA}$	-20%		20%	
$V_{SHORT}$	Battery Short Voltage	$V_{BAT}$ falling		2		V
$V_{SHORT\_HYST}$	Battery Short Voltage hysteresis	$V_{BAT}$ rising		200		mV
$I_{SHORT}$	Battery short current	$V_{BAT} < 2.2\text{V}$		100		mA
$V_{RECHG}$	Recharge threshold below $V_{BAT\_REG}$	$V_{BAT}$ falling, REG04[0] = 0		100		mV
$R_{ON\_BATFET}$	SYS-BAT MOSFET on-resistance	$T_J = 25^{\circ}\text{C}$		12	15	mΩ
		$T_J = -40^{\circ}\text{C} - 125^{\circ}\text{C}$		12	20	

## Electrical Characteristics (接下页)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE/CURRENT REGULATION						
V <sub>INDPM_REG_ACC</sub>	Input voltage regulation accuracy	REG00[6:3]=0110 (4.36V) or 1011 (4.76V)	-2%		2%	
I <sub>USB_DPM</sub>	USB Input current regulation limit, VBUS = 5V, current pulled from SW	USB100	85		100	mA
		USB150	125		150	mA
		USB500	440		500	mA
		USB900	750		900	mA
I <sub>ADPT_DPM</sub>	Input current regulation accuracy	Input current limit 1.5A, REG00[2:0] = 101	1.30		1.55	A
I <sub>IN_START</sub>	Input current limit during system start up	VSYS<2.2V		100		mA
K <sub>ILIM</sub>	I <sub>IN</sub> = K <sub>ILIM</sub> /R <sub>ILIM</sub>	I <sub>INDPM</sub> = 1.5A		485	530	A x Ω
BAT OVERVOLTAGE PROTECTION						
V <sub>BATOV_P</sub>	Battery overvoltage threshold	V <sub>BAT</sub> rising, as percentage of V <sub>BAT_REG</sub>		104%		
V <sub>BATOV_P_HYST</sub>	Battery overvoltage hysteresis	V <sub>BAT</sub> falling, as percentage of V <sub>BAT_REG</sub>		2%		
THERMAL REGULATION AND THERMAL SHUTDOWN						
T <sub>Junction_REG</sub>	Junction temperature regulation accuracy	REG06[1:0] = 11	115	120	125	°C
T <sub>SHUT</sub>	Thermal shutdown rising temperature	Temperature increasing		160		°C
T <sub>SHUT_HYS</sub>	Thermal shutdown hysteresis			30		°C
COLD/HOT THERMISTER COMPARATOR						
V <sub>LTF</sub>	Cold temperature threshold, TS pin voltage rising threshold	Charger suspends charge. As Percentage to V <sub>REGN</sub>	73%	73.5%	74%	
V <sub>LTF_HYS</sub>	Cold temperature hysteresis, TS pin voltage falling	As Percentage to V <sub>REGN</sub>	0.2%	0.4%	0.6%	
V <sub>HTF</sub>	Hot temperature TS pin voltage falling threshold	As Percentage to V <sub>REGN</sub>	46.6%	47.2%	48.8%	
V <sub>TCO</sub>	Cut-off temperature TS pin voltage falling threshold	As Percentage to V <sub>REGN</sub>	44.2%	44.7%	45.2%	
CHARGE OVERCURRENT COMPARATOR						
I <sub>HSFET_OCP</sub>	HSFET overcurrent threshold		5.3	7		A
I <sub>BATFET_OCP</sub>	System over load threshold		9			A
CHARGE UNDERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V <sub>LSFET_UCP</sub>	LSFET charge undercurrent falling threshold	From sync mode to non-sync mode		100		mA
PWM OPERATION						
D <sub>MAX</sub>	Maximum PWM duty cycle			97%		
V <sub>BTST_REFRESH</sub>	Bootstrap refresh comparator threshold	VBTST-VSW when LSFET refresh pulse is requested, VBUS=5V		3.6		V
		VBTST-VSW when LSFET refresh pulse is requested, VBUS>6V		4.5		
BOOST MODE OPERATION						
V <sub>OTG_REG</sub>	OTG output voltage	I <sub>(VBUS)</sub> = 0		5		V
V <sub>OTG_REG_ACC</sub>	OTG output voltage accuracy	I <sub>(VBUS)</sub> = 0	-2.5%		2%	
I <sub>OTG</sub>	OTG mode output current	REG01[0] = 0	0.5			A
		REG01[0] = 1	1.3			A
V <sub>OTG_OVP</sub>	OTG overvoltage threshold			5.3	5.5	V
I <sub>OTG_ILIM</sub>	LSFET cycle-by-cycle current limit		3.2	4.6		A
I <sub>OTG_HSZCP</sub>	HSFET under current falling threshold			100		mA
I <sub>RBFET_OCP</sub>	RBFET overcurrent threshold	REG01[0] = 1	1.4	1.8	2.7	A
		REG01[0] = 0	0.6	1.1	1.8	
REGN LDO						
V <sub>REGN</sub>	REGN LDO output voltage	V <sub>VBUS</sub> = 10V, I <sub>REGN</sub> = 40mA	5.6	6	6.4	V
		V <sub>VBUS</sub> = 5V, I <sub>REGN</sub> = 20mA	4.75	4.8		V
I <sub>REGN</sub>	REGN LDO current limit	V <sub>VBUS</sub> = 10V, V <sub>REGN</sub> = 3.8V	50			mA



## Electrical Characteristics (接下页)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{ACOV}$  and  $V_{VBUS} > V_{BAT} + V_{SLEEP}$ ,  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $T_J = 25^{\circ}\text{C}$  for typical values unless other noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LOGIC I/O PIN CHARACTERISTICS (OTG, <math>\overline{\text{CE}}</math>, PSEL, STAT, <math>\overline{\text{PG}}</math>)</b>						
$V_{ILO}$	Input low threshold				0.4	V
$V_{IH}$	Input high threshold		1.3			V
$V_{OUT\_LO}$	Output low saturation voltage	Sink current = 5 mA			0.4	V
$I_{BIAS}$	High level leakage current	Pull up rail 1.8V			1	$\mu\text{A}$
<b>I<sup>2</sup>C INTERFACE (SDA, SCL, INT)</b>						
$V_{IH}$	Input high threshold level	VPULLUP = 1.8V, SDA and SCL	1.3			V
$V_{IL}$	Input low threshold level	VPULLUP = 1.8V, SDA and SCL			0.4	V
$V_{OL}$	Output low threshold level	Sink current = 5mA			0.4	V
$I_{BIAS}$	High-level leakage current	VPULLUP = 1.8V, SDA and SCL			1	$\mu\text{A}$

## 7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
tBADSRC	Bad source detection duration		30			ms
BOOST MODE OPERATION						
tOTG_DLY	OTG mode enable delay	I(VBUS) = 0 From OTG pin high to VBUS=VOTG_REG Specified by Design	22	50	ms	
tOTG_OCP_OFF	OTG mode overcurrent protection off cycle time		32			ms
tOTG_OCP_ON	OTG mode overcurrent protection on cycle time		100			μs
DIGITAL CLOCK AND WATCHDOG TIMER						
fHIZ	Digital crude clock	REGN LDO disabled	15	35	50	kHz
fDIG	Digital clock	REGN LDO enabled	1300	1500	1700	kHz
tWDT	Watchdog timer	REGN LDO enabled REG05[5:4]=11	136	160	s	
I2C INTERFACE (SDA, SCL, INT)						
fSCL	SCL clock frequency		400			kHz

## 7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>BATTERY CHARGER</b>						
$t_{RECHG}$	Recharge deglitch time	VBAT falling, REG04[0]=0		20		ms
<b>BAT OVERVOLTAGE PROTECTION</b>						
$t_{BATOVP}$	Battery overvoltage deglitch time to disable charge			1		$\mu\text{s}$
<b>THERMAL REGULATION AND THERMAL SHUTDOWN</b>						
	Thermal shutdown rising deglitch	Temperature increasing delay		1		ms
	Thermal shutdown falling deglitch	Temperature decreasing delay		1		ms
<b>PWM OPERATION</b>						
$F_{SW}$	PWM Switching frequency, and digital clock		1300	1500	1700	kHz
<b>COLD/HOT THERMISTOR COMPARATOR</b>						
	Deglitch time for temperature out of range detection	$V_{TS} > V_{LTF}$ , or $V_{TS} < V_{TCO}$ , or $V_{TS} < V_{HTF}$		10		ms

## 7.8 Typical Characteristics

表 1. Tables of Figures

	FIGURE NO.
Charging Efficiency vs. Charging Current	图 1
System Light Load Efficiency vs System Load current	图 2
Boost Mode Efficiency vs VBUS Load Current	图 3
SYS Voltage Regulation vs System Load	图 4
Boost Mode VBUS Voltage Regulation vs VBUS Load Current	图 5
SYS Voltage vs Temperature	图 6
BAT Voltage vs Temperature	图 7
Input Current Limit vs Temperature	图 8
Charge Current vs Temperature	图 9

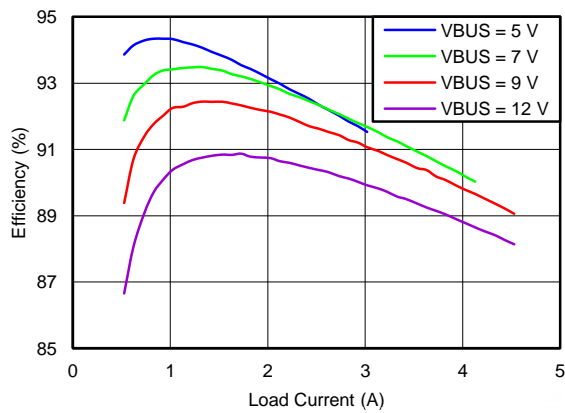


图 1. Charging Efficiency vs Charging Current

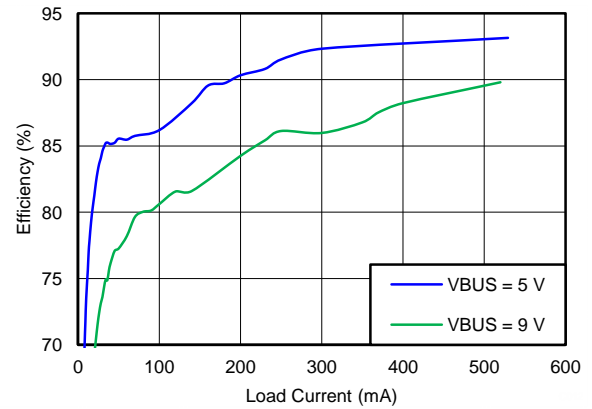


图 2. System Light Load Efficiency vs System Load Current

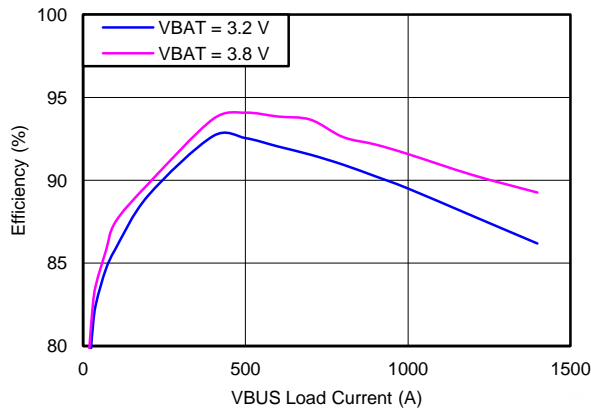


图 3. Boost Mode Efficiency vs VBUS Load Current

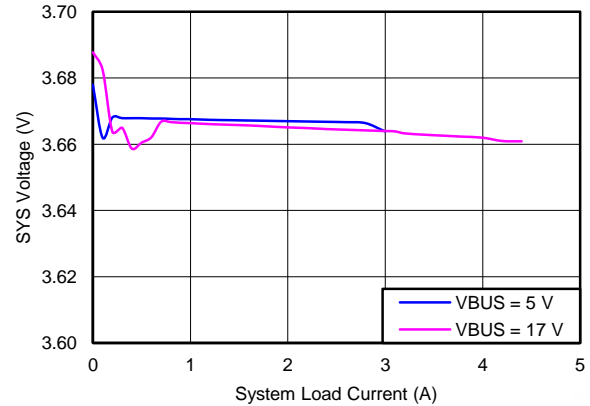
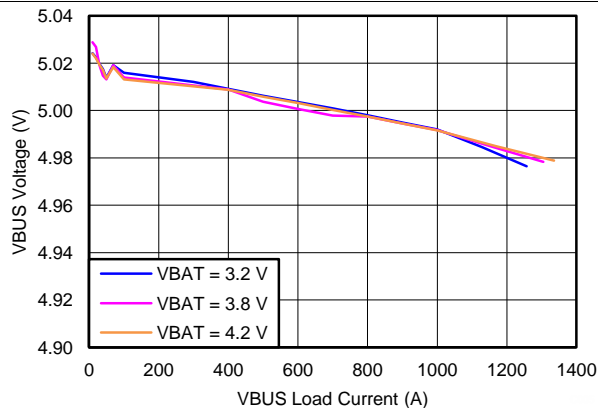
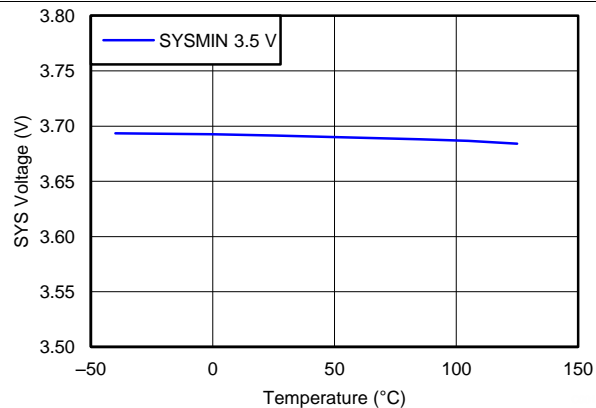


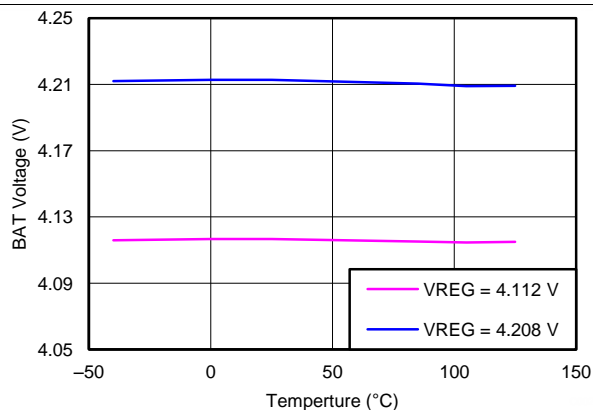
图 4. SYS Voltage Regulation vs System Load



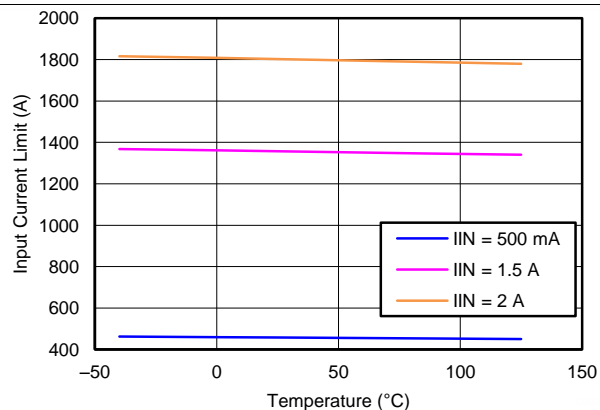
**图 5. Boost Mode VBUS Voltage Regulation vs VBUS Load Current**



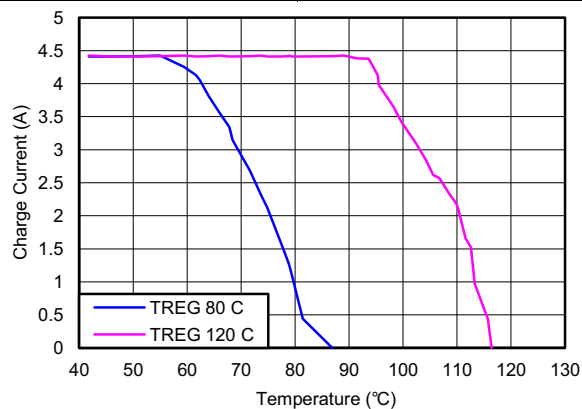
**图 6. SYS Voltage vs Temperature**



**图 7. BAT Voltage vs Temperature**



**图 8. Input Current Limit vs Temperature**



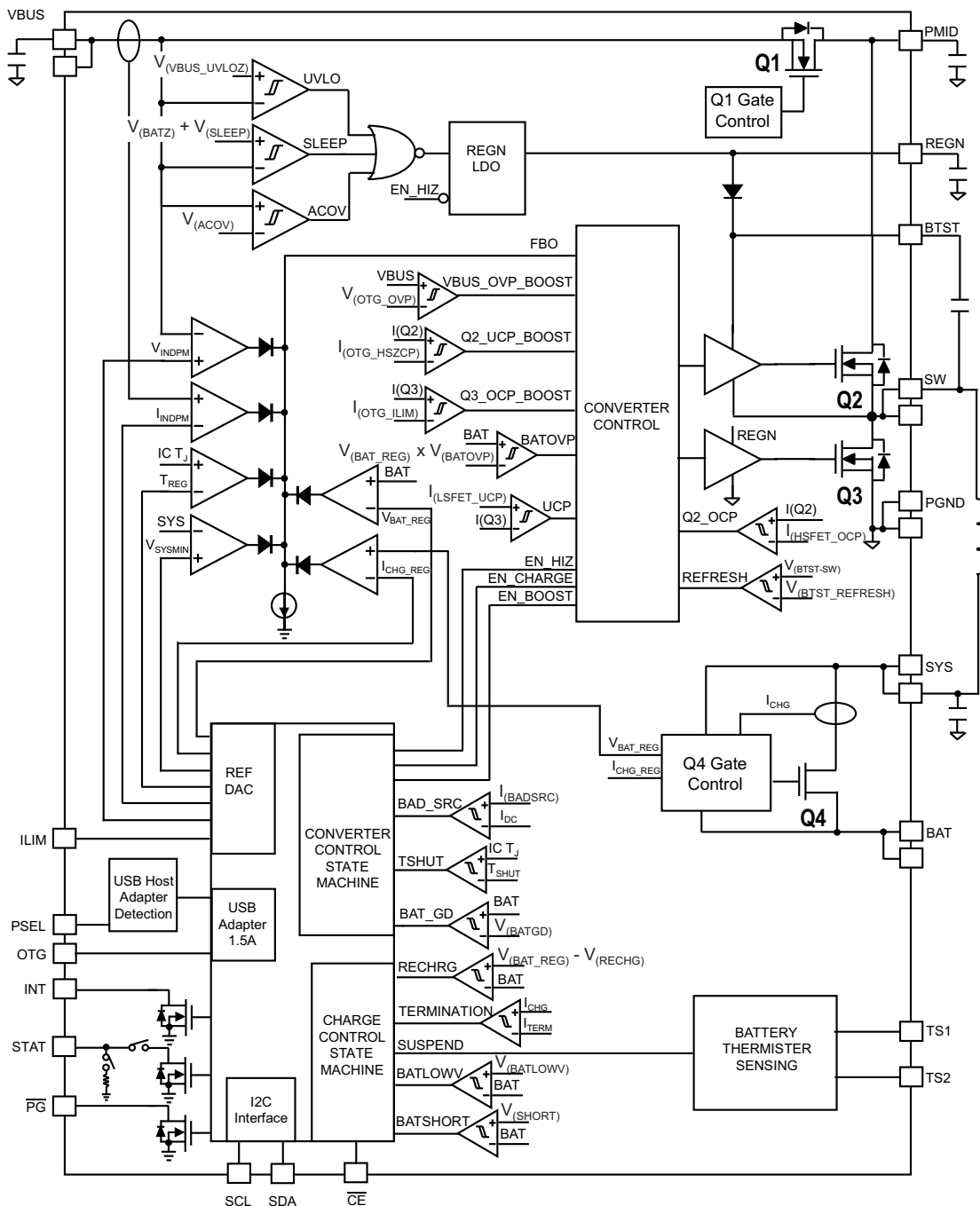
**图 9. Charge Current vs Temperature**

## 8 Detailed Description

### 8.1 Overview

The bq24292i is an I<sup>2</sup>C controlled power path management device and a single cell Li-Ion battery charger. It integrates the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between system and battery. The device also integrates the bootstrap diode for the high-side gate drive.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Device Power Up

#### 8.3.1.1 Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and BAT. When VBUS or VBAT rises above UVLOZ, the sleep comparator, battery depletion comparator and BATFET driver are active. I<sup>2</sup>C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

#### 8.3.1.2 Power Up from Battery without DC Source

If only battery is present and the voltage is above depletion threshold ( $V_{BAT\_DEPL}$ ), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low  $R_{DS(on)}$  in BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time. The device always monitors the discharge current through BATFET. When the system is overloaded or shorted, the device will immediately turn off BATFET and keep BATFET off until the input source plugs in again.

##### 8.3.1.2.1 BATFET Turn Off

The BATFET can be forced off by the host through I<sup>2</sup>C REG07[5]. This bit allows the user to independently turn off the BATFET when the battery condition becomes abnormal during charging. When BATFET is off, there is no path to charge or discharge the battery.

When battery is not attached, the BATFET should be turned off by setting REG07[5] to 1 to disable charging and supplement mode.

##### 8.3.1.2.2 Shipping Mode

When end equipment is assembled, the system is connected to battery through BATFET. There will be a small leakage current to discharge the battery even when the system is powered off. To extend the battery life during shipping and storage, the device can turn off BATFET so that the system voltage is zero to minimize the leakage.

To keep BATFET off during shipping mode, the host has to disable the watchdog timer (REG05[5:4]=00) and disable BATFET (REG07[5]=1) at the same time.

Once the BATFET is disabled, the BATFET can be turned on by plugging in adapter.

#### 8.3.1.3 Power Up from DC Source

When the DC source plugs in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It also checks the input current limit before starts the buck converter.

##### 8.3.1.3.1 REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The LDO also provides bias rail to TS1/TS2 external resistors. The pullup rail of STAT and  $\overline{PG}$  can be connected to REGN as well.

The REGN is enabled when all of the following conditions are valid:

- VBUS above UVLOZ
- VBUS above battery +  $V_{SLEEPZ}$  in buck mode or VBUS below battery +  $V_{SLEEPZ}$  in boost mode
- After typical 220ms delay (100ms minimum) is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than 50 $\mu$ A from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

##### 8.3.1.3.2 Input Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements to start the buck converter.

1. VBUS voltage below 18V (not in ACOV)

## Feature Description (接下页)

2. VBUS voltage above 3.8V when pulling 30mA (poor source detection)

Once the input source passes all the conditions above, the status register REG08[2] goes high and the  $\overline{\text{PG}}$  pin goes low. An INT is asserted to the host.

If the device fails the poor source detection, it will repeat the detection every 2 seconds.

### 8.3.1.3.3 Input Current Limit Detection

The USB ports on personal computers are convenient charging source for portable devices (PDs). If the portable device is attached to a USB host, the USB specification requires the portable device to draw limited current (100mA/500mA in USB 2.0, and 150mA/900mA in USB 3.0). If the portable device is attached to a charging port, it is allowed to draw up to 1.5A.

After the  $\overline{\text{PG}}$  is LOW or REG08[2] goes HIGH, the charger device always runs input current limit detection when a DC source plugs in unless the charger is in HIZ during host mode.

The device sets input current limit through PSEL and OTG pins.

After the input current limit detection is done, the host can write to REG00[2:0] to change the input current limit.

### 8.3.1.3.4 PSEL/OTG Pins Set Input Current Limit

The device has PSEL which directly takes the USB PHY device output to decide whether the input is USB host or charging port.

**表 2. Input Current Limit Detection**

PSEL	OTG	INPUT CURRENT LIMIT	REG08[7:6]
HIGH	LOW	100 mA	01
HIGH	HIGH	500 mA	01
LOW	—	1.5A	10

### 8.3.1.3.5 HIZ State with 100mA USB Host

In battery charging spec, the good battery threshold is the minimum charge level of a battery to power up the portable device successfully. When the input source is 100mA USB host, and the battery is above bat-good threshold ( $V_{\text{BATGD}}$ ), the device follows battery charging spec and enters high impedance state (HIZ). In HIZ state, the device is in the lowest quiescent state with REGN LDO and the bias circuits off. The charger device sets REG00[7] to 1, and the VBUS current during HIZ state will be less than 30 $\mu$ A. The system is supplied by the battery.

Once the charger device enters HIZ state in host mode, it stays in HIZ until the host writes REG00[7]=0. When the processor host wakes up, it is recommended to first check if the charger is in HIZ state.

In default mode, the charger IC will reset REG00[7] back to 0 when input source is removed. When another source plugs in, the charger IC will run detection again, and update the input current limit.

### 8.3.1.3.6 Force Input Current Limit Detection

The host can force the charger device to run input current limit detection by setting REG07[7]=1. After the detection is complete, REG07[7] will return to 0 by itself.

### 8.3.1.4 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The device provides soft-start when ramp up the system rail. When the system rail is below 2.2V, the input current limit is forced to 100mA. After the system rises above 2.2V, the charger device sets the input current limit set by the lower value between register and ILIM pin.

As a battery charger, the device deploys a 1.5MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

A type III compensation network allows using ceramic capacitors at the output of the converter. An internal saw-tooth ramp is compared to the internal error control signal to vary the duty cycle of the converter. The ramp height is proportional to the PMID voltage to cancel out any loop gain variation due to a change in input voltage.

To improve light-load efficiency, the device switches to PFM control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

### **8.3.1.5 Boost Mode Operation from Battery**

The device can operate in boost converter mode to support USB On-The-Go (OTG) standard with fast startup and deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500mA output requirement. The maximum output current is 1.3A. The boost operation can be enabled only if all of the following conditions are valid:

- BAT above BATLOWV threshold ( $V_{BATLOWV}$  set by REG04[1])
- VBUS less than BAT+ $V_{SLEEP}$  (in sleep mode)
- Boost mode operation is enabled (OTG pin HIGH and REG01[5:4]=10)
- After  $t_{OTG\_DLY}$  (22ms typical) delay from boost mode enable

In boost mode, the device employs a 1.5MHz step-up switching regulator. Similar to buck operation, the device switches from PWM operation to PFM operation at light load to improve efficiency.

During boost mode, the status register REG08[7:6] is set to 11, the VBUS output is 5V and the output current can reach up to 500mA or 1.3A, selected via I<sup>2</sup>C (REG01[0]).

Any fault during boost operation, including VBUS overvoltage or overcurrent, sets the fault register REG09[6] to 1 and an INT is asserted.

## **8.3.2 Power Path Management**

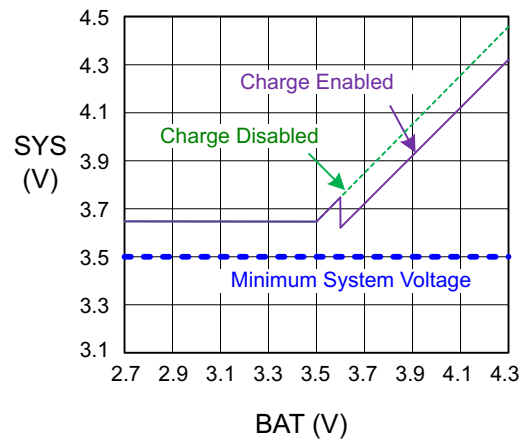
The device accommodates a wide range of input sources from USB, wall adapter, to car battery. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

### **8.3.2.1 Narrow VDC Architecture**

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by REG01[3:1]. Even with a fully depleted battery, the system is regulated above the minimum system voltage (default 3.5V).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is 150mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the  $V_{DS}$  of BATFET.

When the battery charging is disabled or terminated, the system is always regulated at 150mV above the minimum system voltage setting. The status register REG08[0] goes high when the system is in minimum system voltage regulation.


**图 10. V(SYS) vs V(BAT)**

### 8.3.2.2 Dynamic Power Management

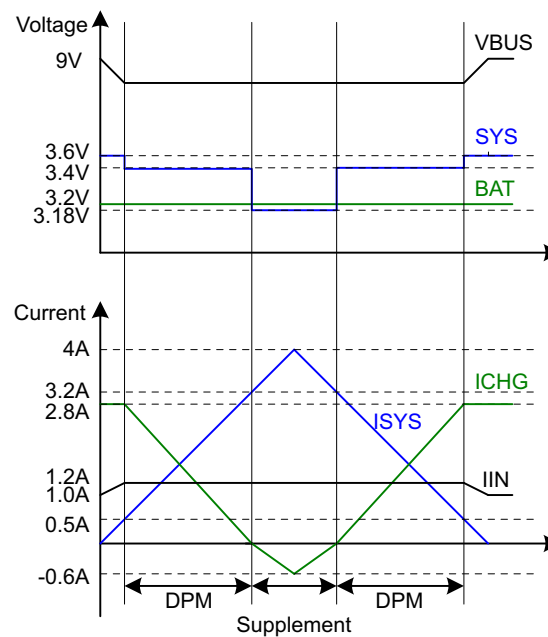
To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage.

When input source is over-loaded, either the current exceeds the input current limit (REG00[2:0]) or the voltage falls below the input voltage limit (REG00[6:3]). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode (either VINDPM or IINDPM), the status register REG08[3] will go high.

图 11 shows the DPM response with 9V/1.2A adapter, 3.2V battery, 2.8A charge current and 3.4V minimum system voltage setting.


**图 11. DPM Response**



### 8.3.2.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET  $V_{DS}$  stays at 30mV when the current is low. This prevents oscillation from entering and exiting the supplement mode. As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce  $R_{DS(on)}$  until the BATFET is in full conduction. At this point onwards, the BATFET  $V_{DS}$  linearly increases with discharge current. 图 12 shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

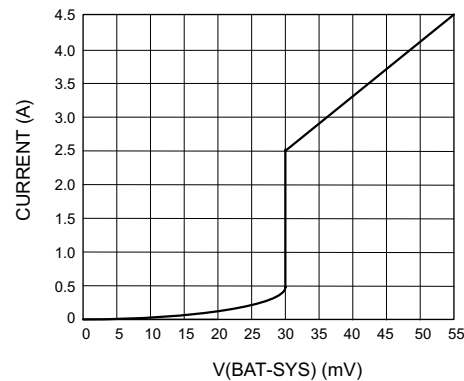


图 12. BATFET V-I Curve

### 8.3.3 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 4.5A charge current for high capacity tablet battery. The 12mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

#### 8.3.3.1 Autonomous Charging Cycle

With battery charging enabled at POR (REG01[5:4]=01), the device can complete a charging cycle without host involvement. The device default charging parameters are listed in .

表 3. Charging Parameter Default Setting

DEFAULT MODE	bq24292i
Charging Voltage	4.112 V
Charging Current	1.024 A
Pre-charge Current	256 mA
Termination Current	256 mA
Temperature Profile	Hot/Cold
Safety Timer	8 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by I<sup>2</sup>C register bit (REG01[5:4]) = 01 and  $\overline{CE}$  is low
- No thermistor fault on TS1 and TS2
- No safety timer fault
- BATFET is not forced to turn off (REG07[5])

The charger device automatically terminates the charging cycle when the charging current is below termination threshold and charge voltage is above recharge threshold. When a full battery voltage is discharged below recharge threshold (REG04[0]), the device automatically starts another charging cycle. After charging is done, either toggle  $\overline{CE}$  pin or REG01[5:4] will initiate a new charging cycle.

The STAT output indicates the charging status of charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The status register REG08[5:4] indicates the different charging phases: 00-charging disable, 01-precharge, 10-fast charge (constant current) and constant voltage mode, 11-charging done. Once a charging cycle is complete, an INT is asserted to notify the host.

The host can always control the charging operation and optimize the charging parameters by writing to the registers through I<sup>2</sup>C.

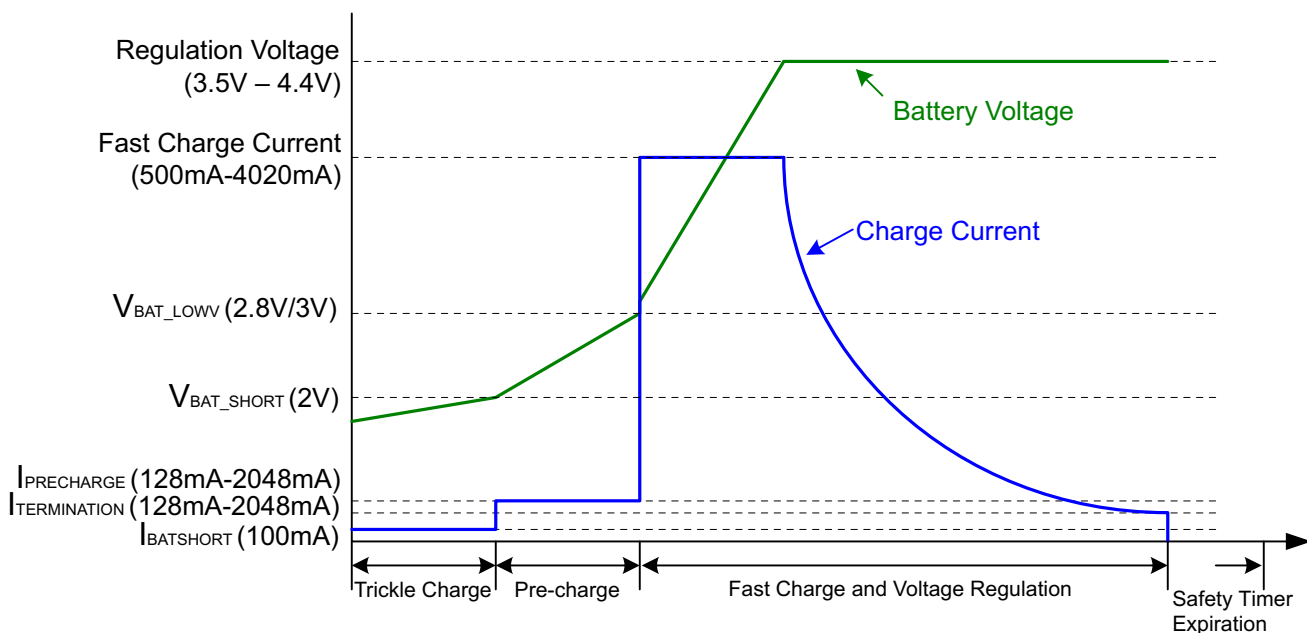
### 8.3.3.2 Battery Charging Profile

The device charges the battery in three phases: preconditioning, constant current and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and applies current.

**表 4. Charging Current Setting**

V <sub>BAT</sub>	CHARGING CURRENT	REG DEFAULT SETTING	REG08[5:4]
<2V	100mA	–	01
2V-3V	REG03[7:4]	256mA	01
>3V	REG02[7:2]	1024mA	10

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.



**图 13. Battery Charging Profile**

### 8.3.3.3 Battery Path Impedance IR Compensation

To speed up the charging cycle, we would like to stay in constant current mode as long as possible. In real system, the parasitic resistance, including routing, connector, MOSFETs and sense resistor in the battery pack, may force the charger device to move from constant current loop to constant voltage loop too early, extending the charge time.

The device allows the user to compensate for the parasitic resistance by increasing the voltage regulation set point according to the actual charge current and the resistance. For safe operation, the user should set the maximum allowed regulation voltage to REG06[4:2], and the minimum trace parasitic resistance (REG06[7:5]).

$$V_{\text{BATREG\_ACTUAL}} = V_{\text{BATREG\_I2C}} + \text{lower of } (I_{\text{CHRG\_ACTUAL}} \times R_{\text{COMP}}) \text{ and } V_{\text{CLAMP}} \quad (1)$$

### 8.3.3.4 Thermistor Qualification

The high capacity battery usually has two or more single cells in parallel. The device provides two TS pins to monitor the thermistor (NTC) in each cell independently.

#### 8.3.3.4.1 Cold/Hot Temperature Window

The device continuously monitors battery temperature by measuring the voltage between the TS pins and ground, typically determined by a negative temperature coefficient thermistor and an external voltage divider. The device compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the  $V_{LTF}$  to  $V_{HTF}$  thresholds. During the charge cycle the battery temperature must be within the  $V_{LTF}$  to  $V_{TCO}$  thresholds, else the device suspends charging and waits until the battery temperature is within the  $V_{LTF}$  to  $V_{HTF}$  range.

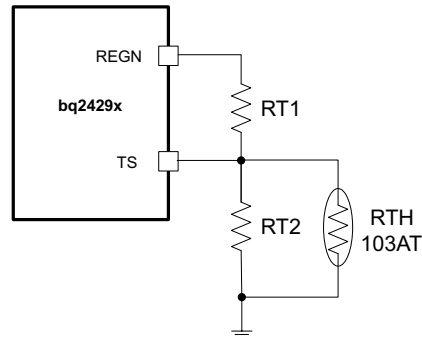


图 14. TS Resistor Network

When the TS fault occurs, the fault register REG09[2:0] indicates the actual condition on each TS pin and an INT is asserted to the host. The STAT pin indicates the fault when charging is suspended.

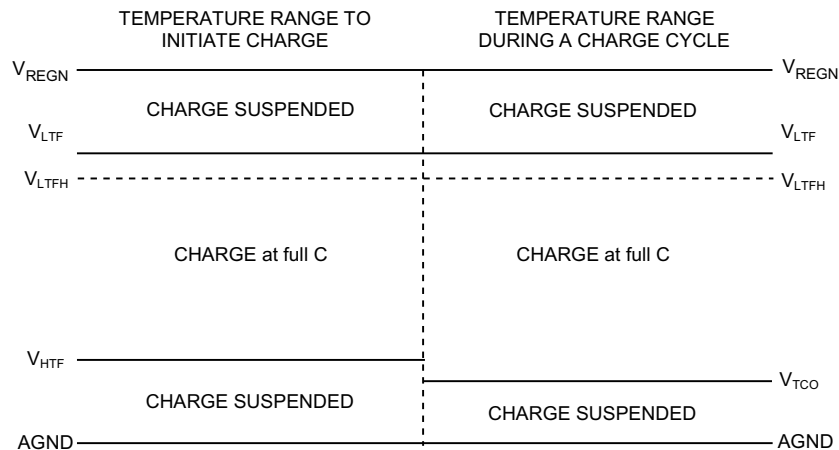


图 15. TS Pin Thermistor Sense Thresholds

Assuming a 103AT NTC thermistor is used on the battery pack 公式 2, the value RT1 and RT2 can be determined by using the following equation:

$$RT2 = \frac{V_{REGN} \times RTH_{COLD} \times RTH_{HOT} \times \left( \frac{1}{V_{LTF}} - \frac{1}{V_{TCO}} \right)}{RTH_{HOT} \times \left( \frac{V_{REGN}}{V_{TCO}} - 1 \right) - RTH_{COLD} \times \left( \frac{V_{REGN}}{V_{LTF}} - 1 \right)}$$

$$RT1 = \frac{\frac{V_{REGN}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}}$$
(2)

Select 0°C to 45°C range for Li-ion or Li-polymer battery,

$RTH_{COLD} = 27.28 \text{ k}\Omega$

$RTH_{HOT} = 4.911 \text{ k}\Omega$

$RT1 = 5.52 \text{ k}\Omega$

$RT2 = 31.23 \text{ k}\Omega$

### 8.3.3.5 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is complete, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn back on to engage supplement mode.

When termination occurs, the status register REG08[5:4] is 11, and an INT is asserted to the host. Termination is temporarily disabled if the charger device is in input current/voltage regulation or thermal regulation. Termination can be disabled by writing 0 to REG05[7].

#### 8.3.3.5.1 Termination when FORCE\_20PCT (REG02[0]) = 1

When REG02[0] is HIGH to reduce the charging current by 80%, the charging current could be less than the termination current. The charger device termination function should be disabled. When the battery is charged to fully capacity, the host can disable charging through  $\overline{CE}$  pin or REG01[5:4].

#### 8.3.3.5.2 Termination when TERM\_STAT (REG05[6]) = 1

Usually the STAT bit indicates charging complete when the charging current falls below termination threshold. Write REG05[6]=1 to enable an early “charge done” indication on STAT pin. The STAT pin goes high when the charge current reduces below 800mA. The charging cycle is still on-going until the current falls below the termination threshold.

### 8.3.3.6 Charging Safety Timer

The device has safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below BATLOWV threshold. The user can program fast charge safety timer through I2C (REG05[2:1]). When safety timer expires, the fault register REG09[5:4] goes 11 and an INT is asserted to the host. The safety timer feature can be disabled via I2C (REG05[3]). The following actions restart the safety timer:

The following actions restart the safety timer:

- At the beginning of a new charging cycle
- Toggle the  $\overline{CE}$  pin HIGH to LOW to HIGH (charge enable)
- Write REG01[5:4] from 00 to 01 (charge enable)
- Write REG05[3] from 0 to 1 (safety timer enable)

During input voltage/current regulation, thermal regulation, or when FORCE\_20PCT (REG02[0]) bit is set, , the safety timer counts at half clock rate since the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM) throughout the whole charging cycle, and the safety time is set to 5 hours, the safety timer will expire in 10 hours. This feature can be disabled by writing 0 to REG07[6].

It is recommended to disable safety timer first by clearing REG05[3] bit before safety timer configuraiton is changed. The safety timer can be re-enabled by setting REG05[3] bit.

### 8.3.3.7 USB Timer when Charging from USB100mA Source

The total charging time in default mode from USB100mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

## 8.3.4 Status Outputs ( $\overline{\text{PG}}$ , STAT, and INT)

### 8.3.4.1 Power Good Indicator ( $\overline{\text{PG}}$ )

The  $\overline{\text{PG}}$  in the device goes LOW to indicate a good input source when all of the following conditions are met:

- VBUS above UVLO
- VBUS above battery (not in sleep)
- VBUS below ACOV threshold
- VBUS above 3.8V when 30mA current is applied (not a poor source)

### 8.3.4.2 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED as the application diagram shows.

**表 5. STAT Pin State**

CHARGING STATE	STAT
Charging in progress (including recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input overvoltage, TS fault, timer fault, input or system overvoltage)	10k $\Omega$ pull down

When a fault occurs, instead of blinking, the STAT pin in the charger device has a 10k $\Omega$  pulldown resistor to ground. When the pullup resistor is 30k $\Omega$ , the STAT voltage during fault is 1/4 of the pullup rail.

### 8.3.4.3 Interrupt to Host (INT)

In some applications, the host does not always monitor the charger operation. The INT notifies the system on the device operation. The following events will generate 256us INT pulse.

- USB/adaptor source identified (through PSEL and OTG pins)
- Good input source detected
  - Not in sleep
  - Not in ACOV
  - Current limit above 30mA
- Input removed or ACOV
- Charge Complete
- Any FAULT event in REG09

When a fault occurs, the charger device sends out INT and latches the fault state in REG09 until the host reads the fault register. Before the host reads REG09, the charger device would not send any INT upon new faults except NTC fault (REG09[2:0]). The NTC fault is not latched and always reports the current thermistor conditions. To read the current fault status, the host has to read REG09 two times consecutively. The 1<sup>st</sup> reads fault register status from the last INT and the 2<sup>nd</sup> reads the current fault register status.

## 8.3.5 Protections

### 8.3.5.1 Input Current Limit on ILIM

For safe operation, the device has an additional hardware pin on ILIM to limit maximum input current on ILIM pin. The input maximum current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{1V}{R_{ILIM}} \times K_{ILIM} \quad (3)$$

The actual input current limit is the lower value between ILIM setting and register setting (REG00[2:0]). For example, if the register setting is 111 for 3A, and ILIM has a 353Ω resistor to ground for 1.5A, the input current limit is 1.5A. ILIM pin can be used to set the input current limit rather than the register settings.

The device regulates ILIM pin at 1V. If ILIM voltage exceeds 1V, the device enters input current regulation (Refer to *Dynamic Power Path Management* section).

The voltage on ILIM pin is proportional to the input current. ILIM pin can be used to monitor the input current following 公式 4:

$$I_{IN} = \frac{V_{ILIM}}{1V} \times I_{INMAX} \quad (4)$$

For example, if ILIM pin sets 2A, and the ILIM voltage is 0.6V, the actual input current 1.2A. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 1V. If ILIM pin is short, the input current limit is set by the register.

### 8.3.5.2 Thermal Regulation and Thermal Shutdown

The charger device monitors the internal junction temperature  $T_J$  to avoid overheat the chip and limits the IC surface temperature. When the internal junction temperature exceeds the preset limit (REG06[1:0]), the device lowers down the charge current. The wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register REG08[1] goes high.

Additionally, the device has thermal shutdown to turn off the converter. The fault register REG09[5:4] is 10 and an INT is asserted to the host.

### 8.3.5.3 Voltage and Current Monitoring in Buck Mode

The charger device closely monitors the input and system voltage, as well as HSFET and LSFET current for safe buck mode operation.

#### 8.3.5.3.1 Input Overvoltage (ACOV)

The maximum input voltage for buck mode operation is 18V. If VBUS voltage exceeds 18V, the device stops switching immediately. During input over voltage (ACOV), the fault register REG09[5:4] will be set to 01. An INT is asserted to the host.

#### 8.3.5.3.2 System Overvoltage Protection (SYSOVP)

The charger device monitors the voltage at SYS. When system overvoltage is detected, the converter is stopped to protect components connected to SYS from high voltage damage.

### 8.3.5.4 Overcurrent Protection in Boost Mode

The charger device closely monitors the Q1, Q2(HSFET) and Q3(LSFET) current to ensure safe boost mode operation. During overcurrent condition, the device will operate in hiccup mode for protection. While in hiccup mode cycle, the device turns off Q1 FET for  $t_{OTG\_OCP\_OFF}$  (32ms typical) and turns on Q1 FET for  $t_{OTG\_OCP\_ON}$  (100us typical) in an attempt to restart. If the overcurrent condition is removed, the boost converter will maintain the Q1 FET on state and the VBUS OTG output will operate normally. When overcurrent condition continues to exist, the device will repeat the hiccup cycle until overcurrent condition is removed.

#### 8.3.5.4.1 VBUS Overvoltage Protection in Boost Mode

The boost mode regulated output is 5V. When an adapter plugs in during boost mode, the VBUS voltage will rise above regulation target. Once the VBUS voltage exceeds  $V_{OTG\_OVP}$ , the charger device stops switching and the device exits boost mode. The fault register REG09[6] is set high to indicate fault in boost operation. An INT is asserted to the host.

### 8.3.5.5 Battery Protection

#### 8.3.5.5.1 Battery Overcurrent Protection (BATOVP)

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charge. The fault register REG09[5] goes high and an INT is asserted to the host.

#### 8.3.5.5.2 Charging During Battery Short Protection

If the battery voltage falls below 2V, the charge current is reduced to 100mA for battery safety.

#### 8.3.5.5.3 System Overcurrent Protection

If the system is shorted or exceeds the overcurrent limit, the BATFET is latched off. DC source insertion on VBUS is required to reset the latch-off condition and turn on BATFET.

### 8.3.6 Serial Interface

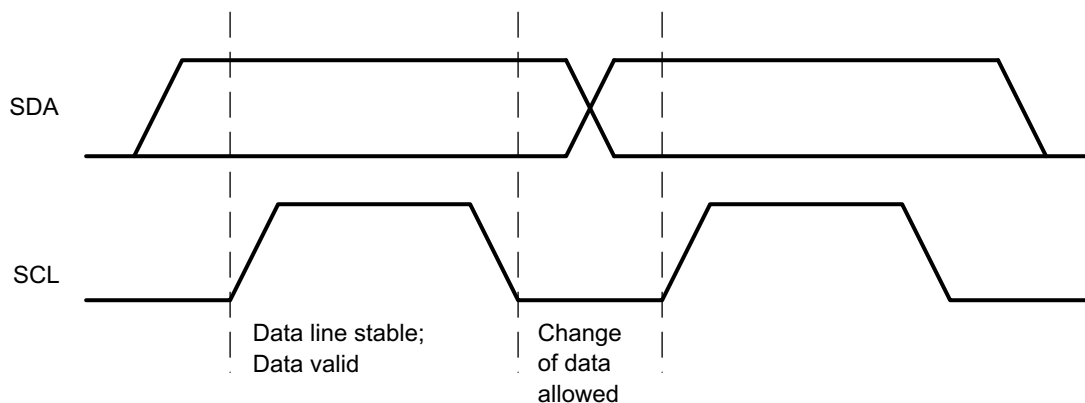
The device uses I<sup>2</sup>C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I<sup>2</sup>C™ is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH, receiving control inputs from the master device like micro controller or a digital signal processor. The I<sup>2</sup>C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits).

Both SDA and SCL are bi-directional lines, connecting to the positive supply voltage via a current source or pullup resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

#### 8.3.6.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

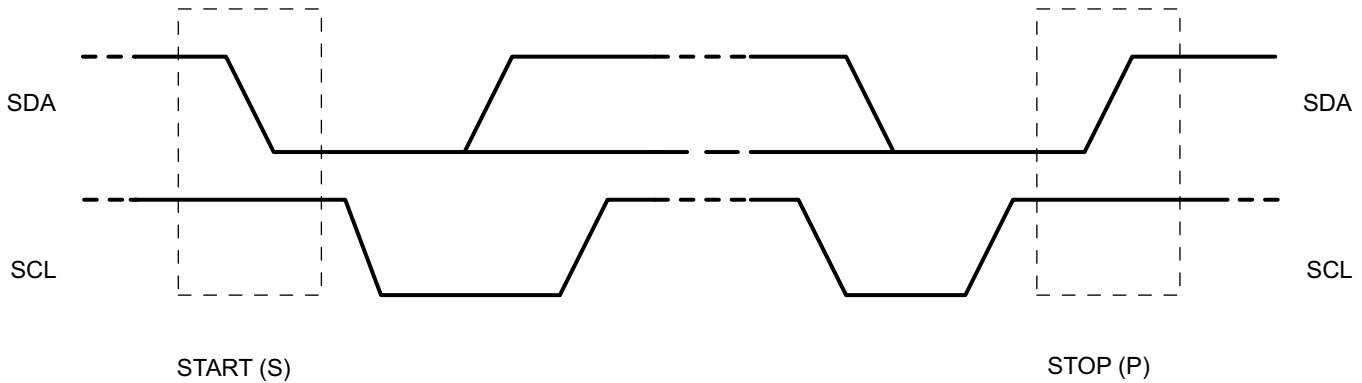


**图 16. Bit Transfer on the I<sup>2</sup>C Bus**

#### 8.3.6.2 START and STOP Conditions

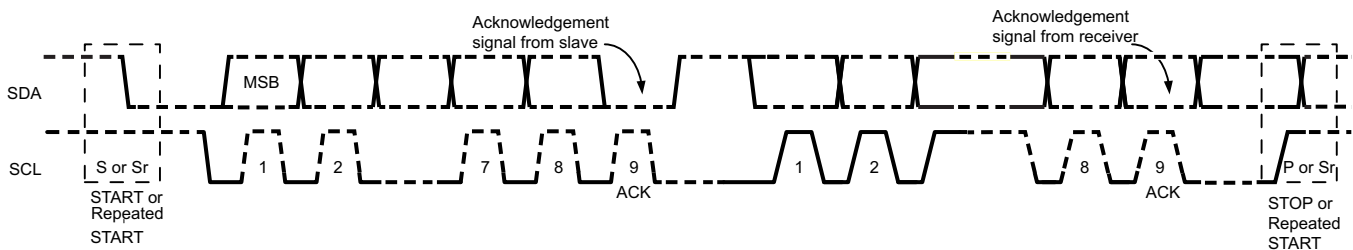
All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.


**图 17. START and STOP conditions**

### 8.3.6.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.


**图 18. Data Transfer on the I<sup>2</sup>C Bus**

### 8.3.6.4 Acknowledge (ACK) and Not Acknowledge (NACK)

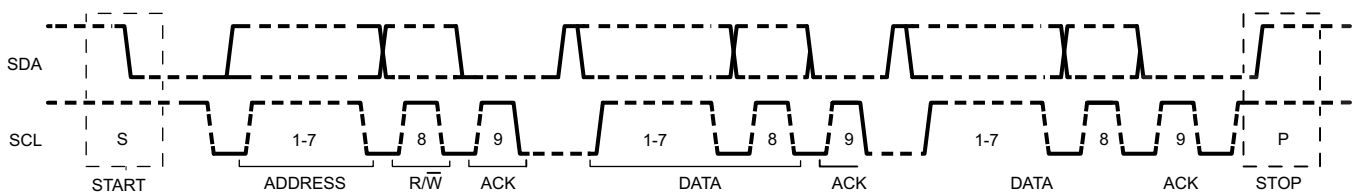
The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9<sup>th</sup> clock pulse, are generated by the master.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

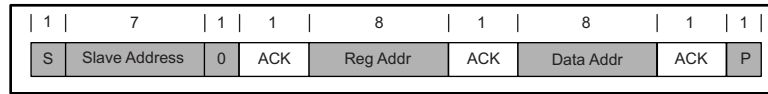
### 8.3.6.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

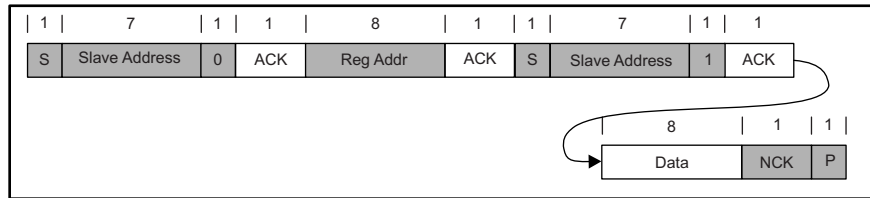

**图 19. Complete Data Transfer**



### 8.3.6.5.1 Single Read and Write



**图 20. Single Write**

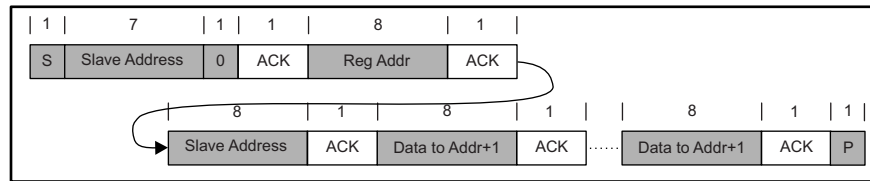


**图 21. Single Read**

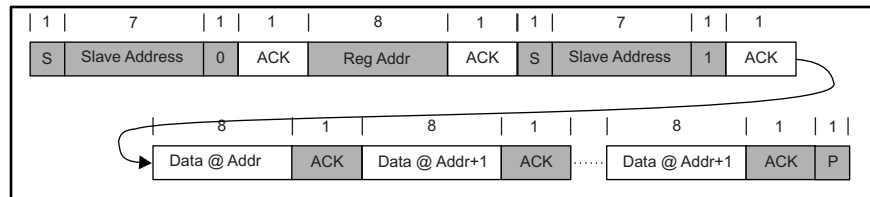
If the register address is not defined, the charger IC send back NACK and go back to the idle state.

### 8.3.6.5.2 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG08.



**图 22. Multi-Write**



**图 23. Multi-Read**

The fault register REG09 locks the previous fault and only clears it after the register is read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. To verify real time fault, the fault register REG09 should be read twice to get the real condition. In addition, the fault register REG09 does not support multi-read or multi-write.

## 8.4 Device Functional Modes

### 8.4.1 Host Mode and Default Mode

The device is a host controlled device, but it can operate in default mode without host management. In default mode, device can be used as an autonomous charger with no host or with host in sleep.

When the charger is in default mode, REG09[7] is HIGH. When the charger is in host mode, REG09[7] is LOW. After power-on-reset, the device starts in watchdog timer expiration state, or default mode. All the registers are in the default settings.

## Device Functional Modes (接下页)

Any write command to the device transitions the device from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to REG01[6] before the watchdog timer expires (REG05[5:4]), or disable watchdog timer by setting REG05[5:4]=00.

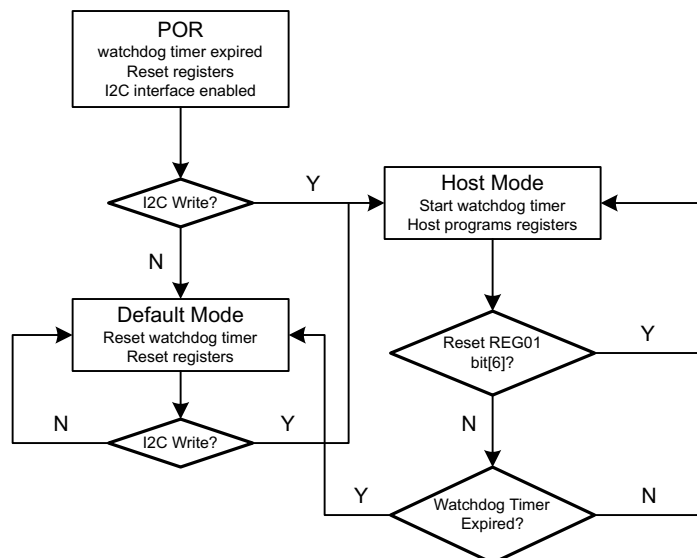


图 24. Watchdog Timer Flow Chart

### 8.4.1.1 Plug in USB 100mA Source with Good Battery

When the input source is detected as 100mA USB host, and the battery voltage is above batgood threshold ( $V_{BATGD}$ ), the charger device enters HIZ state to meet the battery charging spec requirement.

If the charger device is in host mode, it will stay in HIZ state even after the USB100mA source is removed, and the adapter plugs in. During the HIZ state, REG00[7] is set HIGH and the system load is supplied from battery. It is recommended that the processor host always checks if the charger IC is in HIZ state when it wakes up. The host can write REG00[7] to 0 to exit HIZ state.

If the charger is in default mode, when the DC source is removed, the charger device will get out of HIZ state automatically. When the input source plugs in again, the charger IC runs detection on the input source and update the input current limit.

### 8.4.1.2 USB Timer when Charging from USB100mA Source

The total charging time in default mode from USB100mA source is limited by a 45-min max timer. At the end of the timer, the device stops the converter and goes to HIZ.

## 8.5 Register Map

**表 6. Register Map**

REGISTER	REGISTER NAME	RESET
REG00	Input Source Control Register	00111101, or 3D
REG01	Power-On Configuration Register	00011011, or 1B
REG02	Charge Current Control Register	00100000, or 20
REG03	Pre-Charge/Termination Current Control Register	00010001, or 11
REG04	Charge Voltage Control Register	10011010, or 9A
REG05	Charge Termination/Timer Control Register	10011010, or 9A
REG06	IR Compensation / Thermal Regulation Control Register	00000011, or 03
REG07	Misc Operation Control Register	01001011, or 4B
REG08	System Status Register	—
REG09	Fault Register	—
REG0A	Vender / Part / Revision Status Register	—

## 8.5.1 I<sup>2</sup>C Registers

Address: 6BH. REG00-07 support Read and Write. REG08-0A are read only.

### 8.5.1.1 Input Source Control Register REG00 (reset = 00111000, or 3D)

**图 25. REG00 Input Source Control Register Format**

7	6	5	4	3	2	1	0
EN_HIZ	VINDPM[3]	VINDPM[2]	VINDPM[1]	VINDPM[0]	IINLIM[2]	IINLIM[1]	IINLIM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 7. REG00 Input Source Control Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION	
Bit 7	EN_HIZ	R/W	0	0 – Disable, 1 – Enable	Default: Disable (0)
INPUT VOLTAGE LIMIT					
Bit 6	VINDPM[3]	R/W	0	640mV	Offset 3.88V, Range: 3.88V-5.08V Default: 4.44V (0111)
Bit 5	VINDPM[2]	R/W	1	320mV	
Bit 4	VINDPM[1]	R/W	1	160mV	
Bit 3	VINDPM[0]	R/W	1	80mV	
INPUT CURRENT LIMIT (ACTUAL INPUT CURRENT LIMIT IS THE LOWER OF I <sup>2</sup> C AND ILIM)					
Bit 2	IINLIM[2]	R/W	1	000 – 100mA, 001 – 150mA, 010 – 500mA,	Default SDP: 100mA (000)(OTG pin=0) or 500mA (010) (OTG pin=1) Default DCP/CDP: 1.5A (101)
Bit 1	IINLIM[1]	R/W	0	011 – 900mA, 100 – 1.2A, 101 – 1.5A,	
Bit 0	IINLIM[0]	R/W	1	110 – 2A, 111 – 3A	

### 8.5.1.2 Power-On Configuration Register REG01 (reset = 00011011, or 1B)

**图 26. REG01 Power-On Configuration Register Format**

7	6	5	4	3	2	1	0
Register Reset	I <sup>2</sup> C Watchdog Timer Reset	CHG_CONFIG[1]	CHG_CONFIG[0]	SYS_MIN[2]	SYS_MIN[1]	SYS_MIN[0]	BOOST_LIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 8. REG01 Power-On Configuration Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Bit 7	Register Reset	R/W	0	0 – Keep current register setting, 1 – Reset to default	Default: Keep current register setting (0) Back to 0 after register reset
Bit 6	I <sup>2</sup> C Watchdog Timer Reset	R/W	0	0 – Normal ; 1 – Reset	Default: Normal (0) Back to 0 after timer reset
CHARGER CONFIGURATION					
Bit 5	CHG_CONFIG[1]	R/W	0	00 – Charge Disable, 01 – Charge Battery, 10/11 – OTG	Default: Charge Battery (01)
Bit 4	CHG_CONFIG[0]	R/W	1		
MINIMUM SYSTEM VOLTAGE LIMIT					
Bit 3	SYS_MIN[2]	R/W	1	0.4V	Offset: 3.0V, Range 3.0V-3.7V Default: 3.5V (101)
Bit 2	SYS_MIN[1]	R/W	0	0.2V	
Bit 1	SYS_MIN[0]	R/W	1	0.1V	
BOOST MODE CURRENT LIMIT					
Bit 0	BOOST_LIM	R/W	1	0 – 500mA, 1 – 1.3A	Default: 1.3A (1)

### 8.5.1.3 Charge Current Control Register REG02 (reset = 00100000, or 20)

**图 27. REG02 Charge Current Control Register Format**

7	6	5	4	3	2	1	0
ICHG[5]	ICHG[4]	ICHG[3]	ICHG[2]	ICHG[1]	ICHG[0]	Reserved	FORCE_20PCT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 9. REG02 Charge Current Control Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
<b>FAST CHARGE CURRENT LIMIT</b>					
Bit 7	ICHG[5]	R/W	0	2048mA	Offset: 512mA Range: 512-4544mA Default: 1024mA (001000)
Bit 6	ICHG[4]	R/W	0	1024mA	
Bit 5	ICHG[3]	R/W	1	512mA	
Bit 4	ICHG[2]	R/W	0	256mA	
Bit 3	ICHG[1]	R/W	0	128mA	
Bit 2	ICHG[0]	R/W	0	64mA	
Bit 1	Reserved	R/W	0	0 - Reserved	
Bit 0	FORCE_20PCT	R/W	0	0 – ICHG as REG02[7:2] (Fast Charge Current Limit) and REG03[7:4] (Pre-Charge Current Limit) programmed 1 – ICHG as 20% of REG02[7:2] (Fast Charge Current Limit) and 50% of REG03[7:4] (Pre-Charge Current Limit) programmed	Default: (0) ICHG as 20% of REG02[7:2] (Fast Charge Current Limit) and 50% of REG03[7:4] (Pre-Charge Current Limit) programmed

### 8.5.1.4 Pre-Charge/Termination Current Control Register REG 03 (reset = 00010001, or 11)

**图 28. REG03 Pre-Charge/Termination Current Control Register Format**

7	6	5	4	3	2	1	0
IPRECHG[3]	IPRECHG[2]	IPRECHG[1]	IPRECHG[0]	ITERM[3]	ITERM[2]	ITERM[1]	ITERM[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 10. REG03 Pre-Charge/Termination Current Control Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
PRE-CHARGE CURRENT LIMIT					
Bit 7	IPRECHG[3]	R/W	0	1024mA	Offset: 128mA, Range: 128mA – 640mA Default: 256mA (0001)
Bit 6	IPRECHG[2]	R/W	0	512mA	
Bit 5	IPRECHG[1]	R/W	0	256mA	
Bit 4	IPRECHG[0]	R/W	1	128mA	
TERMINATION CURRENT LIMIT					
Bit 3	ITERM[3]	R/W	0	1024mA	Offset: 128mA Range: 128mA – 2048mA Default: 256mA (0001)
Bit 2	ITERM[2]	R/W	0	512mA	
Bit 1	ITERM[1]	R/W	0	256mA	
Bit 0	ITERM[0]	R/W	1	128mA	

### 8.5.1.5 Charge Voltage Control Register REG04 (reset = 10011010, or 9A)

**图 29. REG04 Charge Voltage Control Register Format**

7	6	5	4	3	2	1	0
VREG[5]	VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	BATLOWV	VRECHG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 11. REG04 Charge Voltage Control Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
CHARGE VOLTAGE LIMIT					
Bit 7	VREG[5]	R/W	1	512mV	Offset: 3.504V Range: 3.504V – 4.400V (111000) Default: 4.112V (100110)
Bit 6	VREG[4]	R/W	0	256mV	
Bit 5	VREG[3]	R/W	0	128mV	
Bit 4	VREG[2]	R/W	1	64mV	
Bit 3	VREG[1]	R/W	1	32mV	
Bit 2	VREG[0]	R/W	0	16mV	
BATTERY PRECHARGE TO FAST CHARGE THRESHOLD					
Bit 1	BATLOWV	R/W	1	0 – 2.8V, 1 – 3.0V	Default: 3.0V (1)
BATTERY RECHARGE THRESHOLD (BELOW BATTERY REGULATION VOLTAGE)					
Bit 0	VRECHG	R/W	0	0 – 100mV, 1 – 300mV	Default: 100mV (0)

### 8.5.1.6 Charge Termination/Timer Control Register REG05 (reset = 10011010, or 9A)

**图 30. REG05 Charge Termination/Timer Control Register Format**

7	6	5	4	3	2	1	0
EN_TERM	TERM_STAT	WATCHDOG[1]	WATCHDOG[0]	EN_TIMER	CHG_TIMER[1]	CHG_TIMER[0]	Reserved
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 12. REG05 Charge Termination/Timer Control Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
CHARGING TERMINATION ENABLE					
Bit 7	EN_TERM	R/W	1	0 – Disable, 1 – Enable	Default: Enable termination (1)
TERMINATION INDICATOR THRESHOLD					
Bit 6	TERM_STAT	R/W	0	0 – Match ITERM, 1 – STAT pin high before actual termination when charge current below 800 mA	Default Match ITERM (0)
I2C WATCHDOG TIMER SETTING					
Bit 5	WATCHDOG[1]	R/W	0	00 – Disable timer, 01 – 40s, 10 – 80s, 11 – 160s	Default: 40s (01)
Bit 4	WATCHDOG[0]	R/W	1		
CHARGING SAFETY TIMER ENABLE					
Bit 3	EN_TIMER	R/W	1	0 – Disable, 1 – Enable	Default: Enable (1)
FAST CHARGE TIMER SETTING					
Bit 2	CHG_TIMER[1]	R/W	0	00 – 5 hrs, 01 – 8 hrs, 10 – 12 hrs, 11 – 20 hrs	Default: 8hours (01) (See Charging Safety Timer for details)
Bit 1	CHG_TIMER[0]	R/W	1		
Bit 0	Reserved	R/W	0	0 - Reserved	

### 8.5.1.7 IR Compensation / Thermal Regulation Control Register REG06 (reset = 00000011, or 03)

**图 31. REG06 IR Compensation / Thermal Regulation Control Register Format**

7	6	5	4	3	2	1	0
BAT_COMP[2]	BAT_COMP[1]	BAT_COMP[0]	VCLAMP[2]	VCLAMP[1]	VCLAMP[0]	TREG[1]	TREG[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 13. REG06 IR Compensation / Thermal Regulation Control Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
IR COMPENSATION RESISTOR SETTING					
Bit 7	BAT_COMP[2]	R/W	0	40mΩ	Range: 0 – 70mΩ Default: 0Ω (000)
Bit 6	BAT_COMP[1]	R/W	0	20mΩ	
Bit 5	BAT_COMP[0]	R/W	0	10mΩ	
IR COMPENSATION VOLTAGE CLAMP (ABOVE REGULATION VOLTAGE)					
Bit 4	VCLAMP[2]	R/W	0	64mV	Range: 0 – 112 mV Default: 0mV (000)
Bit 3	VCLAMP[1]	R/W	0	32mV	
Bit 2	VCLAMP[0]	R/W	0	16mV	
THERMAL REGULATION THRESHOLD					
Bit 1	TREG[1]	R/W	1	00 – 60°C, 01 – 80°C, 10 – 100°C, 11 – 120°C	Default: 120°C (11)
Bit 0	TREG[0]	R/W	1		

### 8.5.1.8 Misc Operation Control Register REG07 (reset = 01001011, or 4B)

**图 32. REG07 Misc Operation Control Register Format**

7	6	5	4	3	2	1	0
DPDM_EN	TMR2X_EN	BATFET_Disable	Reserved	Reserved	Reserved	INT_MASK[1]	INT_MASK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**表 14. REG07 Misc Operation Control Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION	NOTE
Set default input current limit from PSEL/OTG pins					
Bit 7	DPDM_EN	R/W	0	0 – Not in Input source detection; 1 – Force Input source detection	Default: Not in Input source detection (0). Reset to 0 after detection complete. INT pulse may not be generated
<b>SAFETY TIMER SETTING DURING INPUT DPM AND THERMAL REGULATION</b>					
Bit 6	TMR2X_EN	R/W	1	0 – Safety timer not slowed by 2X during input DPM or thermal regulation, 1 – Safety timer slowed by 2X during input DPM or thermal regulation	Default: Safety timer slowed by 2X (1)
<b>FORCE BATFET OFF</b>					
Bit 5	BATFET_Disable	R/W	0	0 – Allow Q4 turn on, 1 – Turn off Q4	Default: Allow Q4 turn on(0)
Bit 4	Reserved	R/W	0	0 - Reserved	
Bit 3	Reserved	R/W	1	1 - Reserved	
Bit 2	Reserved	R/W	0	0 - Reserved	
Bit 1	INT_MASK[1]	R/W	1	0 – No INT during CHRG_FAULT, 1 – INT on CHRG_FAULT	Default: INT on CHRG_FAULT (1)
Bit 0	INT_MASK[0]	R/W	1	0 – No INT during BAT_FAULT, 1 – INT on BAT_FAULT	Default: INT on BAT_FAULT (1)

### 8.5.1.9 System Status Register REG08

**图 33. REG08 System Status Register Format**

7	6	5	4	3	2	1	0
VBUS_STAT[1]	VBUS_STAT[0]	CHRG_STAT[1]	CHRG_STAT[0]	DPM_STAT	PG_STAT	THERM_STAT	VSYS_STAT
R	R	R	R	R	R	R	R

LEGEND: R = Read only; -n = value after reset

**表 15. REG08 System Status Register Description**

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	VBUS_STAT[1]	R	00 – Unknown (no input, or DPDM detection incomplete), 01 – USB host, 10 – Adapter port, 11 – OTG
Bit 6	VBUS_STAT[0]	R	
Bit 5	CHRG_STAT[1]	R	00 – Not Charging, 01 – Pre-charge ( $<V_{BATLOWV}$ ), 10 – Fast Charging, 11 – Charge Termination Done
Bit 4	CHRG_STAT[0]	R	
Bit 3	DPM_STAT	R	0 – Not DPM, 1 – VINDPM or IINDPM
Bit 2	PG_STAT	R	0 – Not Power Good, 1 – Power Good
Bit 1	THERM_STAT	R	0 – Normal, 1 – In Thermal Regulation
Bit 0	VSYS_STAT	R	0 – Not in VSYSMIN regulation ( $BAT > VSYSMIN$ ), 1 – In VSYSMIN regulation ( $BAT < VSYSMIN$ )

### 8.5.1.10 Fault Register REG09

**图 34. REG09 Fault Register Format**

7	6	5	4	3	2	1	0
WATCHDOG_FAULT	BOOST_FAULT	CHRG_FAULT[1]	CHRG_FAULT[0]	BAT_FAULT	NTC_FAULT[2]	NTC_FAULT[1]	NTC_FAULT[0]
R	R	R	R	R	R	R	R

LEGEND: R = Read only; -n = value after reset

**表 16. REG09 Fault Register Description**

BIT	FIELD	TYPE	DESCRIPTION
Bit 7	WATCHDOG_FAULT	R	0 – Normal, 1- Watchdog timer expiration
Bit 6	BOOST_FAULT	R	0 – Normal, 1 – VBUS overloaded (OCP), or VBUS OVP in boost mode
Bit 5	CHRG_FAULT[1]	R	00 – Normal, 01 – Input fault (VBUS OVP or $VBAT < VBUS < 3.8V$ ), 10 - Thermal shutdown, 11 – Charge Safety Timer Expiration Note: a one time Input fault is generated when VBUS source is removed
Bit 4	CHRG_FAULT[0]	R	
Bit 3	BAT_FAULT	R	0 – Normal, 1 – BATOVP
Bit 2	NTC_FAULT[2]	R	000 – Normal, 001 – TS1 Cold, 010 – TS1 Hot, 011 – TS2 Cold, 100 – TS2 Hot, 101 – Both Cold, 110 – Both Hot
Bit 1	NTC_FAULT[1]	R	
Bit 0	NTC_FAULT[0]	R	



### 8.5.1.11 Vender / Part / Revision Status Register REG0A

**图 35. REG0A Vender / Part / Revision Status Register Format**

7	6	5	4	3	2	1	0
Reserved	Reserved	PN[2]	PN[1]	PN[0]	TS_PROFILE	DEV_REG[0]	DEV_REG[1]
R	R	R	R	R	R	R	R

LEGEND: R = Read only; -n = value after reset

**表 17. REG0A Vender / Part / Revision Status Register Description**

BIT	FIELD	TYPE	RESET	DESCRIPTION
Bit 7	Reserved	R	0	0 - Reserved
Bit 6	Reserved	R	0	0 - Reserved
<b>DEVICE CONFIGURATION</b>				
Bit 5	PN[2]	R	0	011
Bit 4	PN[1]	R	1	
Bit 3	PN[0]	R	1	
Bit 2	TS_PROFILE	R	0	0 – Cold/Hot window
Bit 1	DEV_REG[0]	R	0	00
Bit 0	DEV_REG[1]	R	0	

## 9 Application and Implementation

### 注

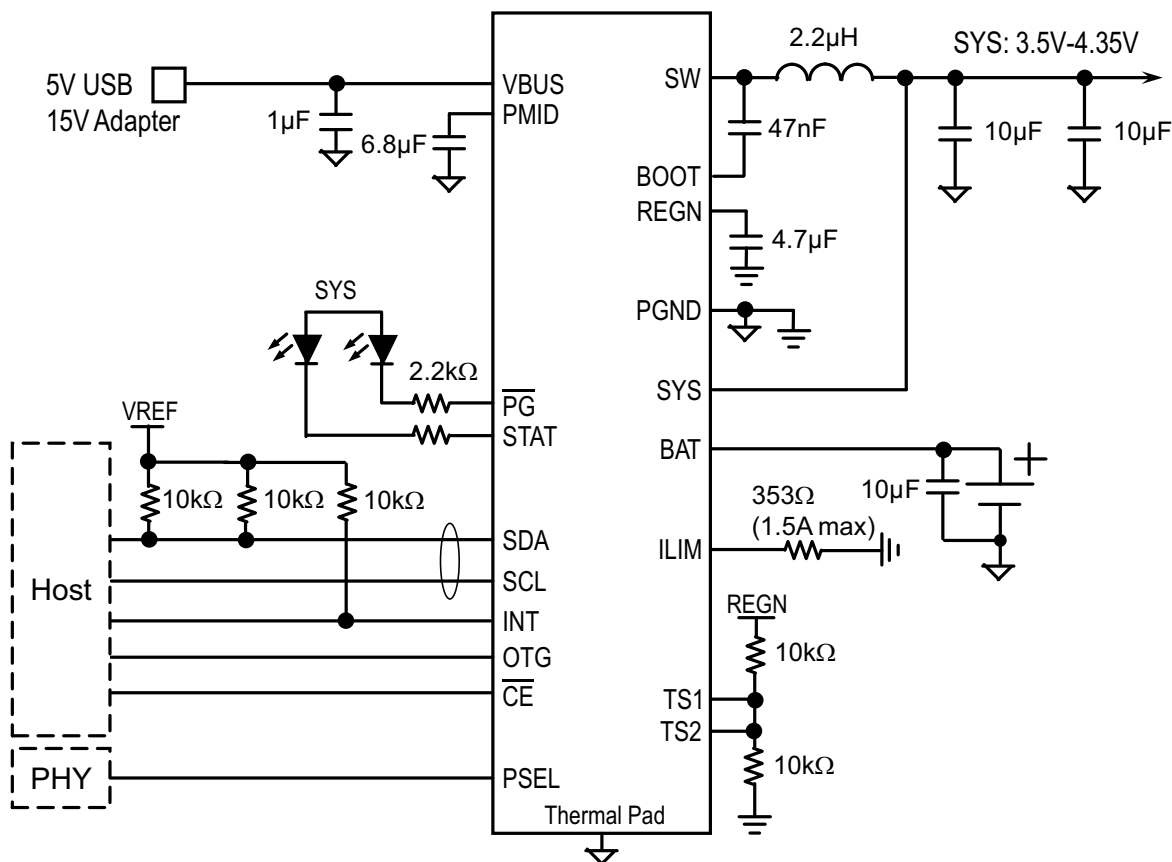
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

A typical application consists of the device configured as an I<sup>2</sup>C controlled power path management device and a single cell Li-Ion battery charger for single cell Li-Ion and Li-polymer batteries used in a wide range of tablets and other portable devices. It integrates an input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and BATFET (Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

### 9.2 Typical Application

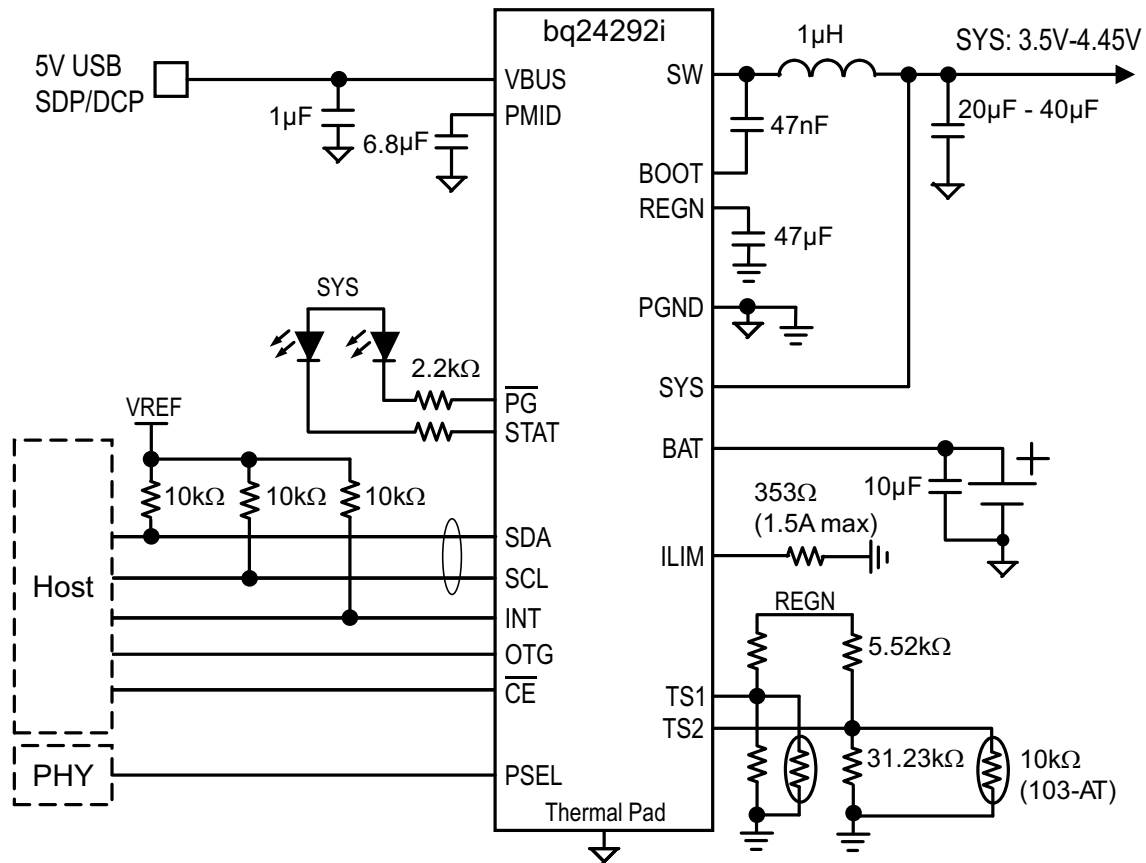
Typical applications are shown in 图 36 and 图 37.



VREF is the pull up voltage of I2C communication interface.

图 36. bq24292i with PSEL, USB On-The-Go (OTG), No Thermistor Connections

## Typical Application (接下页)



VREF is the pull up voltage of I2C communication interface.

图 37. bq24292i with PSEL, Charging from 5V USB, and Two Thermistor Connections

### 9.2.1 Design Requirements

The design parameters are listed in the following table.

表 18. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.9 V - 17 V
Input current limit	3A
Fast charge current	4A
Boost mode output current	1.3A

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Inductor Selection

The device has 1.5 MHz switching frequency to allow the use of small inductor and capacitor values. The Inductor saturation current should be higher than the charging current ( $I_{CHG}$ ) plus half the ripple current ( $I_{RIPPLE}$ ):

$$I_{SAT} \geq I_{CHG} + (1/2) I_{RIPPLE} \quad (5)$$

The inductor ripple current depends on input voltage (VBUS), duty cycle ( $D = V_{BAT}/V_{VBUS}$ ), switching frequency (fs) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1-D)}{f_s \times L} \quad (6)$$

The maximum inductor ripple current happens with  $D = 0.5$  or close to 0.5. Usually inductor ripple is designed in the range of (20–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design. Typical inductor value is 2.2μH.

### 9.2.2.2 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current  $I_{CIN}$  occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (7)$$

For best performance, VBUS should be decouple to PGND with 1μF capacitance. The remaining input capacitor should be place on PMID.

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high side MOSFET and source of the low side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. 25V rating or higher capacitor is preferred for 15V input voltage.

### 9.2.2.3 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current  $I_{COUT}$  is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (8)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCf_s^2} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (9)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The charger device has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15 kHz and 36 kHz. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.

## 9.2.3 Application Performance Curves

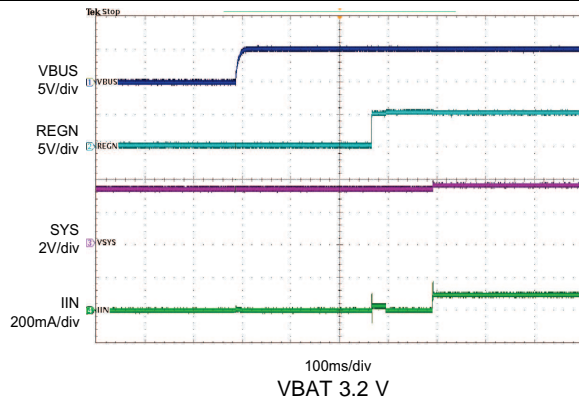


图 38. Power Up from USB100mA

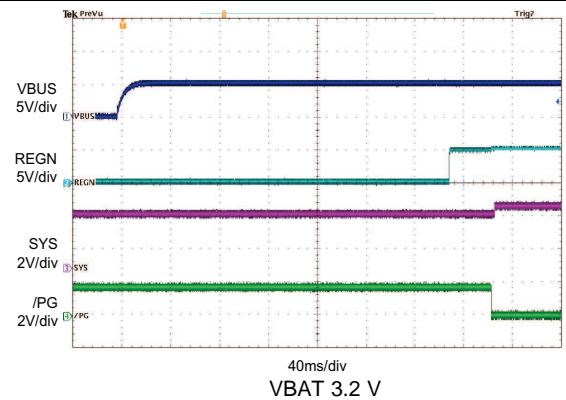


图 39. Power Up with Charge Disabled

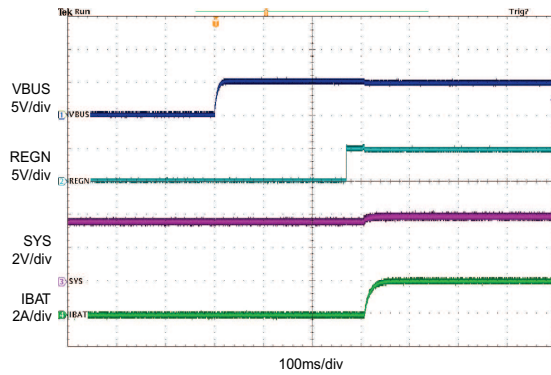


图 40. Power Up with Charge Enabled

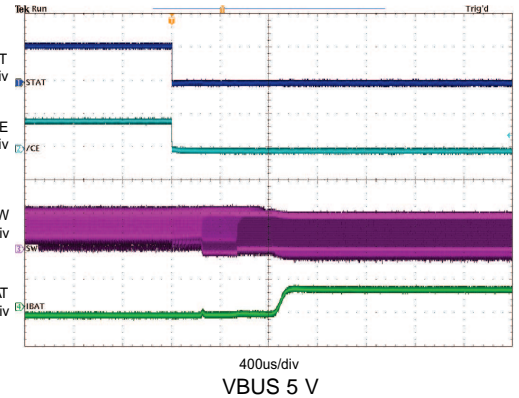


图 41. Charge Enable

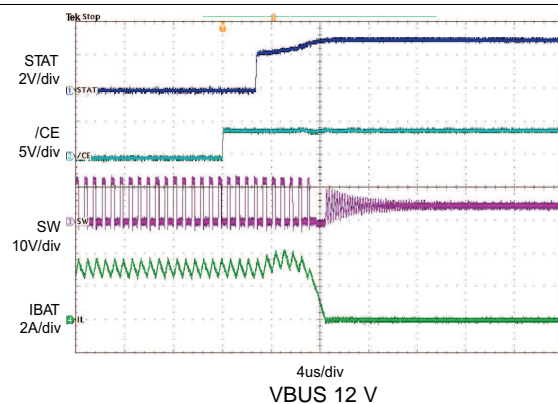


图 42. Charge Disable

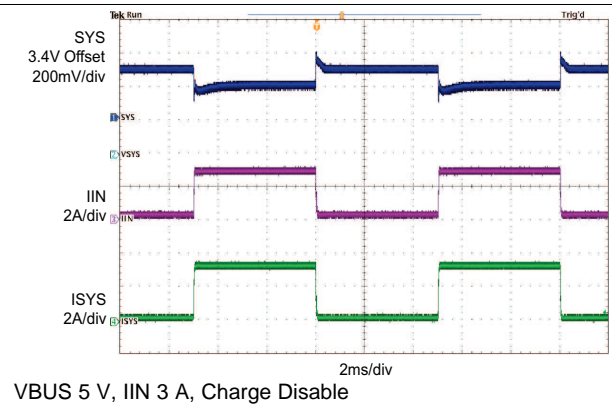


图 43. Input Current DPM Response without Battery

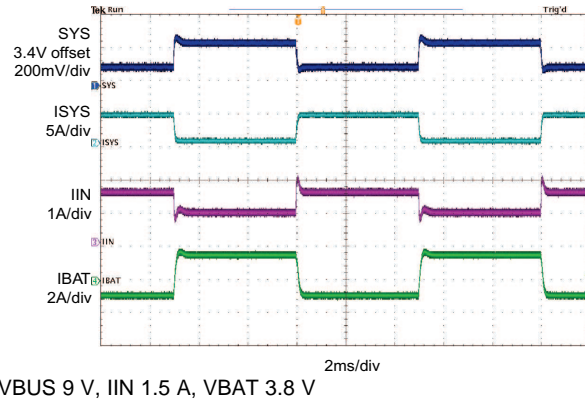


图 44. Load Transient during Supplement Mode

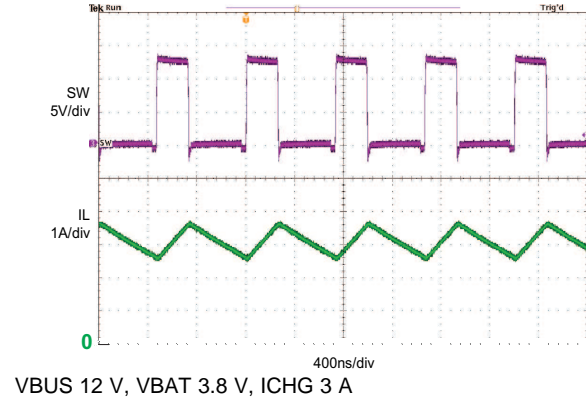


图 45. PWM Switching Waveform

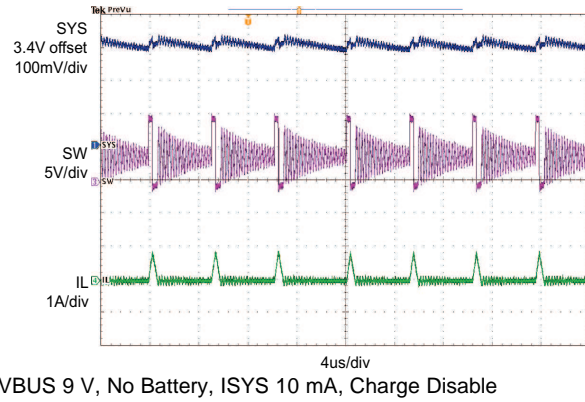


图 46. PFM Switching Waveform

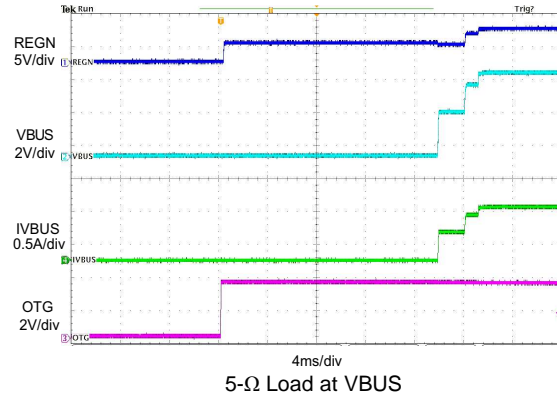


图 47. Boost Mode Enable

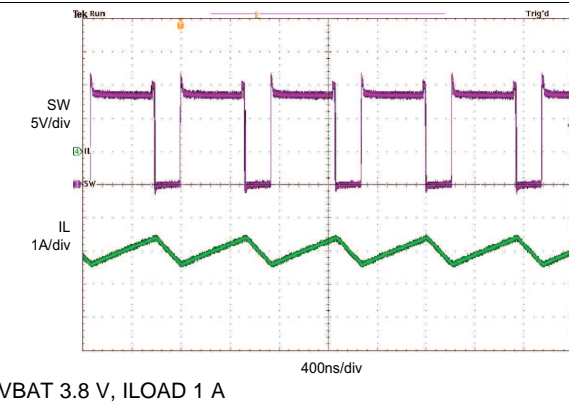


图 48. Boost Mode Switching Waveform

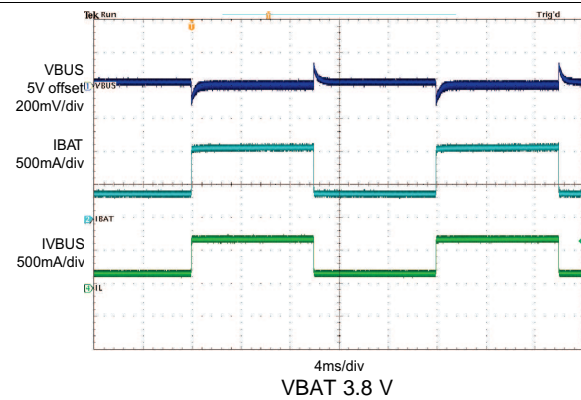
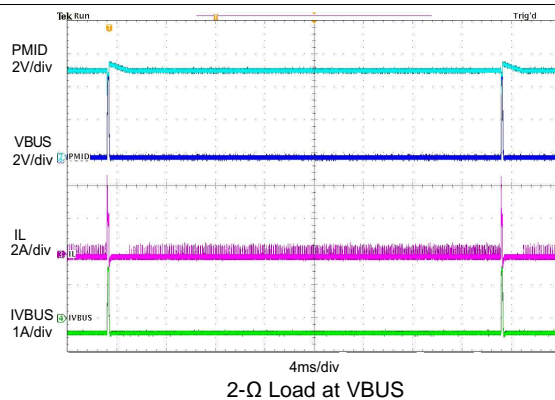


图 49. Boost Mode Load Transient



**图 50. Boost Mode Hiccup Mode Overcurrent Protection**

## 10 Power Supply Recommendations

To provide an output voltage on SYS, the bq24292i requires a power supply between 3.9 V and 17 V input with at least 100-mA current rating connected to VBUS; or, a single-cell Li-Ion battery with voltage > VBATUVLO connected to BAT. The source current rating needs to be at least 3 A for the buck converter of the charger to provide maximum output power to SYS.

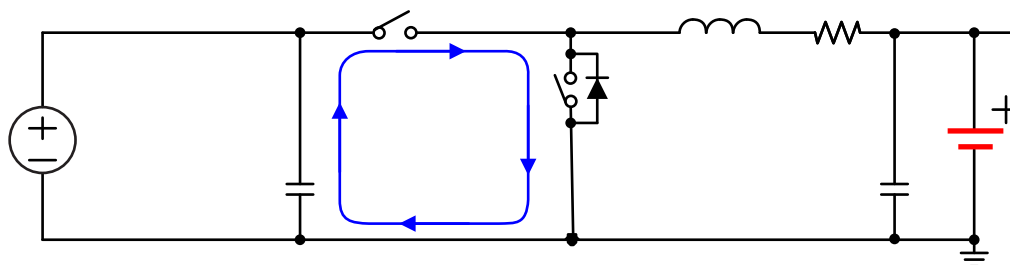
## 11 Layout

### 11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see [图 51](#)) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane.
2. Place inductor input terminal to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the IC. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using power pad as the single ground connection point. Or using a 0Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the IC. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Decoupling capacitors should be placed next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. The via size and number should be enough for a given current path.

See the EVM design for the recommended component placement with trace and via locations. For the QFN information, refer to [SCBA017](#) and [SLUA271](#).



**图 51. High Frequency Current Path**



## 11.2 Layout Example

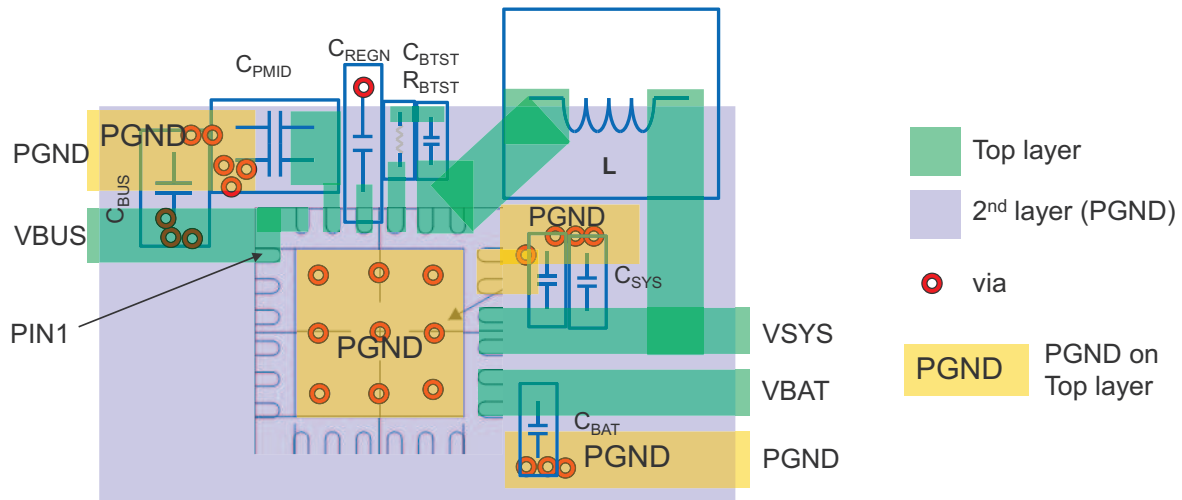


图 52. Layout Example Diagram

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

相关文档如下：

- 《bq24292i EVM (PWR021) 用户指南》(SLUUA14C)
- 《四方扁平无引线逻辑封装应用报告》(SCBA017)
- 《QFN/SON PCB 连接应用报告》(SLUA271)

### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。请单击右上角的通知我 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

### 12.3 社区资源

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24292IRGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24292I	<a href="#">Samples</a>
BQ24292IRGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24292I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24292IRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24292IRGER	VQFN	RGE	24	3000	330.0	12.4	4.35	4.35	1.1	8.0	12.0	Q2
BQ24292IRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24292IRGET	VQFN	RGE	24	250	180.0	12.5	4.35	4.35	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24292IRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24292IRGER	VQFN	RGE	24	3000	338.0	355.0	50.0
BQ24292IRGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24292IRGET	VQFN	RGE	24	250	338.0	355.0	50.0

**RGE 24**

**GENERIC PACKAGE VIEW**

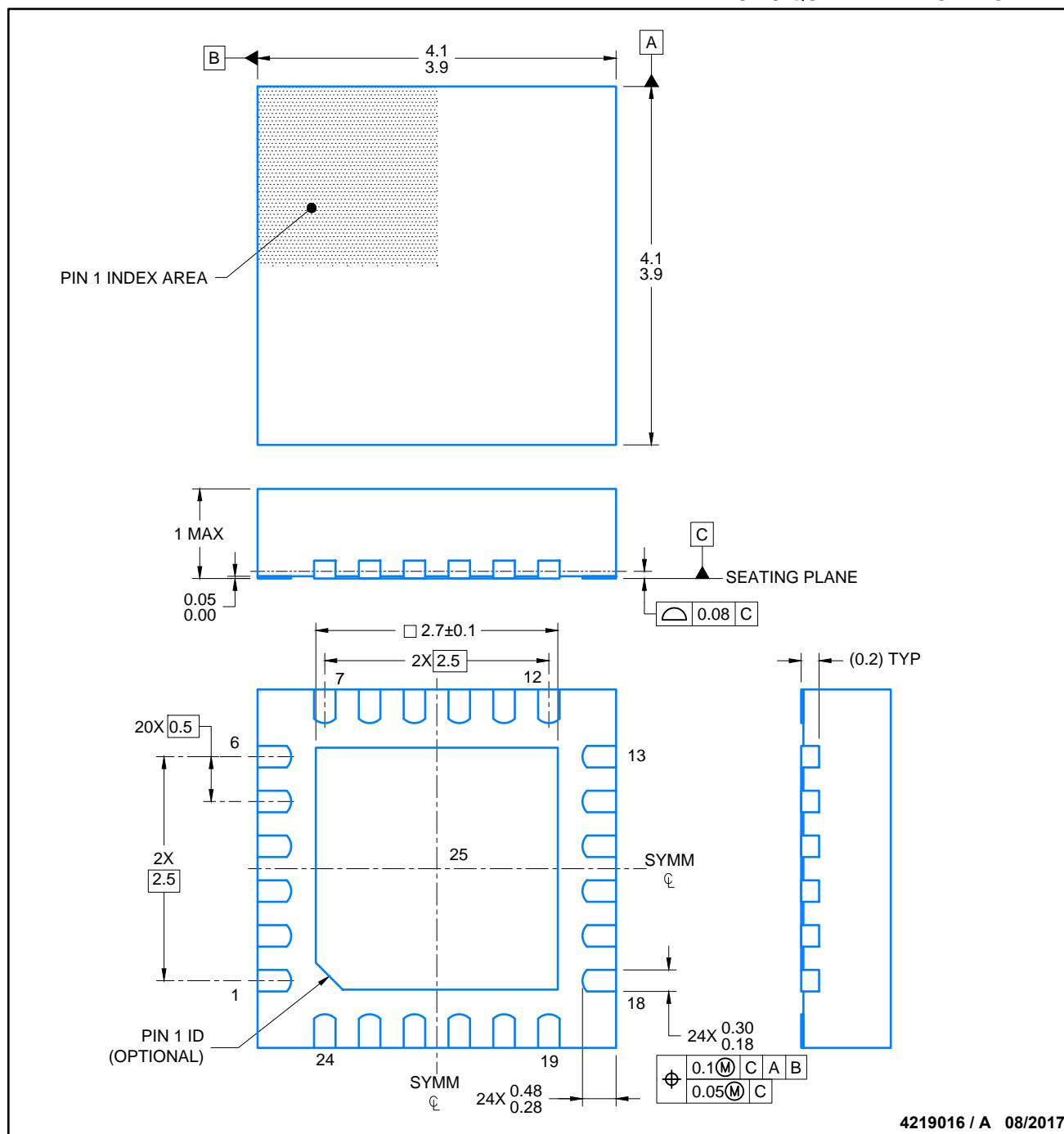
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



**VQFN - 1 mm max height**

24X (0.58)

24X (0.24)

20X (0.5)

SYMM

(Ø0.2) VIA TYP

(R0.05)

24

19

18

13

7

12

25

2X(1.1)

SYMM

(3.825)

(3.825)

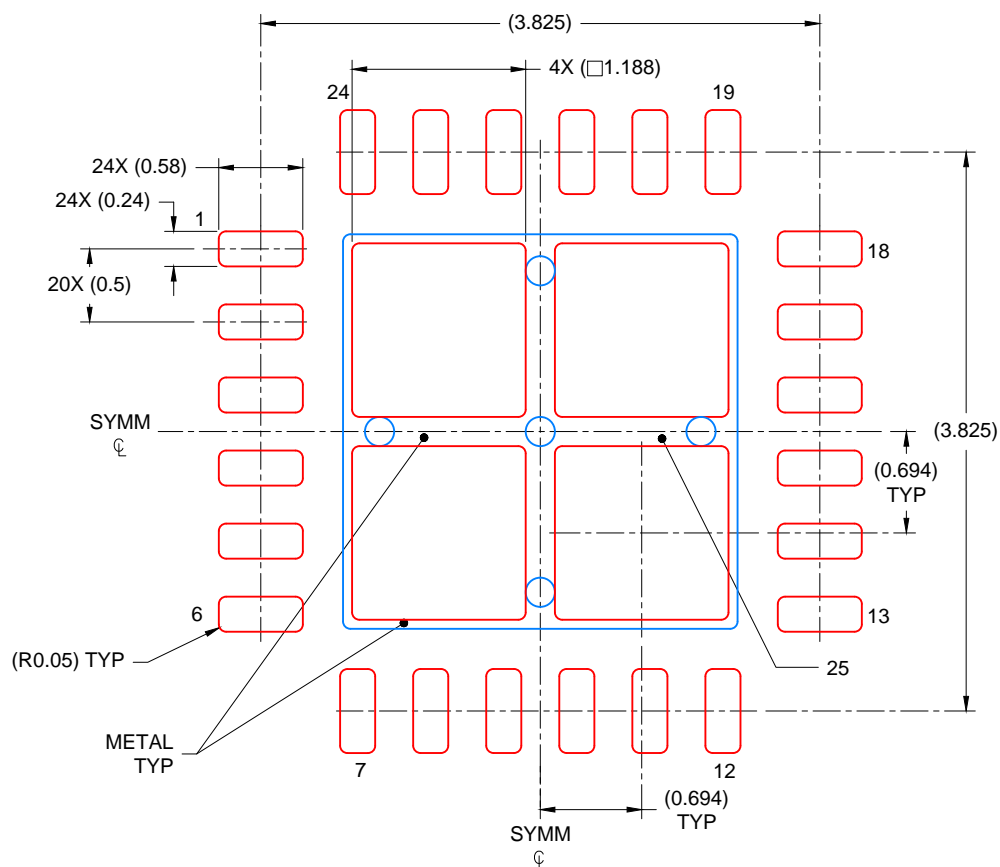
(2.7)

The diagram illustrates two types of solder mask openings on a metal pad:

- NON SOLDER MASK DEFINED (PREFERRED):** This type shows a metal pad with a solder mask opening. The opening is defined by the metal itself, and the solder mask is applied all around it. The dimension is labeled as 0.07 MAX ALL AROUND.
- SOLDER MASK DEFINED:** This type shows a metal pad with a solder mask opening. The opening is defined by the solder mask, and the metal is applied all around it. The dimension is labeled as 0.07 MIN ALL AROUND.

**SOLDER MASK DETAILS**

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
78% PRINTED COVERAGE BY AREA  
SCALE: 20X

4219016 / A 08/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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