CDCL1810A 1.8V、10 输出高性能时钟分配器

1 特性

- 1.8V 单电源
- 具有 10 输出的高性能时钟分配器
- 低输入输出附加抖动：低至 10fs 均方根 (RMS)
- 低压差分信令 (LVDS) 输入，100Ω 差分片上端接，频率高达 650MHz
- 差分电流模式逻辑 (CML) 输出、50Ω 单端片上端接、频率高达 650MHz
- 两组输出，每组有 5 个且均具有独立的频分比
- 输出频率可采用 1、2、4、5、8、10、16、20、32、40 和 80 频分比
- 符合 ANSI TIA/EIA-644-A-2001 LVDS 标准要求
- 功耗：410mW（典型值）
- 针对每个输出的输出使能控制
- 串行数据/串行时钟 (SDA/SCL) 器件管理接口
- 48 引脚超薄四方扁平无引线 (VQFN) (RGZ) 封装
- 工业温度范围：-40°C 至 +85°C

2 应用

- 针对高速串行解串器 (SERDES) 的时钟分配
- 针对 1G/10G 以太网、1X/2X/4X/10X 光纤通道、PCI Express、串行 ATA、同步光纤网 (SONET)、通用公共无线接口 (CPRI) 和开放式基站架构联盟 (OBSAI) 等的 SERDES 基准时钟分配
- 多达 1 到 10 的时钟缓冲和扇出

3 说明

CDCL1810A 是一款高性能时钟分配器。 可编程分频器（P0 和 P1）为输出输入频率比的设置提供了较高的灵活性：$F_{OUT} = F_{IN}/P$，其中 P（P0 或 P1）= 1、2、4、5、8、10、16、20、32、40、80。

CDCL1810A 支持 1 个差分 LVDS 时钟输入以及总共 10 个差分 CML 输出。 CML 输出为交流耦合时，可兼容 LVDS 接收器。

在认真遵守输入电压摆幅和共模电压限制的情况下，CDCL1810A 可支持*引脚配置和功能*中概述的单端时钟输入。

所有器件设置均可通过两线制串口 SDA/SCL 进行编程。 该串口只能承受 1.8V 电压。

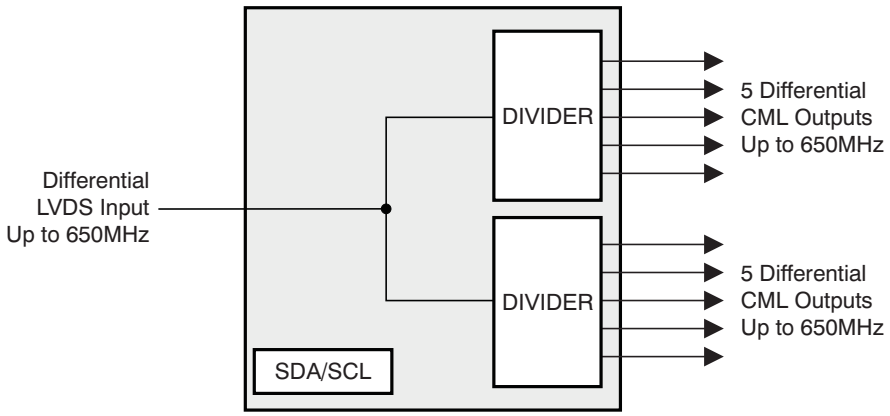
此器件在 1.8V 电源供电环境下运行，额定工作温度范围为 –40°C 至 +85°C。 CDCL1810A 采用 48 引脚 QFN (RGZ) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
CDCL1810A	VQFN (48)	7.00mm x 7.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



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5 修订历史记录

日期	修订版本	注释
2014 年 11 月	*	最初发布。

6 Device Comparison Tables

Table 1. T_A Device Comparison

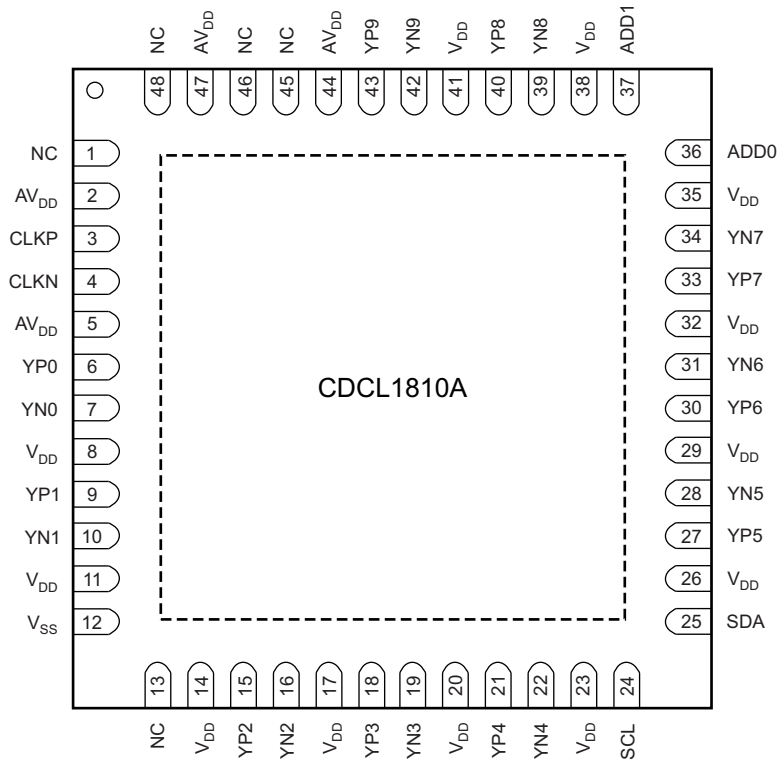
T_A	PACKAGED DEVICES	FEATURES
–40°C to +85°C	CDCL1810ARGZT	48-pin VQFN (RGZ) Package, small tape and reel
–40°C to +85°C	CDCL1810ARGZR	48-pin VQFN (RGZ) Package, tape and reel

Table 2. Device Feature Comparison

FEATURE	CDCL1810	CDCL1810A
Divider Synchronization after power up and after each programming access. During Synchronization all outputs are disabled.	Yes	No
Output Group Phase Adjustment	Yes	No
Device Revision ID	b'011'	b'100'
1:10 Clock Fanout	Yes	Yes
Outputs grouped into two divider banks	Yes	Yes
Individual Output enabled/disable with I2C	Yes	Yes
Continuous and independent operation of outputs which are not programmed, while configuring and programming other outputs.	No	Yes

7 Pin Configuration and Functions

48-Pin
RGZ Package
(Top View)



NOTE: Exposed thermal pad must be soldered to V_{SS}.

The CDCL1810A is available in a 48-pin VQFN (RGZ) package with a pin pitch of 0,5mm. The exposed thermal pad serves both thermal and electrical grounding purposes.

NOTE

The device must be soldered to ground (V_{SS}) using as many ground vias as possible. The device performance will be severely impacted if the exposed thermal pad is not grounded appropriately.

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
V_{DD}	8, 11, 14, 17, 20, 23, 26, 29, 32, 35, 38, 41	Power	1.8V digital power supply.
AV_{DD}	2, 5, 44, 47	Power	1.8V analog power supply.
V_{SS}	Exposed thermal pad and pin 12	Power	Ground reference.
NC	1, 13, 45, 46, 48	I	Not connected; leave open.
CLKP, CLKN	3, 4	I	Differential LVDS input. Single-ended 1.8-V input can be dc-coupled to pin 3 with pin 4 either tied to pin 3 (recommended) or left open.
YP0, YN0 YP1, YN1 YP2, YN2 YP3, YN3 YP4, YN4 YP5, YN5 YP6, YN6 YP7, YN7 YP8, YN8 YP9, YN9	6, 7 9, 10 15, 16 18, 19 21, 22 27, 28 30, 31 33, 34 40, 39 43, 42	O	10 differential CML outputs.
SCL	24	I	SCL serial clock pin. SCL tolerated 1.8V on the input only. Open drain. Always connect to a pull-up resistor.
SDA	25	I/O	SDA bidirectional serial data pin. SDA tolerates 1.8V on the input only.Open drain. Always connect to a pull-up resistor.
ADD1, ADD0	37, 36	I	Configurable least significant bits (ADD[1:0]) of the SDA/SCL device address. The fixed most significant bits (ADD[6:2]) of the 7-bit device address are 11010.

8 Specifications

8.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
V_{DD}, AV_{DD}	Supply voltage(2)	–0.3	2.5	V
V_{LVDS}	Voltage range at LVDS input pins(2)	–0.3	VDD+0.6	V
V_I	Voltage range at all non-LVDS input pins(2)	–0.3	VDD+0.6	V
T_J	Junction temperature		+125	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating condition* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	+150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	

(1) JEDEC document JEP155 states that 2000-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{DD}	Digital supply voltage	1.7	1.8	1.9	V
AV_{DD}	Analog supply voltage	1.7	1.8	1.9	V
T_A	Ambient temperature (no airflow, no heatsink)	–40		+85	°C
T_J	Junction temperature			+105	°C

8.4 Thermal Information

THERMAL METRIC(1)		CDCL1810A RGZ 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2).	28.3, Airflow = 0 LFM	°C/W
		22.4, Airflow = 50 LFM	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) No heatsink; power uniformly distributed; 36 ground vias (6 x 6 array) tied to the thermal exposed pad; 4-layer high-K board.

8.5 DC Electrical Characteristics

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDD}	Total current from digital 1.8V supply	All outputs enabled; $V_{DD} = V_{DD,typ}$ 650MHz LVDS input		212		mA
I_{AVDD}	Total current from analog 1.8V supply	All outputs enabled; $AV_{DD} = V_{DD,typ}$ 650MHz LVDS input		16		mA
$V_{IL,CMOS}$	Low level CMOS input voltage	V_{DD} = 1.8V	–0.2		0.6	V
$V_{IH,CMOS}$	High level CMOS input voltage	V_{DD} = 1.8V	V_{DD} –0.6		V_{DD}	V
$I_{IL,CMOS}$	Low level CMOS input current	$V_{DD} = V_{DD,max}$, V_{IL} = 0.0V			–120	µA
$I_{IH,CMOS}$	High level CMOS input current	$V_{DD} = V_{DD,max}$, V_{IH} = 1.9V			65	µA
$V_{OL,SDA}$	Low level CMOS output voltage for the SDA pin	Sink current = 3 mA	0		$0.2V_{DD}$	V
$I_{OL,CMOS}$	Low level CMOS output current				8	mA

8.6 AC Electrical Characteristics

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_{D,IN}$	Differential input impedance for the LVDS input terminals		90		132	Ω
$V_{CM,IN}$	Common-mode voltage, LVDS input		1125	1200	1375	mV
$V_{S,IN}$	Single-ended LVDS input voltage swing		100		600	mV_{PP}
$V_{D,IN}$	Differential LVDS input voltage swing		200		1200	
$t_{R,OUT}$, $t_{F,OUT}$	Output signal rise/fall time	20%–80%		100		ps
$V_{CM,OUT}$	Common-mode voltage, CML outputs		V_{DD} – 0.31	V_{DD} – 0.23	V_{DD} – 0.19	V
$V_{S,OUT}$	Single-ended CML output voltage swing	ac-coupled	180	230	280	mV_{PP}
$V_{D,OUT}$	Differential CML output voltage swing	measured in a 50-Ω scope; The CML output incorporates 50-Ω resistors to VDD	360	460	560	
F_{IN}	Clock input frequency				650	MHz
F_{OUT}	Clock output frequency				650	

AC Electrical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADDITIVE CLOCK OUTPUT JITTER						
J_{OUT}	F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz $V_{D,IN}$ = 200mV_{PP}	10 Hz to 1 MHz offset		180		fs RMS
		1 MHz to 5 MHz offset		348		
		12 kHz to 5 MHz offset		388		
	F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz $V_{D,IN}$ = 1200mV_{PP}	10 Hz to 1 MHz offset		175		fs RMS
		1 MHz to 5 MHz offset		347		
		12 kHz to 5 MHz offset		388		
	F_{IN} = 650MHz, F_{OUT} = 650MHz $V_{D,IN}$ = 200mV_{PP}	10 Hz to 1 MHz offset		41		fs RMS
		1 MHz to 20 MHz offset		36		
		12 kHz to 20 MHz offset		42		
	F_{IN} = 650MHz, F_{OUT} = 650MHz $V_{D,IN}$ = 1200mV_{PP}	10 Hz to 1 MHz offset		48		fs RMS
		1 MHz to 20 MHz offset		33		
		12 kHz to 20 MHz offset		39		
T_P	Input-to-output delay	F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz YP[9:0] outputs		0.7		ns
TS_{OUT}	Clock output skew	F_{IN} = 30.72MHz, F_{OUT} = 30.72MHz YP[9:0] outputs relative to YP[0]	–64		64	ps

8.7 AC Electrical Characteristics for the SDA/SCL Interface(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCL}	SCL frequency			400	kHz
$t_{h(START)}$	START hold time	0.6			µs
$t_{w(SCLL)}$	SCL low-pulse duration	1.3			µs
$t_{w(SCLH)}$	SCL high-pulse duration	0.6			µs
$t_{su(START)}$	START setup time	0.6			µs
$t_{h(SDATA)}$	SDA hold time	0			µs
$t_{su(DATA)}$	SDA setup time	0.6			µs
$t_{r(SDATA)}$	SCL / SDA input rise time			0.3	µs
$t_{f(SDATA)}$	SCL / SDA input fall time			0.3	µs
$t_{su(STOP)}$	STOP setup time	0.6			µs
t_{BUS}	bus free time	1.3			µs

(1) See Figure 7 for the timing behavior.

8.8 Typical Characteristics

Typical operating conditions are at V_{DD} = 1.8V and T_A = +25°C, $V_{D,IN}$ = 200mV$_{PP}$ (unless otherwise noted).

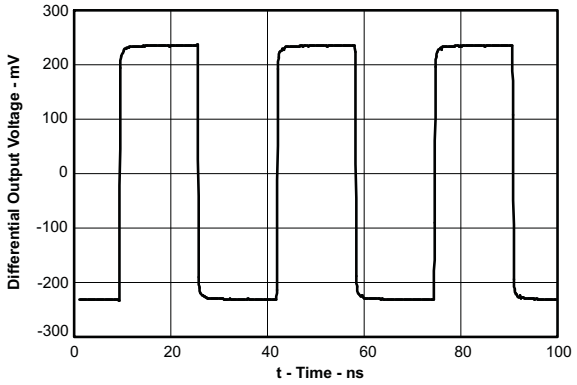


Figure 1. Transient Performance: F_{IN} = 30.72 MHz, F_{OUT} = 30.72 MHz

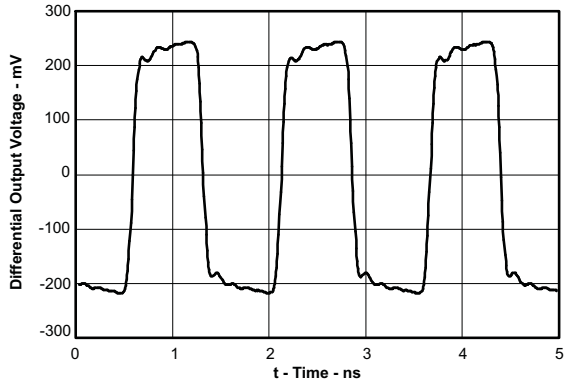


Figure 2. Transient Performance: F_{IN} = 650 MHz, F_{OUT} = 650 MHz

9 Detailed Description

9.1 Overview

The CDCL1810A is a high performance fanout clock buffer that features two banks of independent integer dividers ranging from 1 to 80. CDCL1810A is designed in a way that individual outputs can be configured -- or reconfigured -- without impacting operation of other outputs.

9.2 Functional Block Diagram

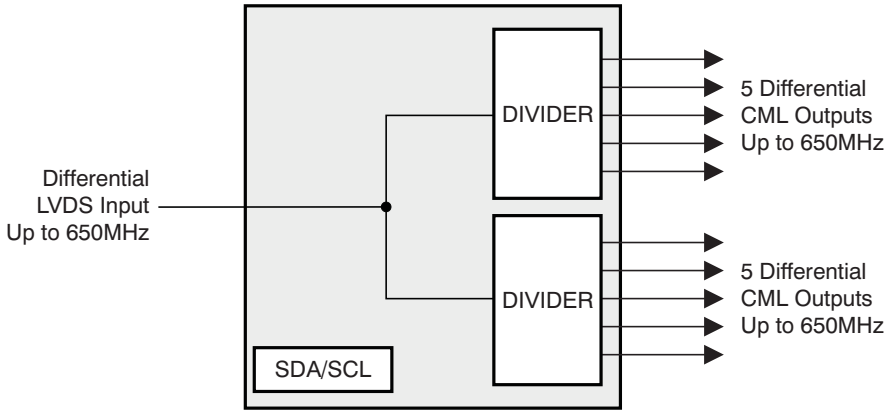
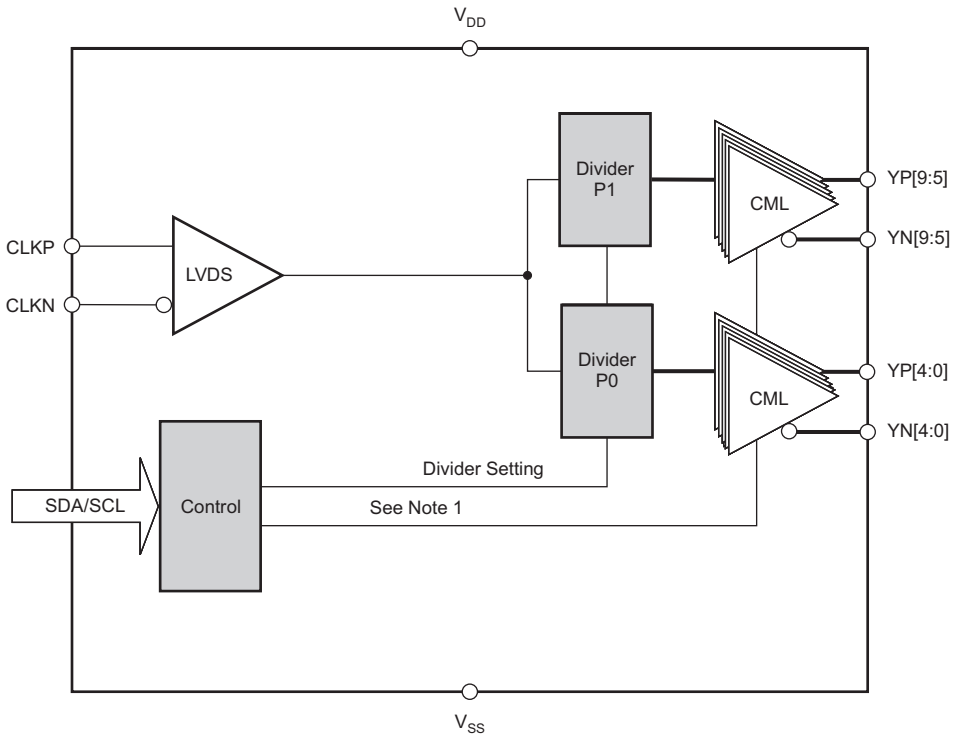


Figure 3. CDCL1810A Simplified Schematic



Note 1: Outputs can be disabled to floating. When outputs are left floating, internal 50 Ω termination to V_{DD} pulls both YN and YP to VDD.

Figure 4. Functional Block Diagram

9.3 Feature Description

9.3.1 Output Enable/Disable

The CDCL1810A does not have an output synchronization feature like the CDCL1810. The CDCL1810A ensures that all outputs stay enabled during any device communication like output enable/disable. Divider changes will apply immediately at the outputs. This may cause a glitch and may result in different phase offsets between both dividers.

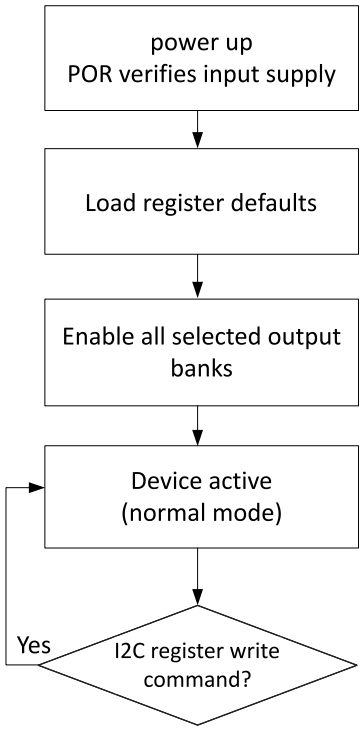


Figure 5. Device Status Flow Chart

9.3.2 SDA/SCL Interface

This section describes the SDA/SCL interface of the CDCL1810A device. The CDCL1810A operates as a slave device of the industry standard 2-pin SDA/SCL bus. It operates in the fast-mode at a bit-rate of up to 400 kbit/s and supports 7-bit addressing compatible with the popular 2-pin serial interface standard.

9.3.2.1 SDA/SCL Bus Slave Device Address

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	ADD1	ADD0	0/1

The device address is made up of the fixed internal address, 11010 (A6:A2), and configurable external pins ADD1 (A1) and ADD0 (A0). Four different devices with addresses 1101000, 1101001, 1101010 and 1101011, can be addressed via the same SDA/SCL bus interface. The least significant bit of the address byte designates a write or read operation.

R/W Bit:

0 = write to CDCL1810A device

1 = read from CDCL1810A device

Feature Description (continued)

9.3.2.2 SDA/SCL Connections Recommendations

The serial interface inputs don't have glitch suppression circuit. So, any noises or glitches at serial input lines may cause programming error. The serial interface lines should be routed in such a way that the lines would have minimum noise impact from the surroundings.

Figure 6 is recommended to improve the interconnections.

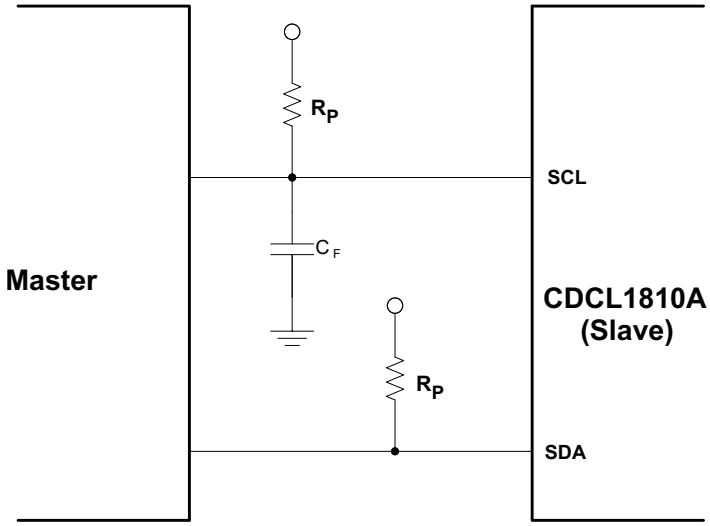


Figure 6. Serial Interface Connections

Lower R_P resistor value (around 1 kΩ) should be chosen so that signals will have faster rise time. A capacitor can be connected to SCL line to ground which will act as a filter.

An I^2C level translator will help to overcome the noises issue.

9.4 Device Functional Modes

The device is designed to operate from an input voltage supply of 1.8 V. In the default power on reset, all device outputs are enabled and the dividers P0 and P1 are set to 1.

9.5 Programming

9.5.1 SDA/SCL Interface

This section describes the SDA/SCL interface of the DCDL1810A device. The CDCL1810A operates as a slave device of the industry standard 2-pin SDA/SCL bus. It operates in the fast-mode at a bit-rate of up to 400 kb/s and supports 7-bit addressing compatible with the popular 2-pin serial interface standard. The device address is made up of the fixed internal address, 11010 (A6:A2), and configurable external pins ADD1 (A1) and ADD0 (A0). Four different devices with addresses 1101000, 1101001, 1101010, and 1101011, can be addressed via the same SDA/SCL bus interface. The least significant bit of the address byte designates a write or read operation.

R/W bit:

0 = write to CDCL1810 device.

1 = read from CDCL1810 device.

9.5.2 Command Code Definition

Table 3. Command Code Definition

BIT	DESCRIPTION
C7	1 = *Byte Write* / *Read* or *Word Write* / *Read* operation
(C6:C0)	Byte Offset for *Byte Write* / *Read* and *Word Write* / *Read* operation.

Table 4. SDA/SCL Bus Slave Device Address

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	ADD1	ADD0	0/1

Table 5. Command Code for Byte Write / Read Operation

	HEX CODE	C7	C6	C5	C4	C3	C2	C1	C0
byte 0	80h	1	0	0	0	0	0	0	0
byte 1	81h	1	0	0	0	0	0	0	1
byte 2	82h	1	0	0	0	0	0	1	0
byte 3	83h	1	0	0	0	0	0	1	1
byte 4	84h	1	0	0	0	0	1	0	0
byte 5	85h	1	0	0	0	0	1	0	1
byte 6	86h	1	0	0	0	0	1	1	0

Table 6. Command Code for Word Write / Read Operation

	HEX CODE	C7	C6	C5	C4	C3	C2	C1	C0
word 0: byte 0 and byte 1	80h	1	0	0	0	0	0	0	0
word 1: byte 1 and byte 2	81h	1	0	0	0	0	0	0	1
word 2: byte 2 and byte 3	82h	1	0	0	0	0	0	1	0
word 3: byte 3 and byte 4	83h	1	0	0	0	0	0	1	1
word 4: byte 4 and byte 5	84h	1	0	0	0	0	1	0	0
word 5: byte 5 and byte 6	85h	1	0	0	0	0	1	0	1
word 6: byte 6 and byte 7	86h	1	0	0	0	0	1	1	0

9.5.3 SDA/SCL Timing Characteristics

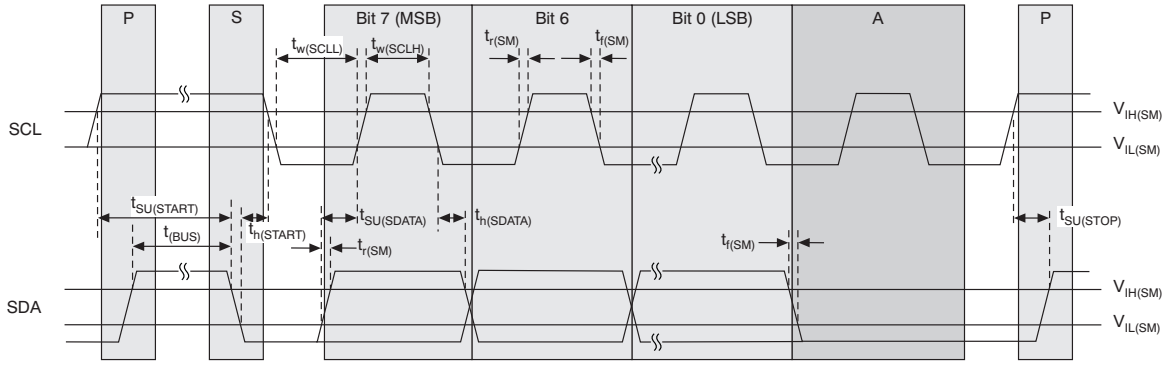


Figure 7. Timing Diagram for the SDA/SCL Serial Control Interface

9.5.4 SDA/SCL Programming Sequence

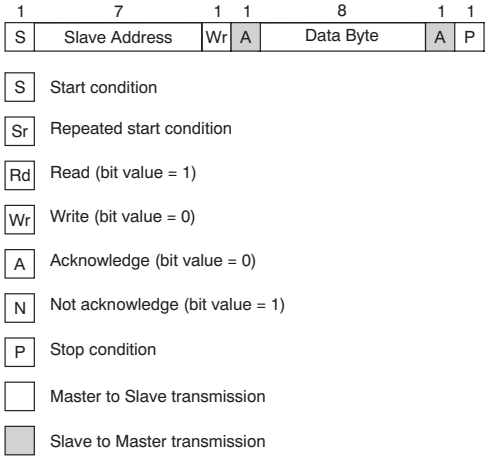


Figure 8. Legend for Programming Sequence

Table 7. *Byte Write* Programming Sequence

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

Table 8. *Byte Read* Programming Sequence

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	N	P

Table 9. *Word Write* Programming Sequence:

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

Table 10. *Word Read* Programming Sequence:

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	A	Data Byte	N	P

9.6 Register Maps

9.6.1 SDA/SCL Bus Configuration Command Bitmap

9.6.1.1 Byte 0:

BIT	BIT NAME	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	REFERENCE TO
7	MANF[7]	Manufacturer reserved	R		
6	MANF[6]	Manufacturer reserved	R		
5	REV[2]	Device revision	R	1	
4	REV[1]	Device revision	R	0	
3	REV[0]	Device revision	R	0	
2	MANF[2]	Manufacturer reserved	R		
1	MANF[1]	Manufacturer reserved	R		
0	MANF[0]	Manufacturer reserved	R		

9.6.1.2 Byte 1:

BIT	BIT NAME	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	REFERENCE TO
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	RES	Reserved	R/W	1	
4	RES	Reserved	R/W	0	
3	RES	Reserved	R/W	0	
2	RES	Reserved	R/W	0	
1	RES	Reserved	R/W	0	
0	RES	Reserved	R/W	0	

9.6.1.3 Byte 2:

BIT	BIT NAME	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	REFERENCE TO
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	ENP1	Post-divider P1 enable; if 0 output YP[9:5] and YN[9:5] are disabled	R/W	1	
4	RES	Reserved	R/W	1	
3	SELP1[3]	Divide ratio select for post-divider P1	R/W	0	Table 11
2	SELP1[2]	Divide ratio select for post-divider P1	R/W	0	Table 11
1	SELP1[1]	Divide ratio select for post-divider P1	R/W	0	Table 11
0	SELP1[0]	Divide ratio select for post-divider P1	R/W	0	Table 11

9.6.1.4 Byte 3:

BIT	BIT NAME	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	REFERENCE TO
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	RES	Reserved	R/W	0	
4	RES	Reserved	R/W	0	
3	RES	Reserved	R/W	0	
2	RES	Reserved	R/W	0	
1	RES	Reserved	R/W	0	
0	RES	Reserved	R/W	0	

9.6.1.5 Byte 4:

BIT	BIT NAME	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	REFERENCE TO
7	RES	Reserved	R/W	0	
6	RES	Reserved	R/W	0	
5	ENP0	Post-divider P0 enable. If 0, output YP[4:0] and YN[4:0] are disabled	R/W	1	
4	RES	Reserved	R/W	1	
3	SELP0[3]	Divide ratio select for post-divider P0	R/W	0	Table 11
2	SELP0[2]	Divide ratio select for post-divider P0	R/W	0	Table 11
1	SELP0[1]	Divide ratio select for post-divider P0	R/W	0	Table 11
0	SELP0[0]	Divide ratio select for post-divider P0	R/W	0	Table 11

9.6.1.6 Byte 5:

BIT	BIT NAME	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	REFERENCE TO
7	EN	Chip enable; if 0 chip is in Iddq mode	R/W	1	
6	RES	Reserved	R	1	
5	ENDRV9	YP[9], YN[9] enable; if 0 output is disabled	R/W	1	
4	ENDRV8	YP[8], YN[8] enable; if 0 output is disabled	R/W	1	
3	ENDRV7	YP[7], YN[7] enable; if 0 output is disabled	R/W	1	
2	ENDRV6	YP[6], YN[6] enable; if 0 output is disabled	R/W	1	
1	ENDRV5	YP[5], YN[5] enable; if 0 output is disabled	R/W	1	
0	ENDRV4	YP[4], YN[4] enable; if 0 output is disabled	R/W	1	

9.6.1.7 Byte 6:

BIT	BIT NAME	DESCRIPTION/FUNCTION	TYPE	POWER UP CONDITION	REFERENCE TO
7	ENDRV3	YP[3], YN[3] enable; if 0 output is disabled	R/W	1	
6	ENDRV2	YP[2], YN[2] enable; if 0 output is disabled	R/W	1	
5	ENDRV1	YP[1], YN[1] enable; if 0 output is disabled	R/W	1	
4	ENDRV0	YP[0], YN[0] enable; if 0 output is disabled	R/W	1	
3	RES	Reserved	R/W	0	
2	RES	Reserved	R/W	0	
1	RES	Reserved	R/W	0	
0	RES	Reserved	R/W	0	

Table 11. Divide Ratio Settings for Post-Divider P0 or P1

DIVIDE RATIO	SELP1[3] or SELP0[3]	SELP1[2] or SELP0[2]	SELP1[1] or SELP0[1]	SELP1[0] or SELP0[0]	NOTES
1	0	0	0	0	Default
2	0	0	0	1	
4	0	0	1	0	
5	0	0	1	1	
8	0	1	0	0	
10	0	1	0	1	
16	0	1	1	0	
20	0	1	1	1	
32	1	0	0	0	
40	1	0	0	1	
80	1	0	1	0	

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The CDCL1810 is a high-performance buffer that can generate 10 copies of CML clock outputs from a LVDS input. The programmable dividers, P0 and P1, give a high flexibility to the ratio of the output frequency to the input frequency.

10.1.1 Clock Distribution for Multiple TI Keystone DSPs

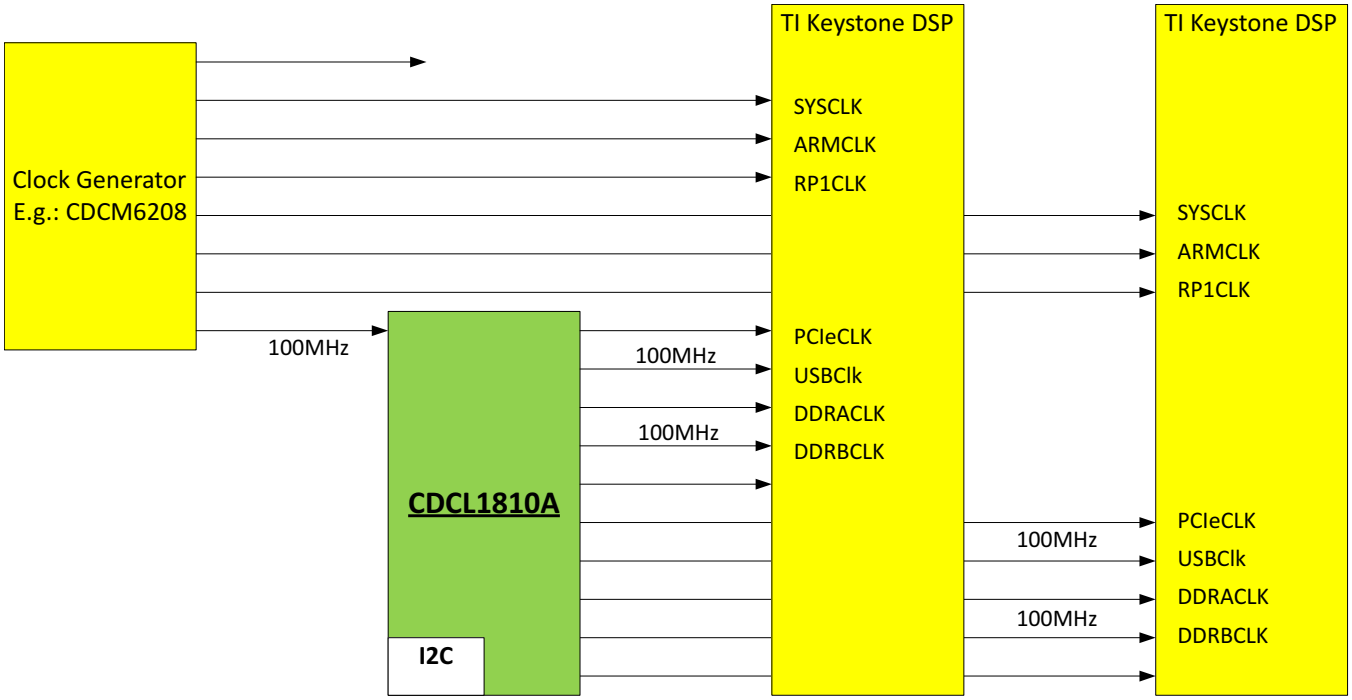


Figure 9. CDCL1810A Application Drawing

10.1.1.1 Design Requirements

A typical application example is multi DSP chip environment. The CDCL1810A is used to buffer the common clocks to the DSP.

10.1.1.2 Detailed Design Procedure

The CDCL1810A does not support output group phase alignment if a divider gets reprogrammed. Both clock groups might be out of phase by multiple input clock cycles. This is especially of concern if both dividers are greater than 1 (see Figure 10).

Continuous operation of output clocks is ensured, while enabling/disabling of outputs in the CDCL1810A. (see Figure 11).

Application Information (continued)

10.1.1.3 Application Curves

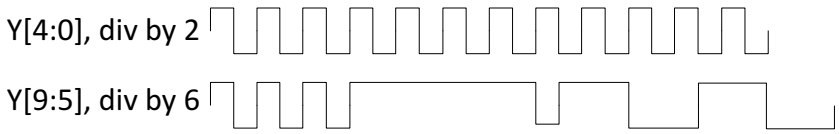


Figure 10. Output Group Divider Change

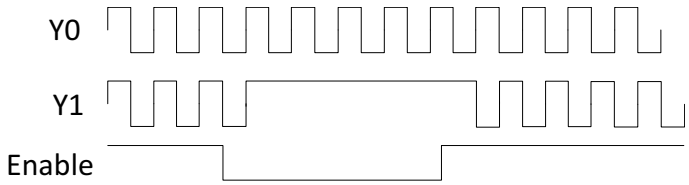


Figure 11. Individual Output Disable/Enable

11 Power Supply Recommendations

The device is designed to operate from an input voltage supply of 1.8 V for analog supply (AVDD) and core supply (VDD). Both AVDD and VDD can be supplied by a single source.

12 Layout

12.1 Layout Guidelines

- Keep the connections between the bypass capacitors and the power supply on the device as short as possible.
- Ground the other side of the capacitor using a low impedance connection to the ground plane.
- If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the Thermal Dissipation Pad can be difficult.
- For component side mounting, use 0201 body size capacitors to facilitate signal routing.

NOTE

The device must be soldered to ground (V_{SS}) using as many ground vias as possible. The device performance will be severely impacted if the exposed thermal pad is not grounded appropriately.

12.2 Layout Example

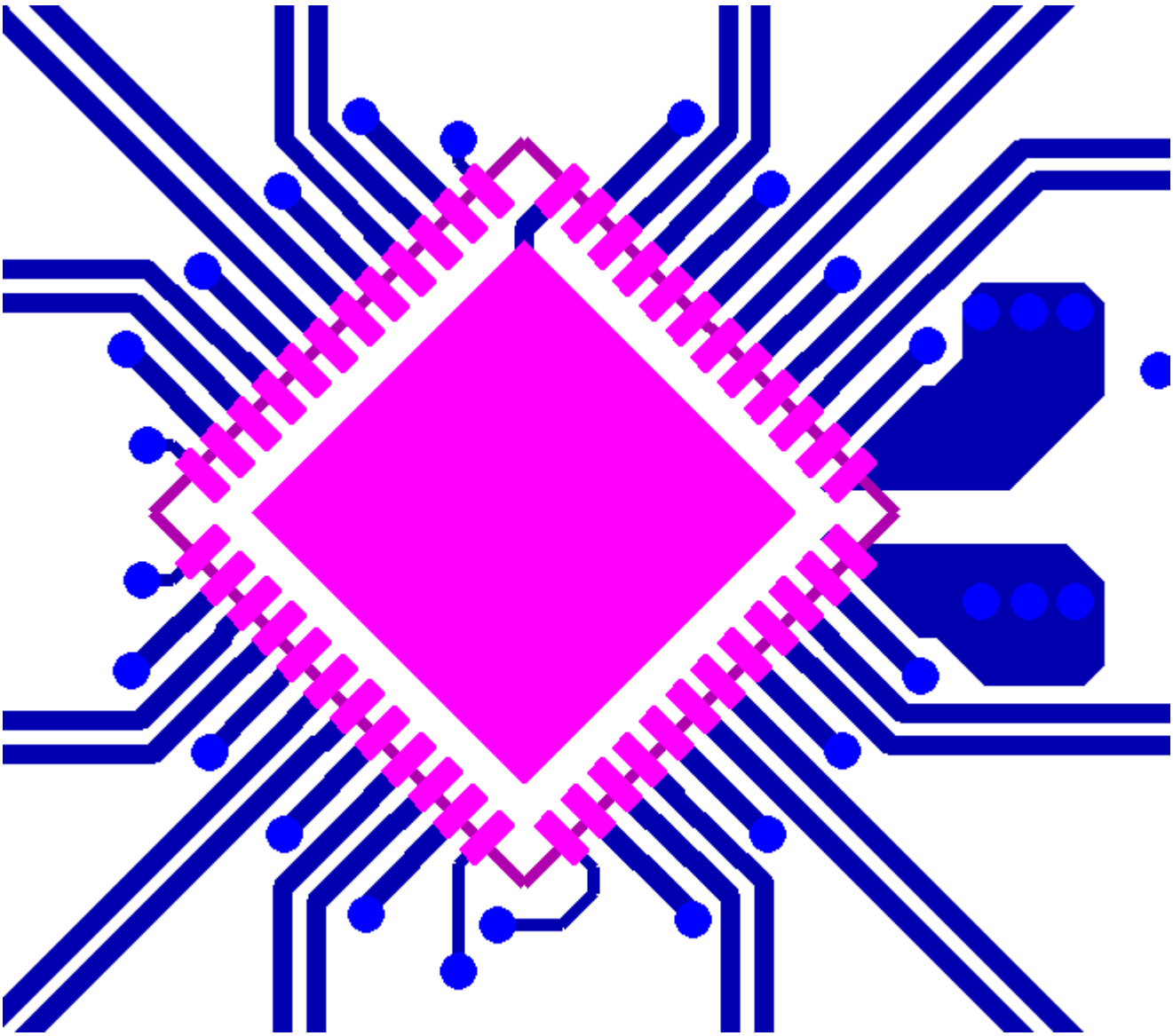


Figure 12. Layout Example: Signal Layer (TOP)

Layout Example (continued)

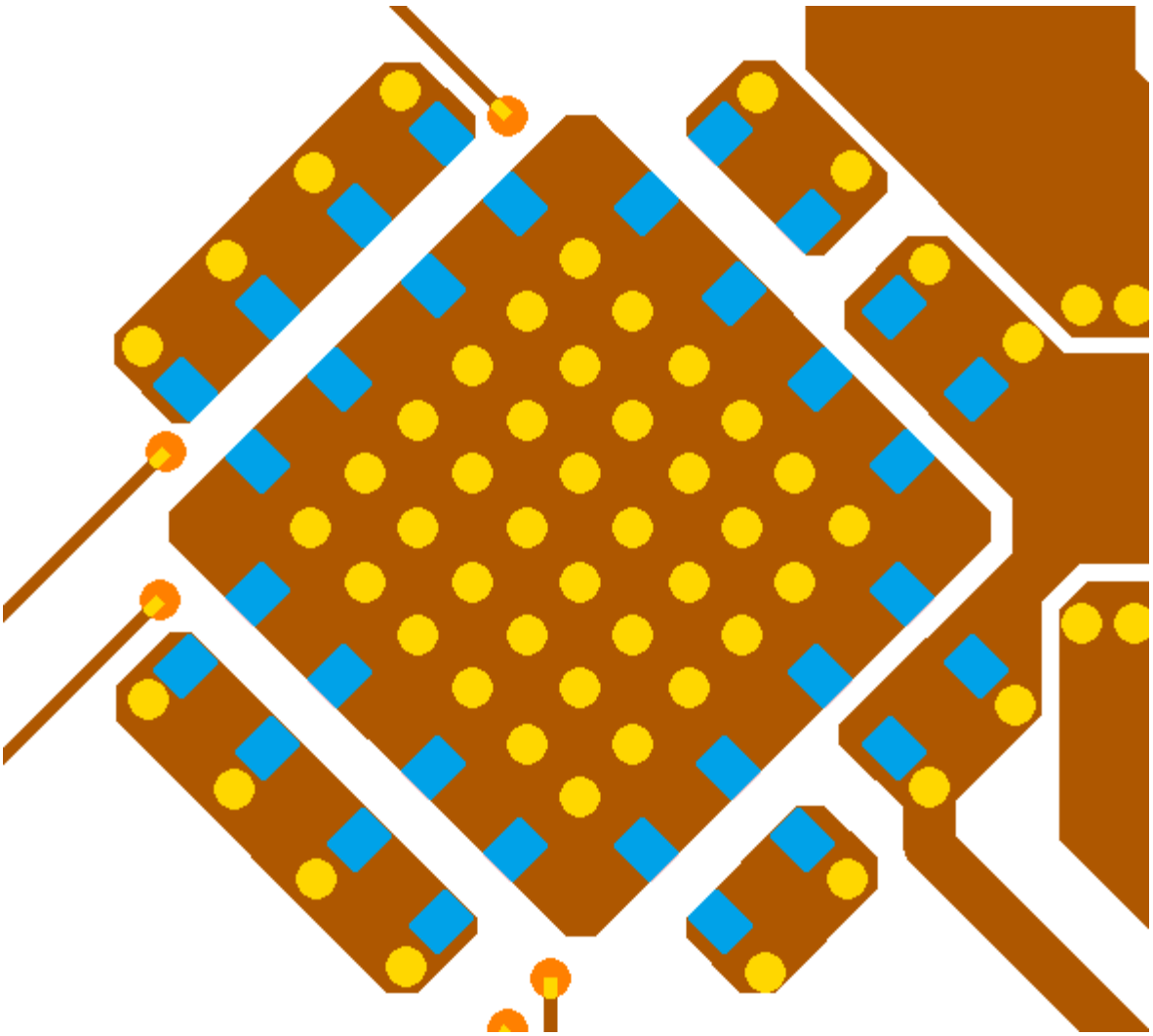


Figure 13. Layout Example: Bottom Layer with Decoupling Capacitors

13 器件和文档支持

13.1 商标

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13.2 静电放电警告

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13.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCL1810ARGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCL 1810A	Samples
CDCL1810ARGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCL 1810A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

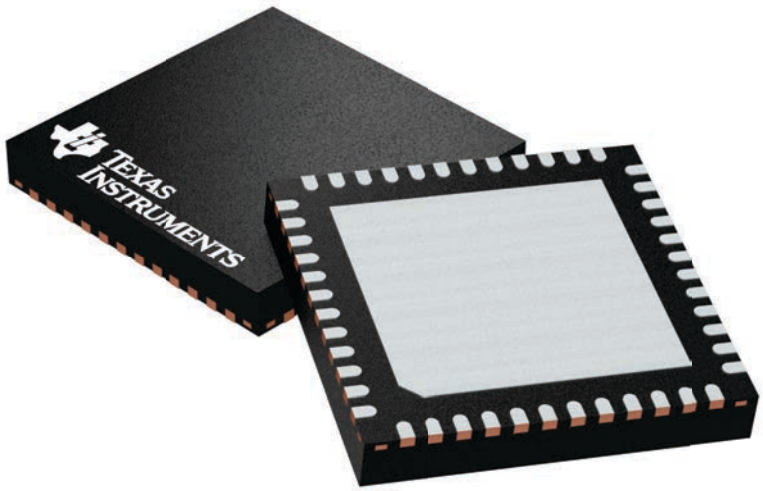
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

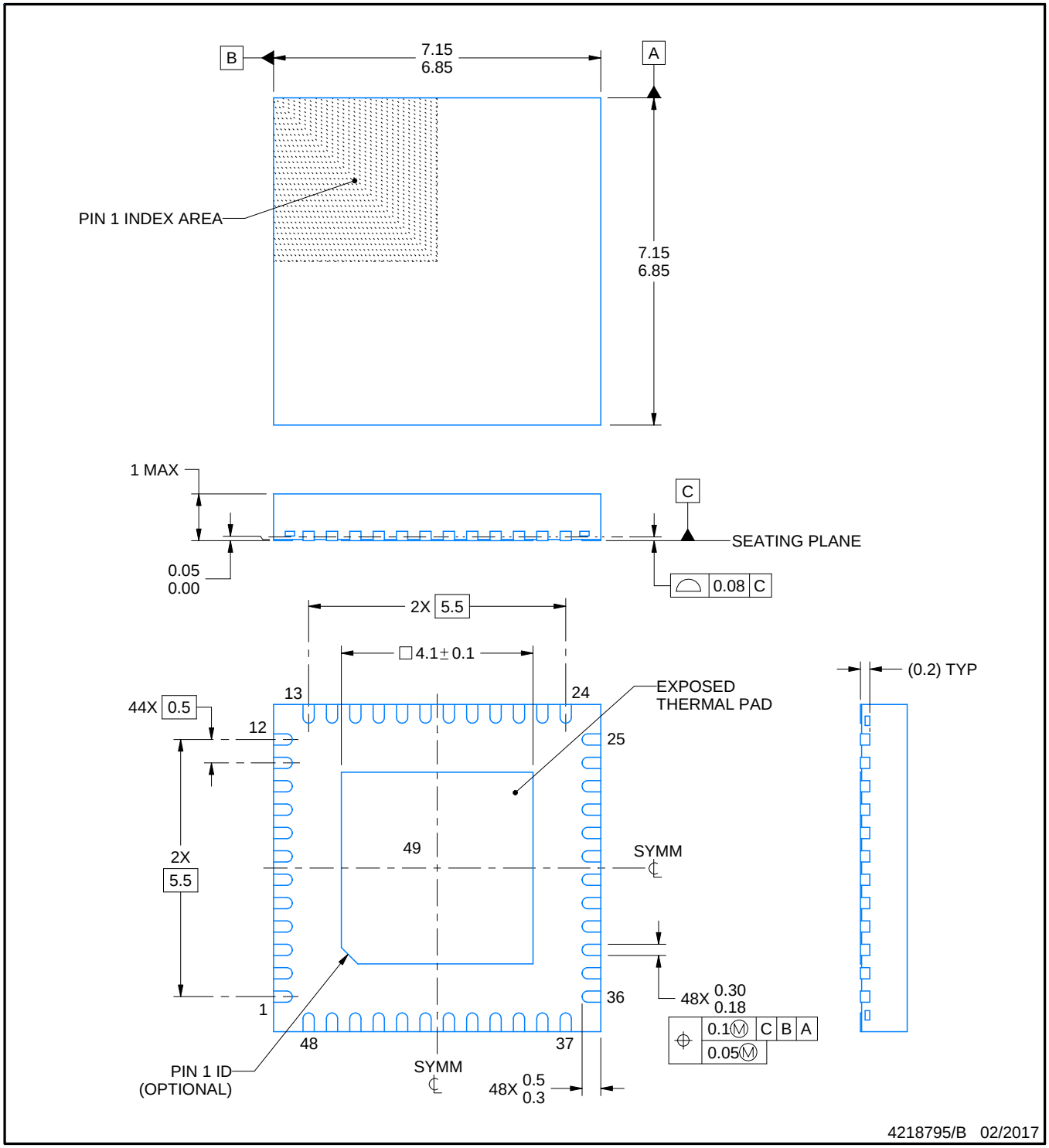
4224671/A

RGZ0048B

PACKAGE OUTLINE

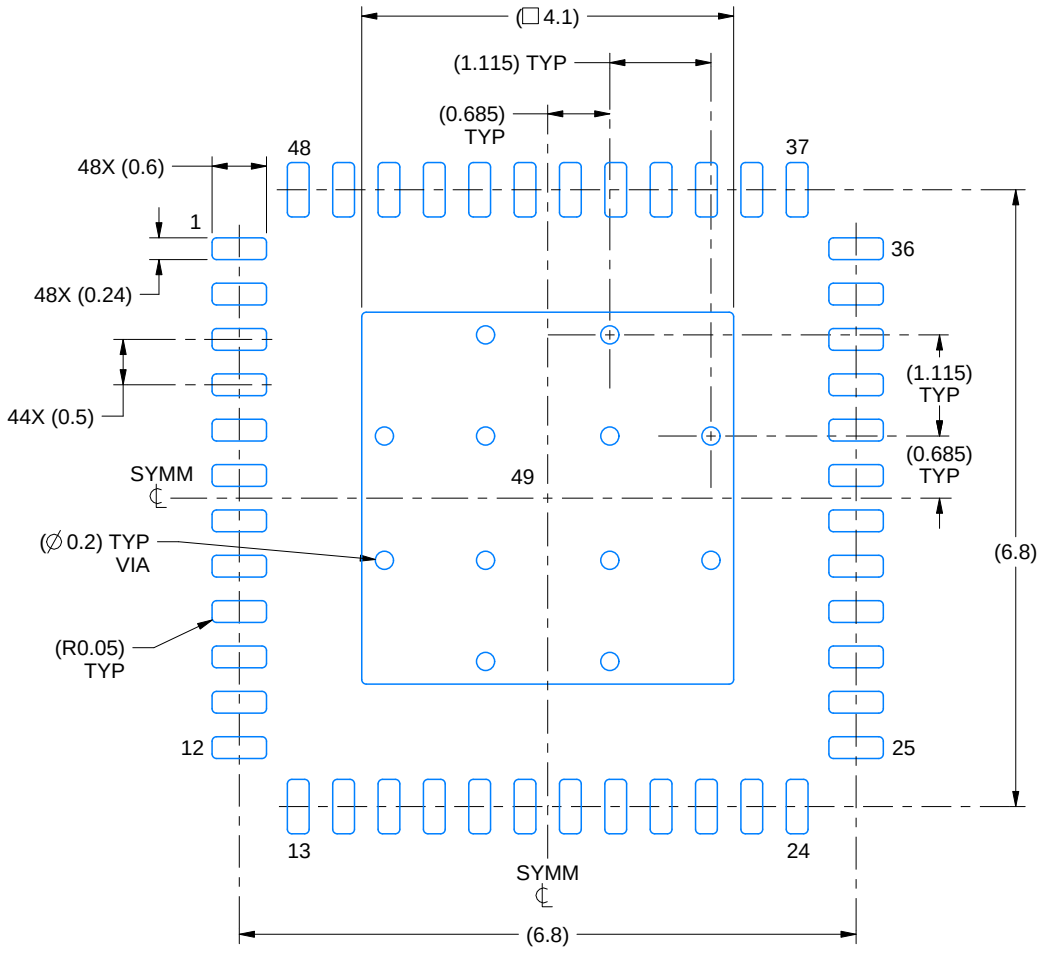
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

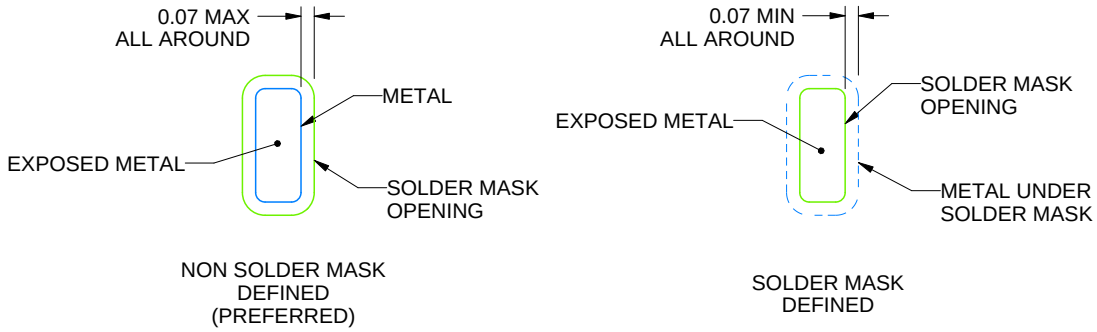


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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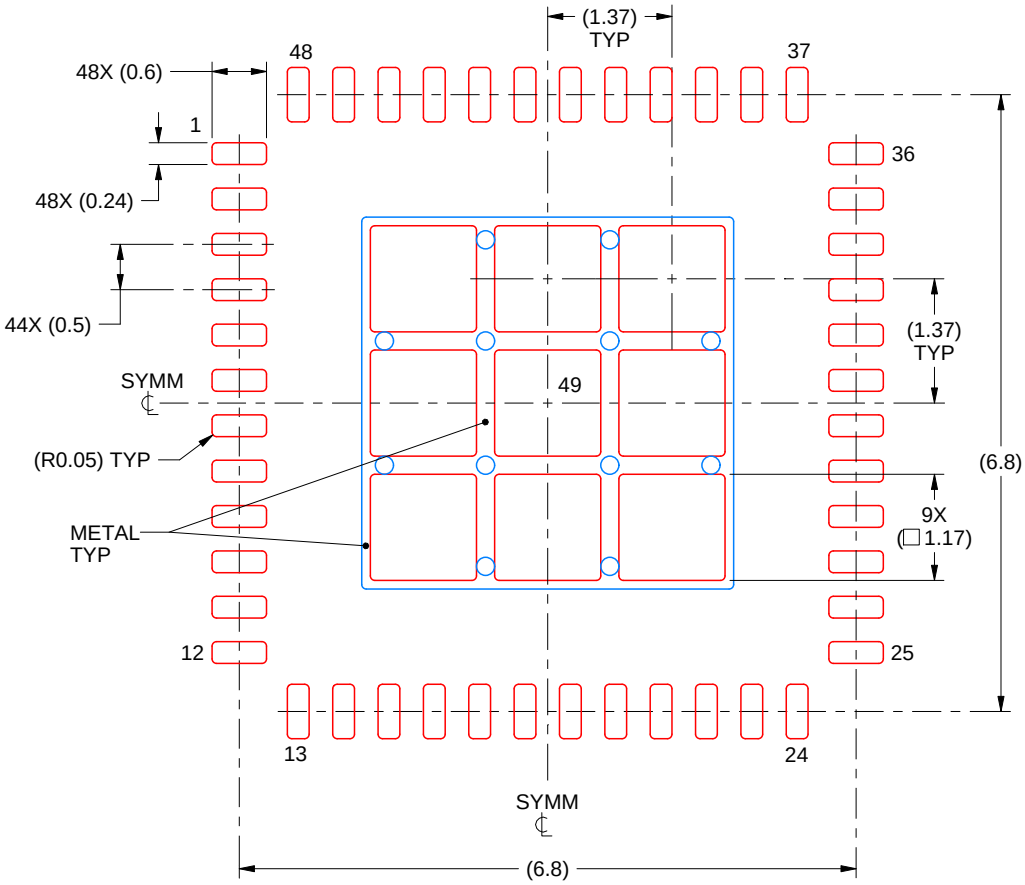
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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