CSD13202Q2 12V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm x 2mm 塑料封装

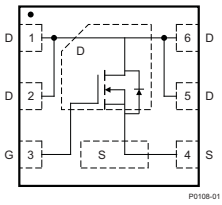
2 应用

- 针对负载开关应用 进行了优化
- 存储、平板电脑和手持设备
- 优化后可适用于控制场效应晶体管 (FET) 应用
- 负载点同步降压转换器

3 说明

此 12V、7.5mΩ NexFET™功率 MOSFET 旨在最大限度降低功率转换和负载管理 应用中的损耗。该 SON 2 × 2 封装尺寸可提供出色的热性能。

顶视图



产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	12		V
Q_g	总栅极电荷 (4.5V)	5.1		nC
Q_{gd}	栅极电荷（栅极到漏极）	0.76		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 2.5V	9.1	mΩ
		V_{GS} = 4.5V	7.5	
$V_{GS(th)}$	阈值电压	0.8		V

器件信息

器件	包装介质	数量	封装	发货
CSD13202Q2	7 英寸卷带	3000	SON 2.00mm × 2.00mm 塑料封装	卷带封装

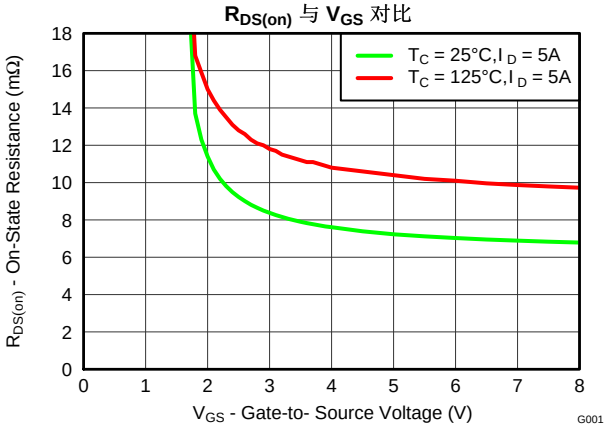
绝对最大额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	12	V
V_{GS}	栅源电压	±8	V
I_D	持续漏极电流（受封装限制）	22	A
	持续漏极电流(1)	14.4	
I_{DM}	脉冲漏极电流，T_A = 25°C 时测得(2)	76	A
P_D	功率耗散(1)	2.7	W
T_J, T_{STG}	工作结温、储存温度	–55 至 150	°C
E_{AS}	雪崩能量，单脉冲 I_D = 20A，L = 0.1mH，R_G = 25Ω	20	mJ

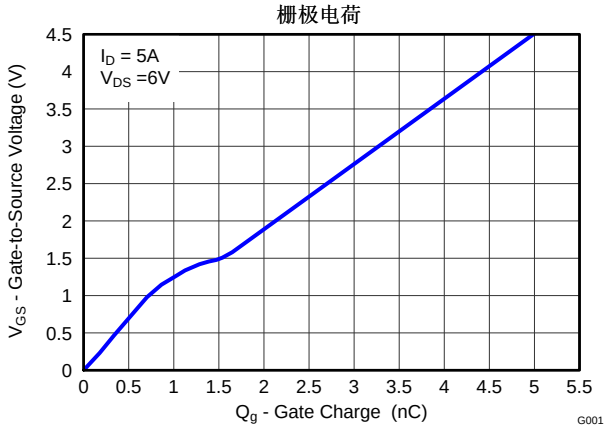
(1) $R_{\theta JA}$ = 45°C/W，这是在一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 平方英寸，2 盎司覆铜上测得的值。

(2) 脉冲持续时间 10µs，占空比 ≤ 2%。

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



目录

4 修订历史记录

Changes from Original (September 2013) to Revision A **Page**

- 已添加 *器件信息* 表、*规格* 部分、*器件和文档支持* 部分和*机械、封装和可订购信息* 部分 1
- 更新了机械制图 8

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C, unless otherwise specified

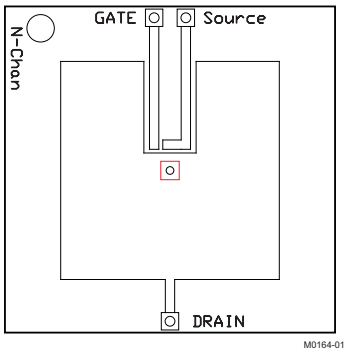
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 µA	12			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 9.6 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 8 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = 250 µA	0.58	0.80	1.10	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5 V, I_{DS} = 5 A		9.1	11.6	mΩ
		V_{GS} = 3 V, I_{DS} = 5 A		8.4	10.4	
		V_{GS} = 4.5 V, I_{DS} = 5 A		7.5	9.3	
g_{fs}	Transconductance	V_{DS} = 6 V, I_{DS} = 5 A		44		S
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0V, V_{DS} = 6 V, f = 1 MHz		767	997	pF
C_{OSS}	Output capacitance			506	657	pF
C_{RSS}	Reverse transfer capacitance			43	56	pF
R_g	Series gate resistance			0.7	1.4	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 6 V, I_{DS} = 5 A		5.1	6.6	nC
Q_{gd}	Gate charge gate-to-drain			0.76		nC
Q_{gs}	Gate charge gate-to-source			0.98		nC
$Q_{g(th)}$	Gate charge at Vth			0.57		nC
Q_{OSS}	Output charge	V_{DS} = 6 V, V_{GS} = 0 V		5.7		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 6 V, V_{GS} = 4.5 V, I_{DS} = 5 A R_G = 2 Ω		4.5		ns
t_r	Rise time			28		ns
$t_{d(off)}$	Turnoff delay time			11.0		ns
t_f	Fall time			13.6		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{DS} = 5 A, V_{GS} = 0 V		0.75	1	V
Q_{rr}	Reverse recovery charge	V_{DD} = 6 V, I_F = 5 A, di/dt = 200 A/µs		13		nC
t_{rr}	Reverse recovery time			28		ns

5.2 Thermal Characteristics

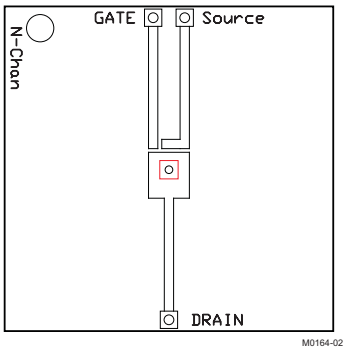
T_A = 25°C unless otherwise stated

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance junction-to-case (1)			6.4	°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient (1) (2)			60	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 60 when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 210 when mounted on minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

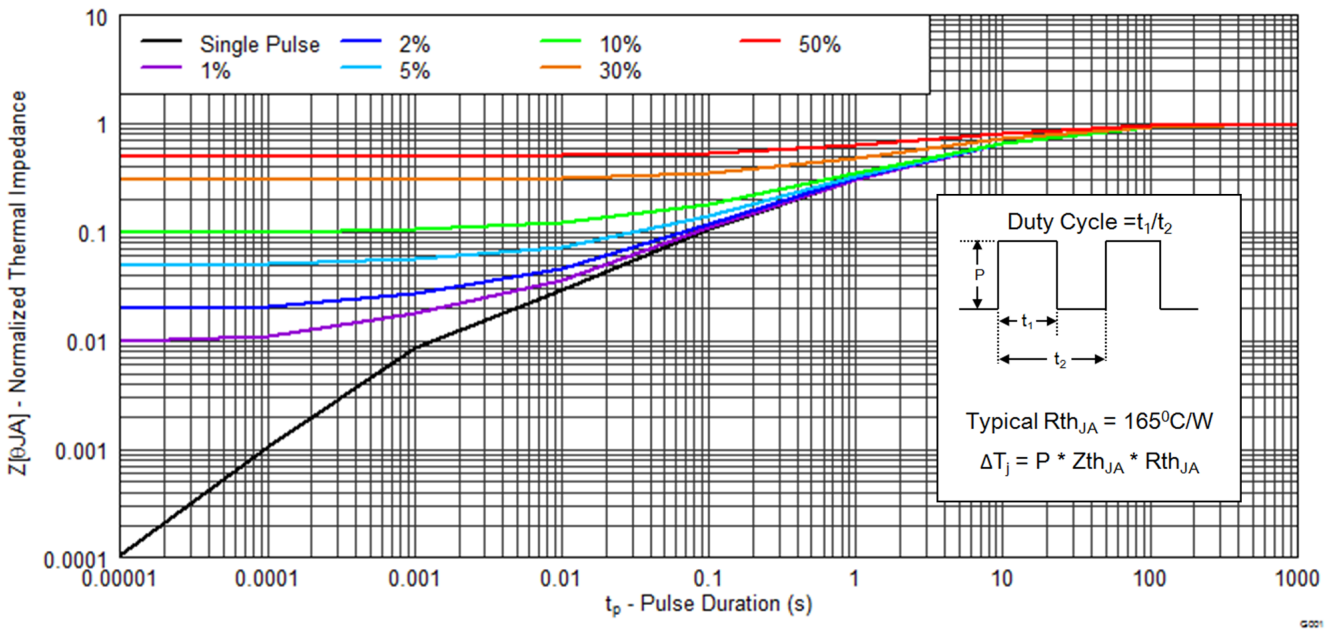


Figure 1. Transient Thermal Impedance

Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

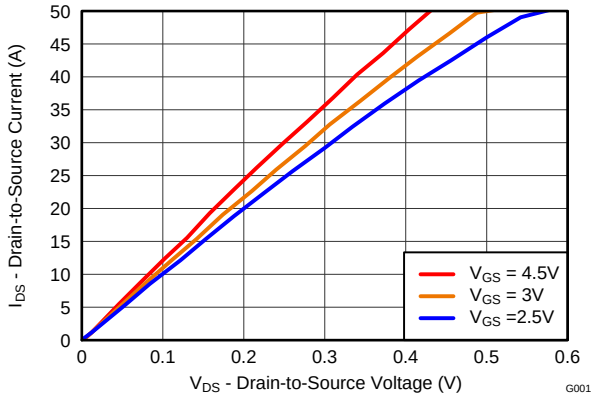


Figure 2. Saturation Characteristics

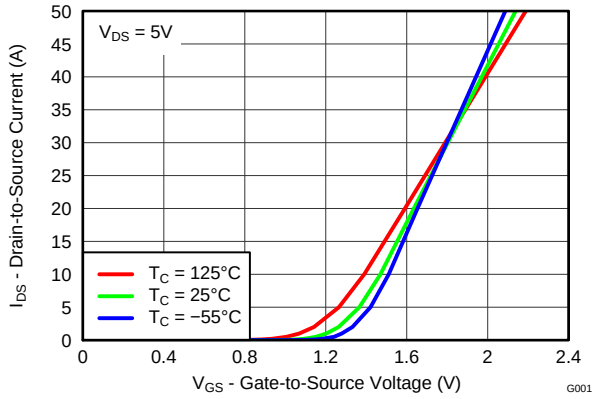


Figure 3. Transfer Characteristics

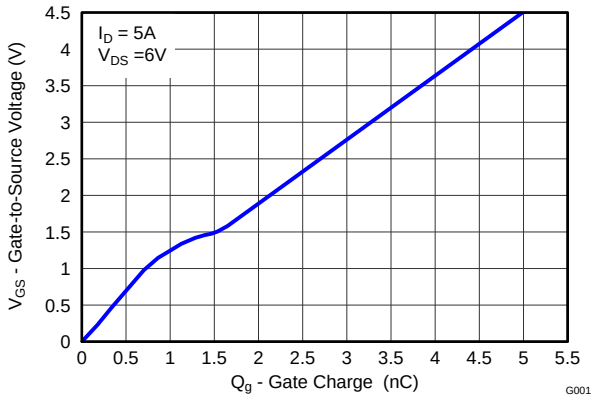


Figure 4. Gate Charge

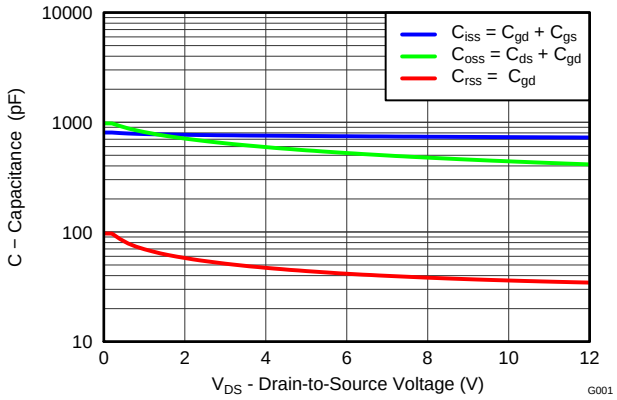


Figure 5. Capacitance

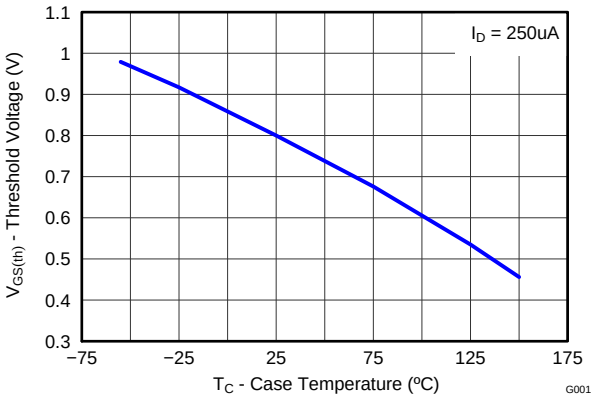


Figure 6. Threshold Voltage vs Temperature

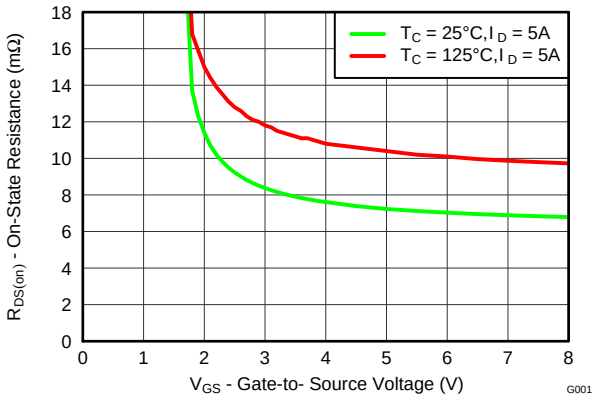


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

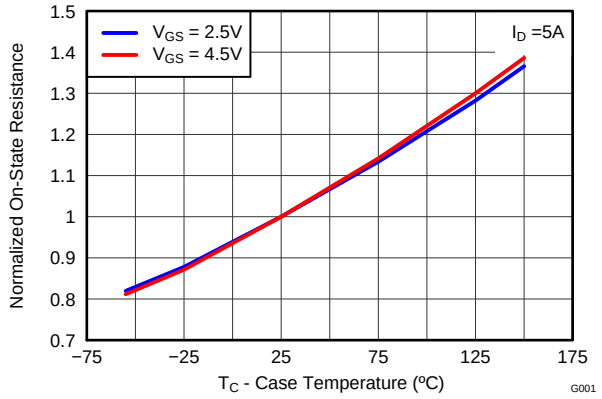


Figure 8. Normalized On-State Resistance vs Temperature

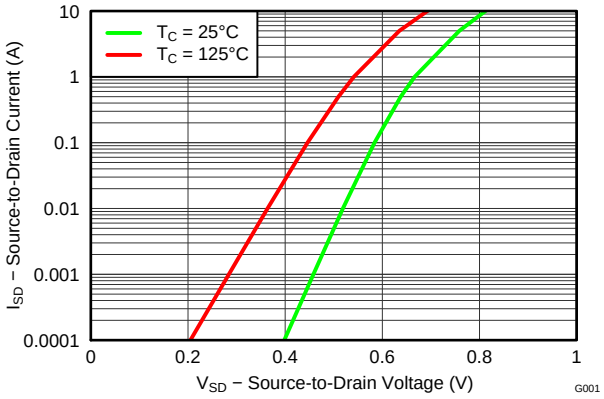


Figure 9. Typical Diode Forward Voltage

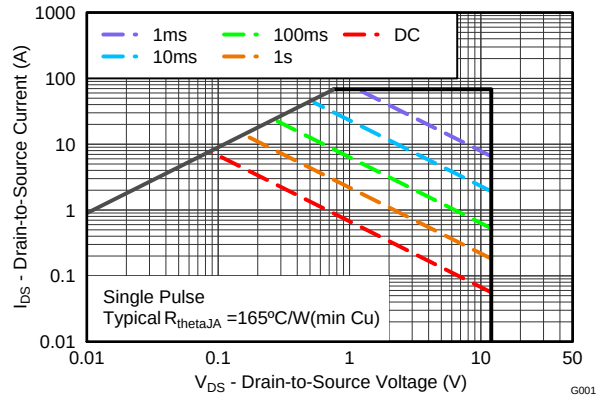


Figure 10. Maximum Safe Operating Area

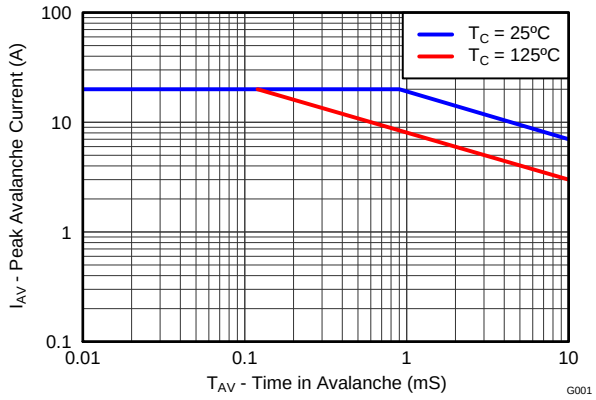


Figure 11. Single Pulse Unclamped Inductive Switching

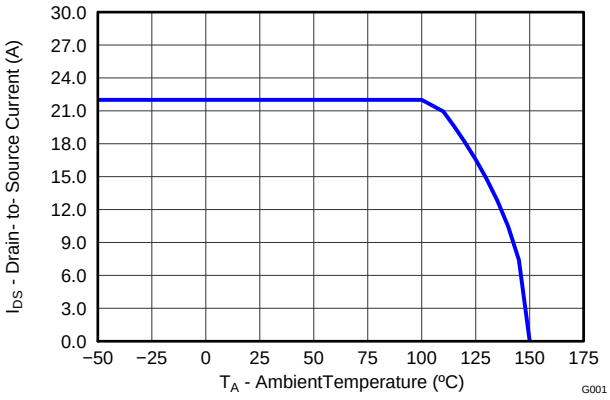


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

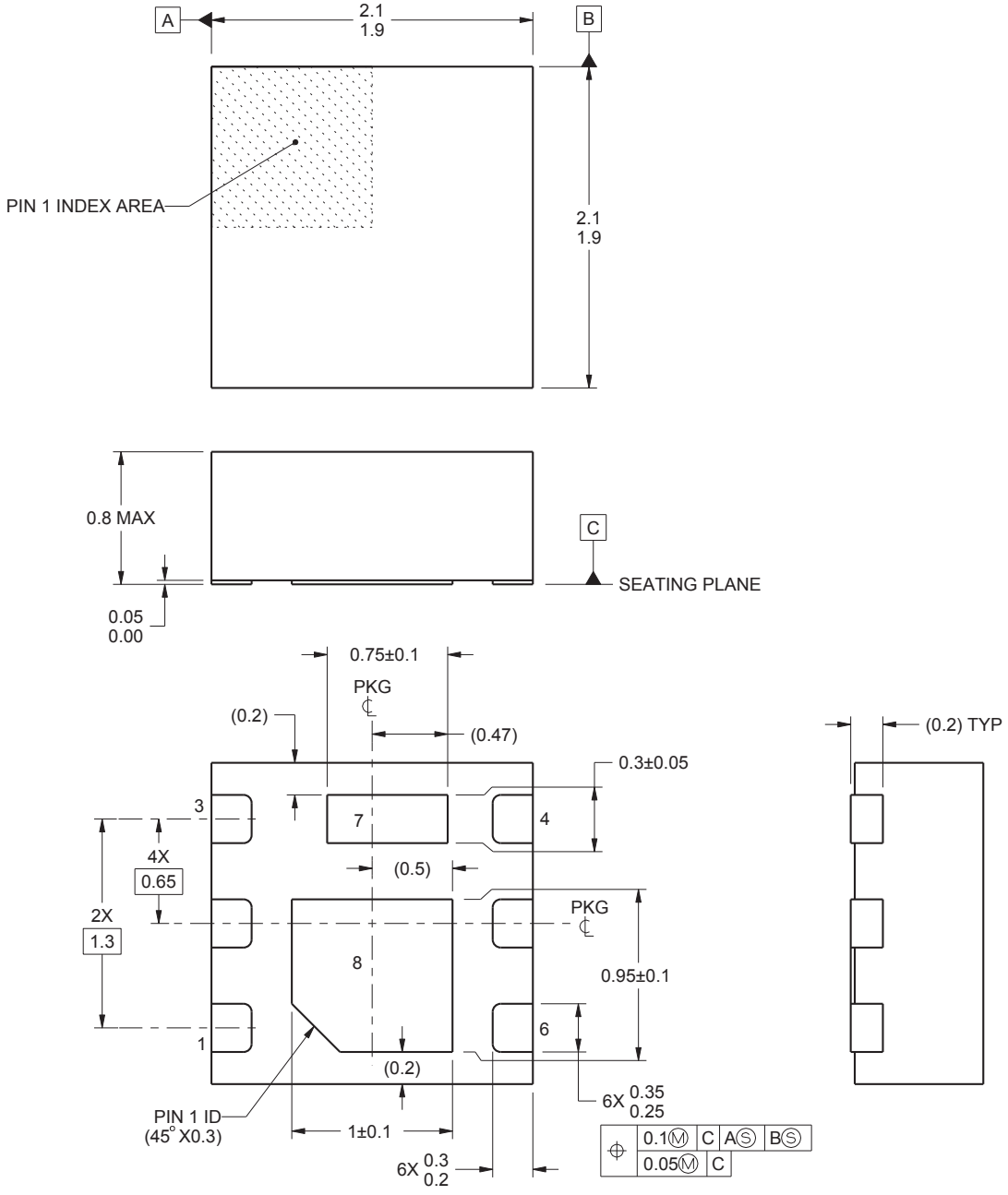
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

7.1 Q2 封装尺寸

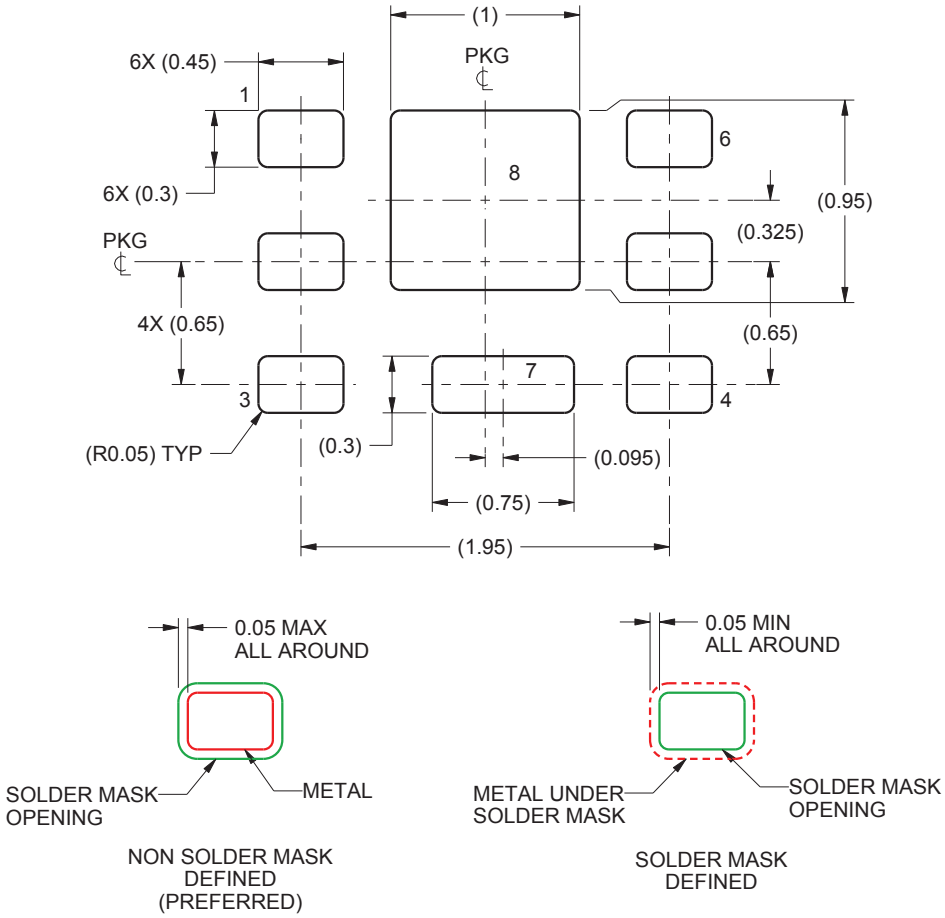


4222322/A 08/2015

1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 封装散热盘必须在印刷电路板上焊接，包装散热和机械性能。

Q2 封装尺寸 (接下页)

7.1.1 建议 PCB 布局

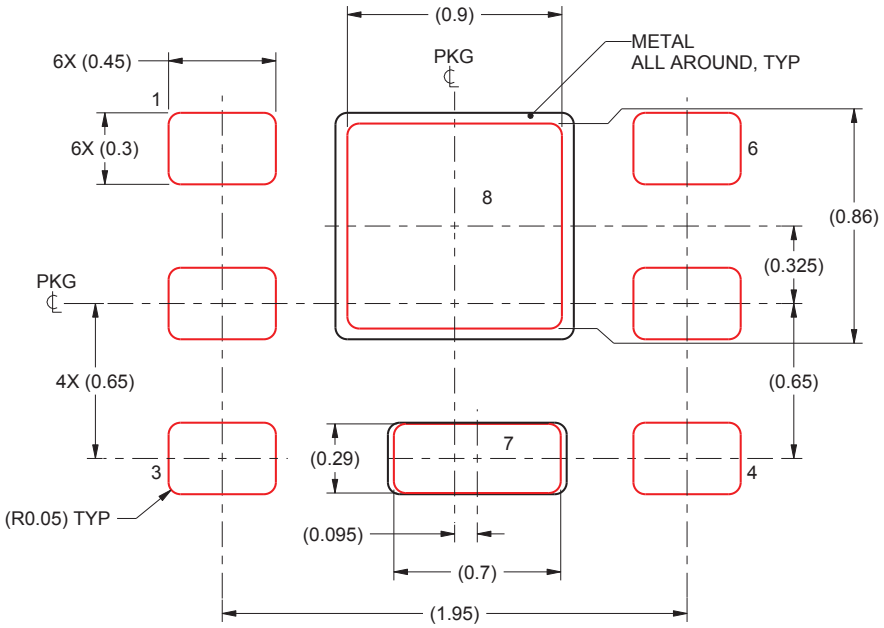


SOLDER MASK DETAILS

1. 此封装设计用于焊接到电路板的散热焊盘上。有关更多信息，请参阅《*QFN/SON PCB 连接*》(SLUA271)。

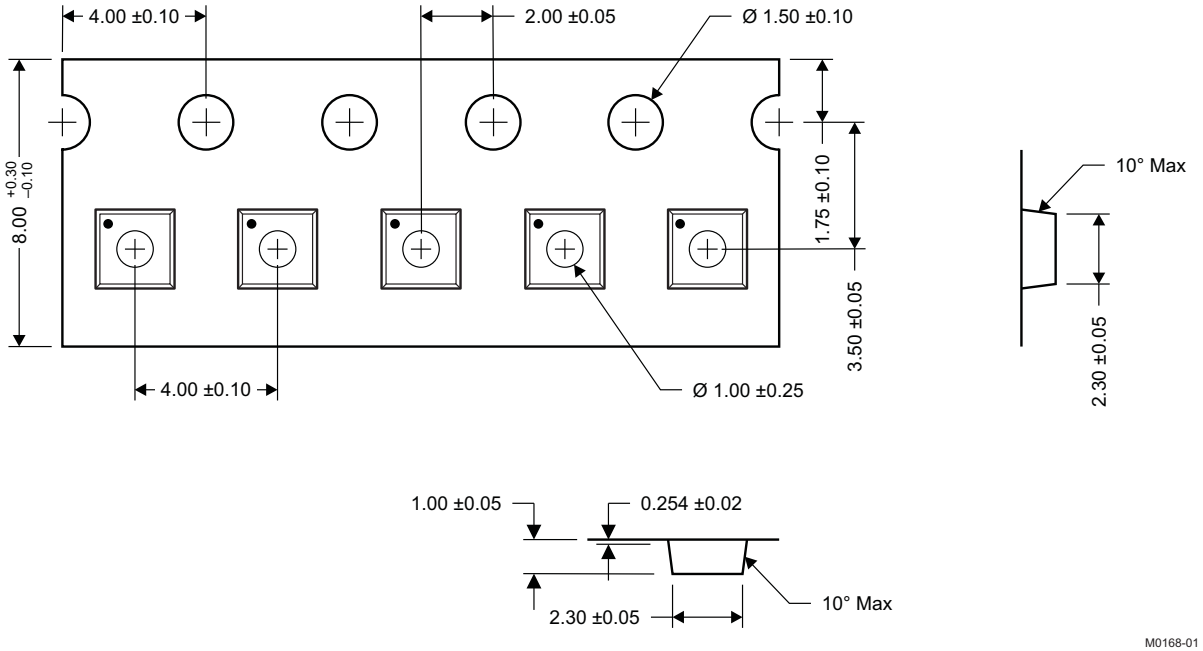
Q2 封装尺寸 (接下页)

7.1.2 推荐的模版布局



1. 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

7.2 Q2 卷带信息



Notes:
1. 测自链齿孔中心线到孔眼中心线。
2. 10 个链齿孔的累积容差为 ±0.2。
3. 提供了其他材料。
4. 卷带的 SR 典型值最大为 10^9 OHM/SQ。
5. 所有尺寸单位均为 mm，除非另有说明。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13202Q2	ACTIVE	WSON	DQK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 150	1322	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要声明和免责声明

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