

20V N 通道 NexFET™ 功率金属氧化物场效应晶体管 (MOSFET)

查询样品: CSD15571Q2

特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅端子镀层
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 2mm x 2mm 塑料封装

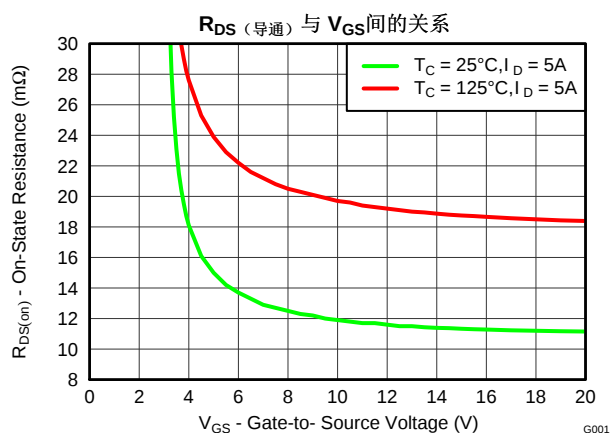
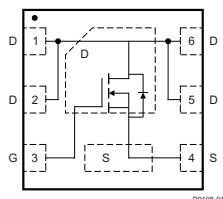
应用范围

- 针对负载开关应用进行了优化
- 存储、平板电脑和手持类器件
- 针对控制场效应晶体管 (FET) 应用进行了优化
- 负载点同步降压转换器

说明

此 NexFET™ 功率 MOSFET 被设计成在功率转换和负载管理应用中大大降低功率损耗。小外形尺寸无引线 (SON) 2mm x 2mm 封装提供针对封装尺寸的出色散热性能。

顶视图



产品概述

V_{DS}	漏源电压	20	V
Q_g	栅极电荷总量 (4.5V)	2.5	nC
Q_{gd}	栅漏栅极电荷	0.66	nC
$R_{DS(on)}$ (导通)	漏源导通电阻	$V_{GS}=4.5\text{V}$	16 mΩ
		$V_{GS}=10\text{V}$	12 mΩ
$V_{GS(th)}$	阈值电压	1.45	V

订购信息

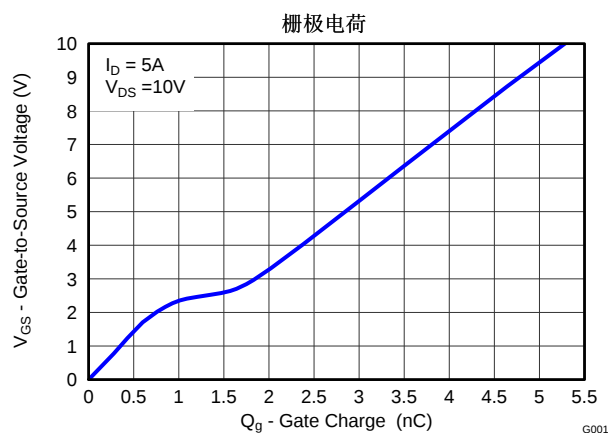
器件	封装	介质	数量	出货
CSD15571Q2	SON 2mm x 2mm 塑料封装	7 英寸卷带	3000	卷带封装

绝对最大额定值

$T_A=25^\circ\text{C}$ 时测得, 除非另外注明		值	单位
V_{DS}	漏源电压	20	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	22	A
	持续漏极电流 ⁽¹⁾	10	A
I_{DM}	脉冲漏极电流, $T_A=25^\circ\text{C}$ 时测得 ⁽²⁾	52	A
P_D	功率耗散 ⁽¹⁾	2.5	W
T_J, T_{STG}	运行结温和储存温度范围	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单脉冲 $I_D=19\text{A}, L=0.1\text{mH}, R_G=25\Omega$	18	mJ

(1) $R_{\theta JA} = 50$, 这是在 1 平方英寸纯铜 (2 盎司), 厚度为 .060" 的环氧板 (FR4) 印刷电路板 (PCB) 上测得的值。

(2) 脉冲持续时间 10μs, 占空比 ≤ 2%



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English Data Sheet: SLPS435



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise specified

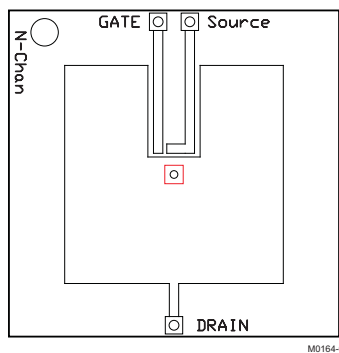
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV _{DSS}	Drain to Source Voltage	V _{GS} = 0V, I _D = 250μA	20			V
I _{DSS}	Drain to Source Leakage Current	V _{GS} = 0V, V _{DS} = 20V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{DS} = 0V, V _{GS} = 20V			100	nA
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250μA	1.10	1.45	1.90	V
R _{DS(on)}	Drain to Source On Resistance	V _{GS} = 4.5V, I _{DS} = 5A		16.0	19.2	mΩ
		V _{GS} = 10V, I _{DS} = 5A		12.0	15.0	mΩ
g _{fs}	Transconductance	V _{DS} = 16V, I _{DS} = 5A		25		S
Dynamic Characteristics						
C _{ISS}	Input Capacitance	V _{GS} = 0V, V _{DS} = 10V, f = 1MHz		320	419	pF
C _{OSS}	Output Capacitance			184	239	pF
C _{RSS}	Reverse Transfer Capacitance			32	42	pF
R _g	Series Gate Resistance			3.8	7.6	Ω
Q _g	Gate Charge Total (4.5V)	V _{DS} = 10V, I _{DS} = 5A		2.5	3.3	nC
Q _g	Gate Charge Total (10V)			5.1	6.7	nC
Q _{gd}	Gate Charge – Gate to Drain			0.66		nC
Q _{gs}	Gate Charge Gate to Source			0.93		nC
Q _{g(th)}	Gate Charge at V _{th}			0.52		nC
Q _{OSS}	Output Charge	V _{DS} = 10V, V _{GS} = 0V		4.1		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 10V, V _{GS} = 4.5V, I _{DS} = 5A R _G = 2Ω		4.7		ns
t _r	Rise Time			17.2		ns
t _{d(off)}	Turn Off Delay Time			9.9		ns
t _f	Fall Time			4.1		ns
Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{DS} = 5A, V _{GS} = 0V		0.82	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 10V, I _F = 5A, di/dt = 300A/μs		10.7		nC
t _{rr}	Reverse Recovery Time			19		ns

THERMAL CHARACTERISTICS

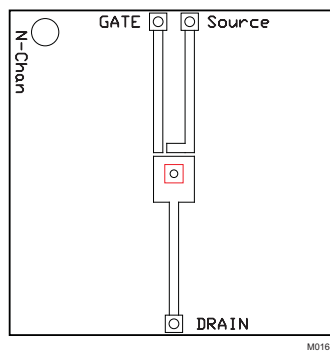
($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			4.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			65	$^\circ\text{C/W}$

- $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch $\times$ 1.5-inch (3.81-cm $\times$ 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 65$ when
mounted on 1 inch²
(6.45 cm²) of 2-oz.
(0.071-mm thick) Cu.



Max $R_{\theta JA} = 235$ when
mounted on minimum
pad area of 2-oz.
(0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

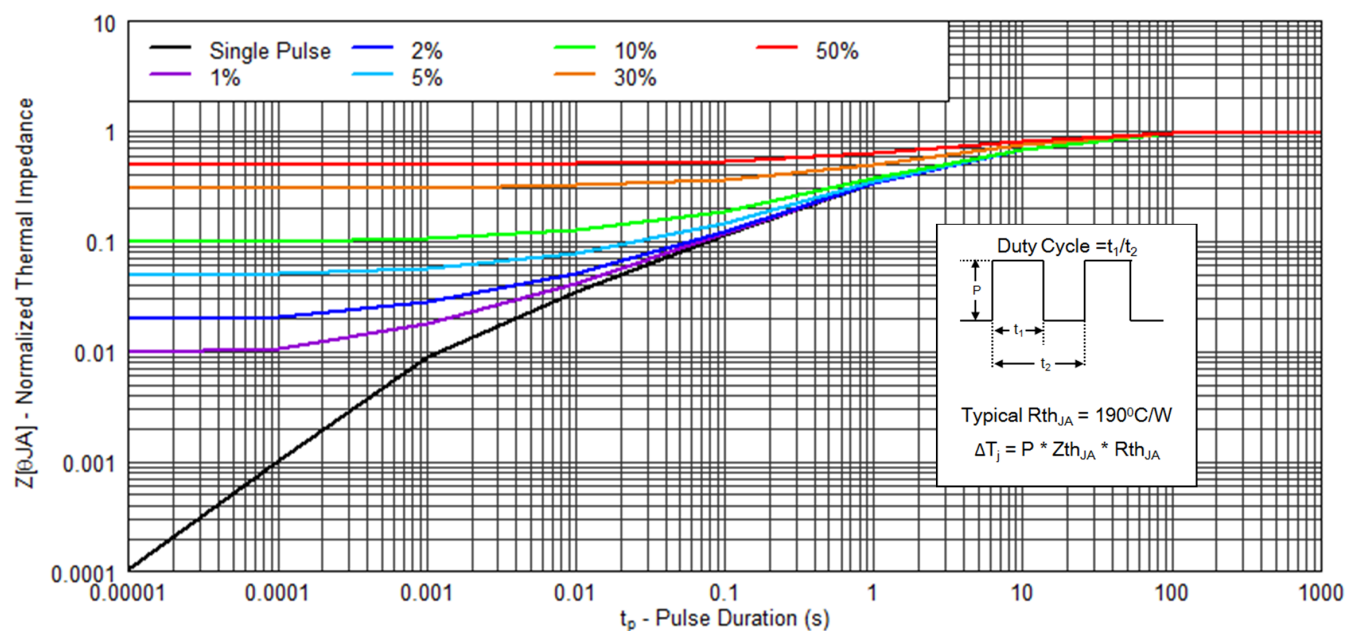


Figure 1. Transient Thermal Impedance

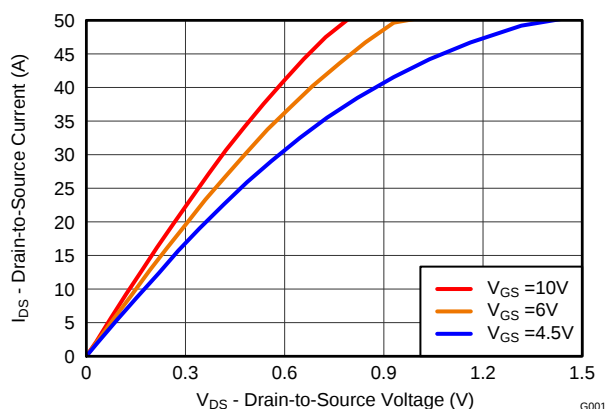


Figure 2. Saturation Characteristics

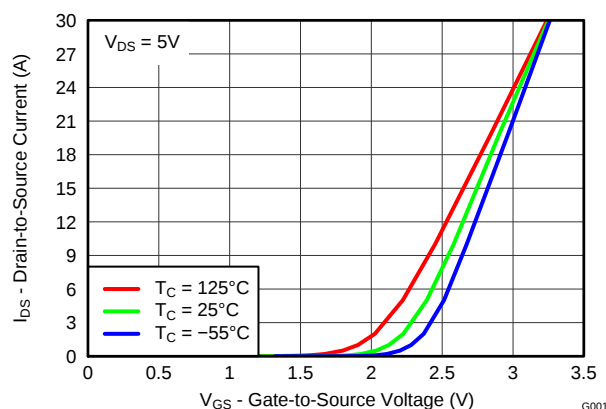
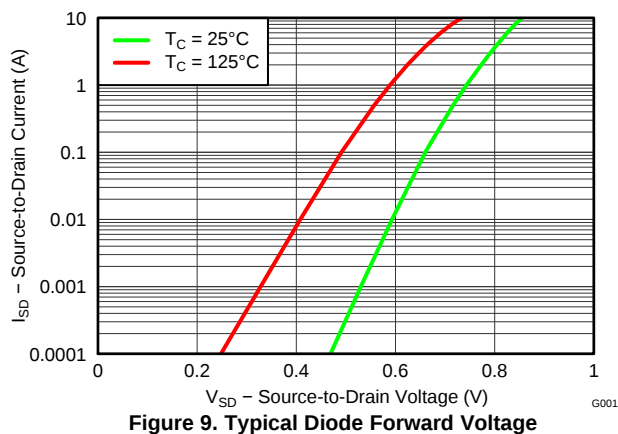
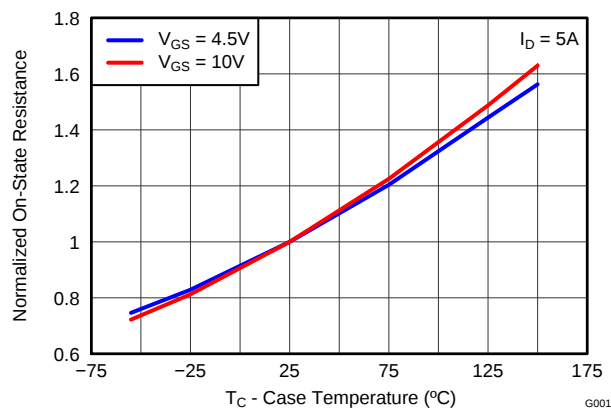
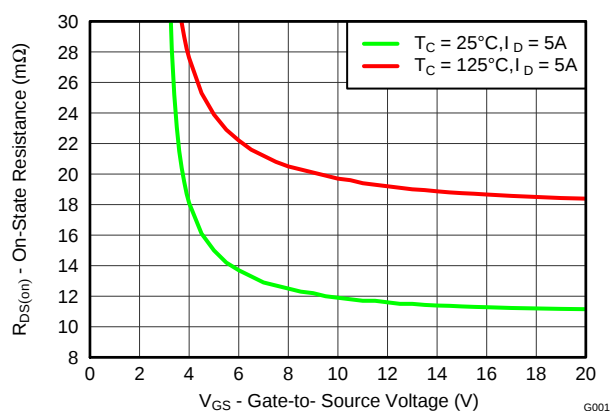
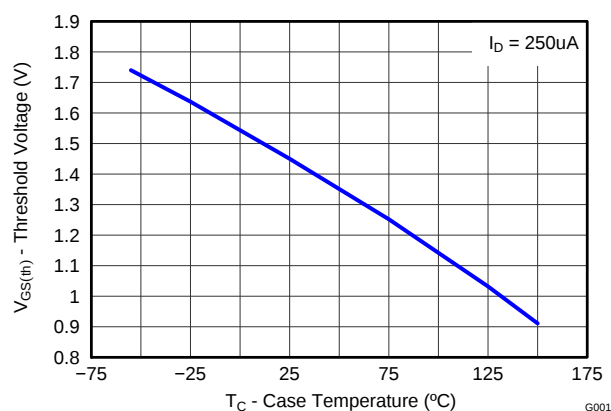
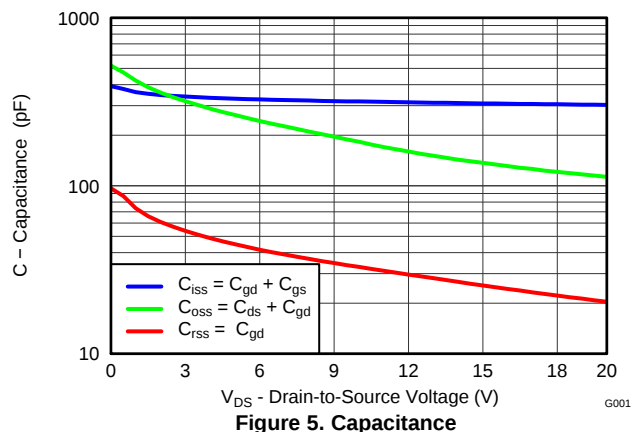
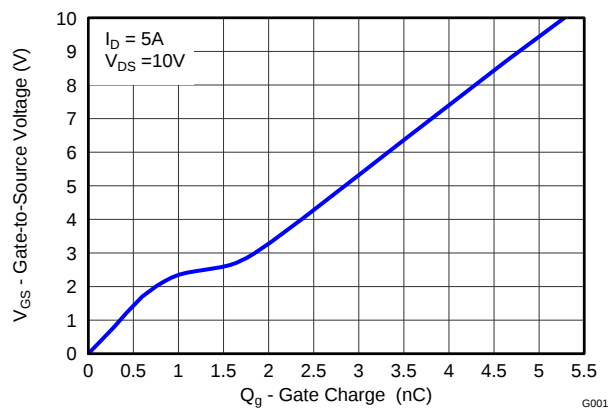


Figure 3. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

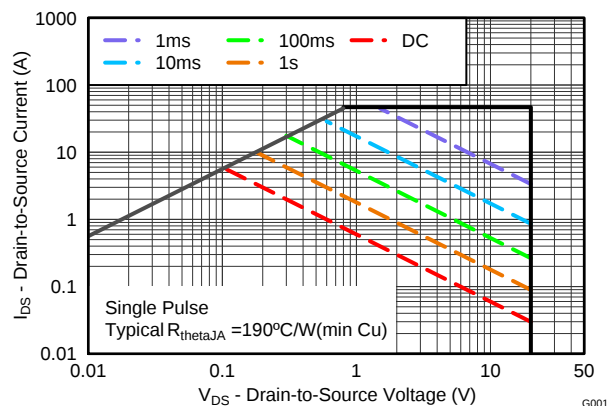


Figure 10. Maximum Safe Operating Area

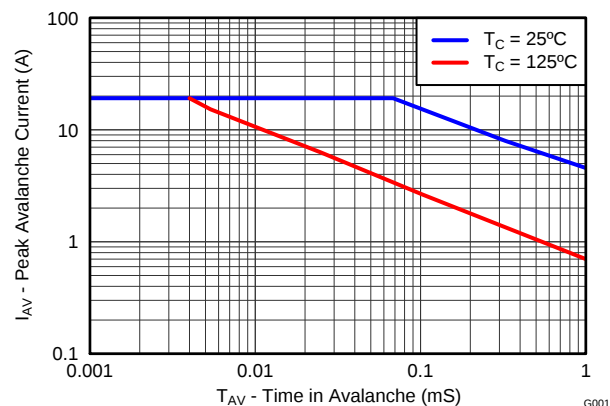


Figure 11. Single Pulse Unclamped Inductive Switching

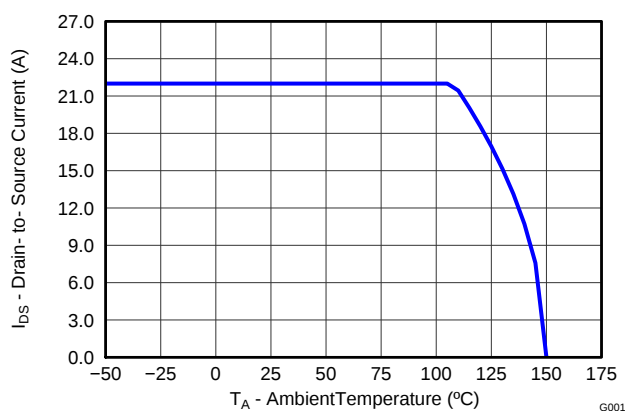
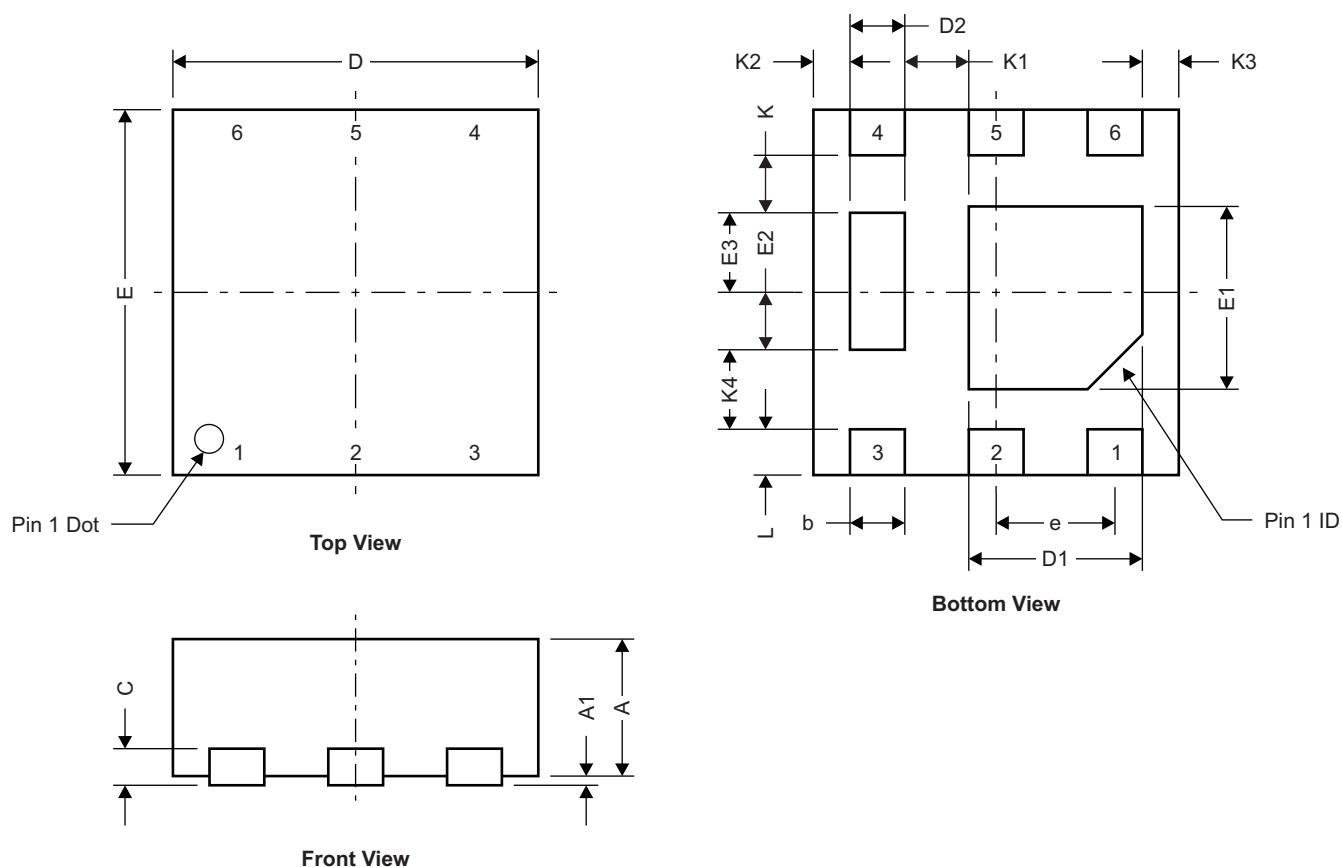


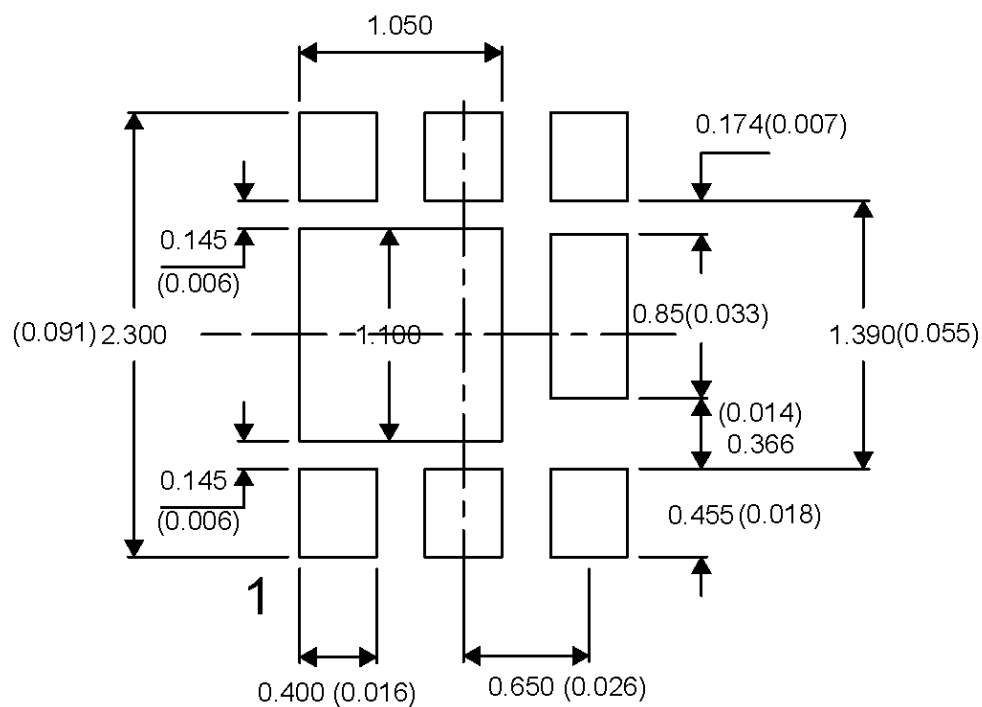
Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA**Q2 Package Dimensions**

M0165-01

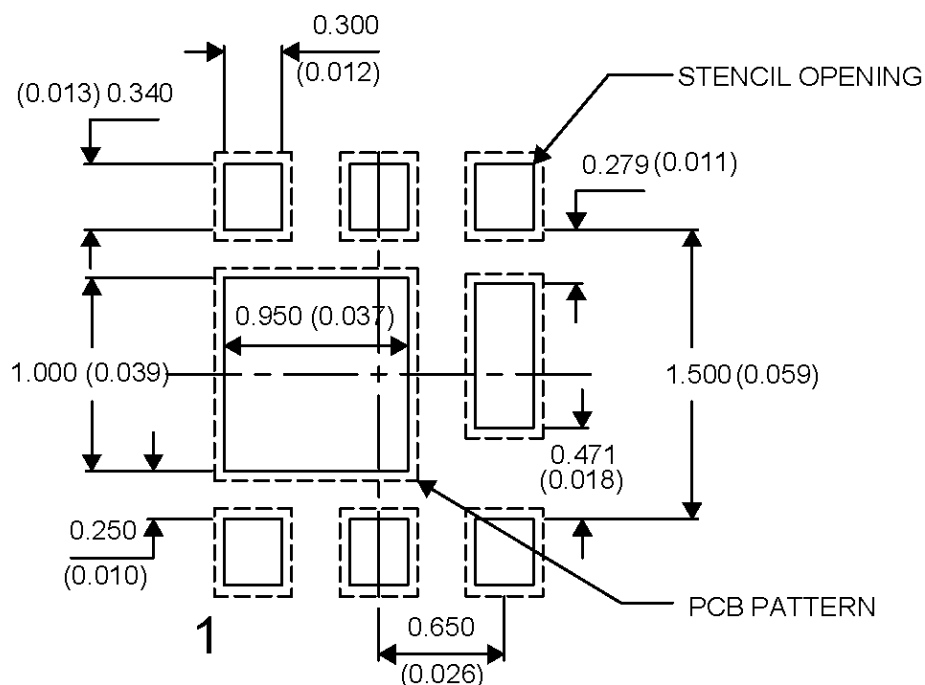
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 BSC			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.012

Recommended PCB Pattern



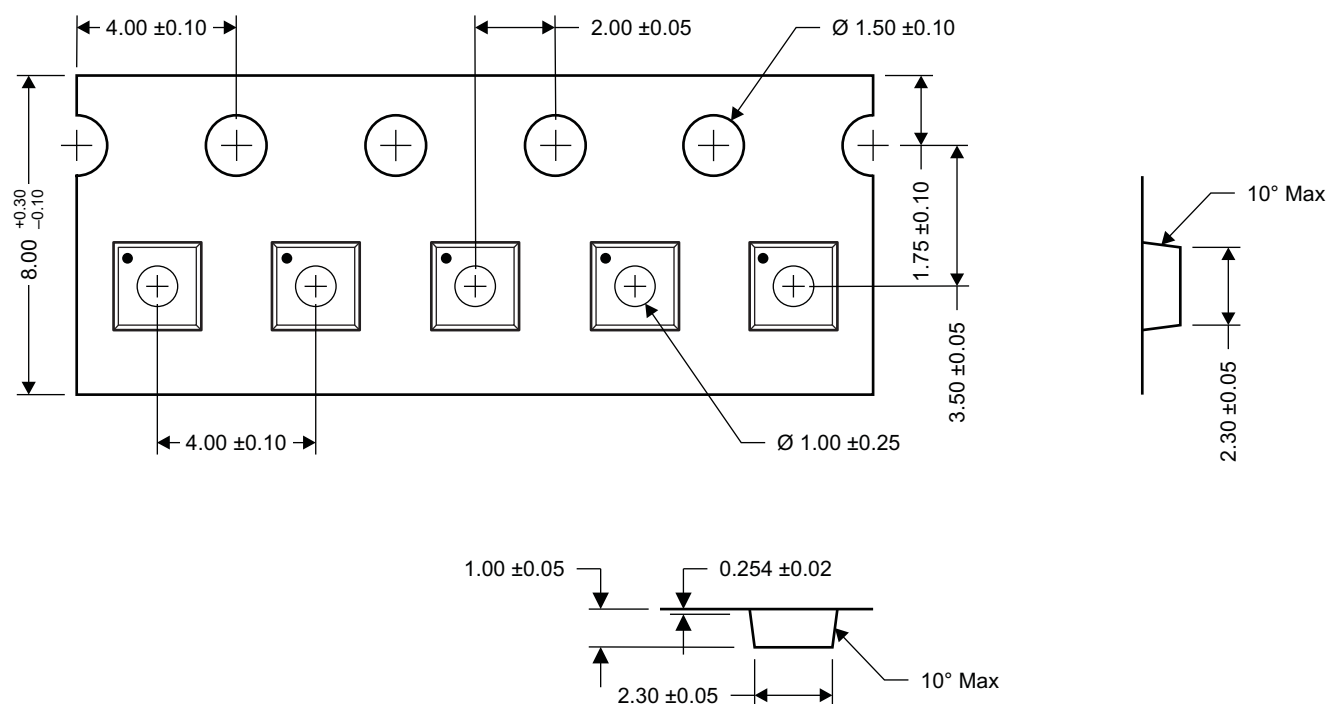
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

Recommended Stencil Pattern



Note: All dimensions are in mm, unless otherwise specified.

Q2 Tape and Reel Information



M0168-01

- Notes:
1. Measured from centerline of sprocket hole to centerline of pocket
 2. Cumulative tolerance of 10 sprocket holes is ± 0.20
 3. Other material available
 4. Typical SR of form tape Max 10^9 OHM/SQ
 5. All dimensions are in mm, unless otherwise specified.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD15571Q2	ACTIVE	WSO	DQK	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 150	1551	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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