



CSD18542KCS 60V N 通道 NexFET™ 功率 MOSFET

1 特性

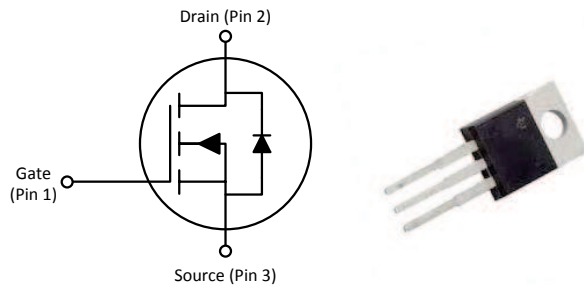
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 逻辑电平
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- 晶体管 (TO)-220 塑料封装

2 应用范围

- 直流 - 直流转换
- 次级侧同步整流器
- 电机控制

3 说明

这款 60V, 3.3mΩ, TO-220 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET) 被设计成在功率转换应用中最大限度地降低功率损耗。



产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源极电压	60		V
Q_g	栅极电荷总量 (10V)	44		nC
Q_{gd}	栅漏栅极电荷	6.9		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	4.0	mΩ
		$V_{GS} = 10\text{V}$	3.3	mΩ
$V_{GS(th)}$	阈值电压	1.8		V

订购信息⁽¹⁾

器件	数量	包装介质	封装	运输
CSD18542KCS	50	管	TO-220 塑料封装	管

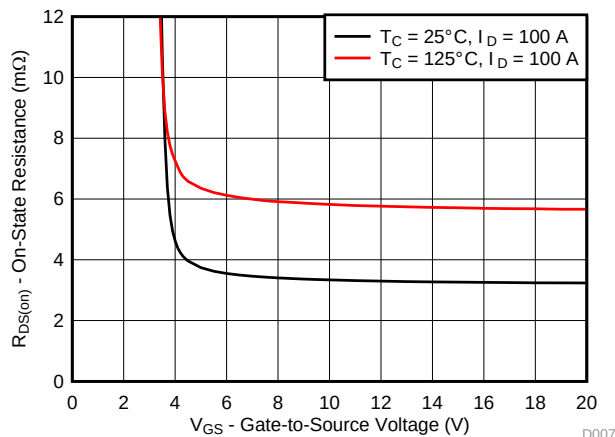
(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

绝对最大额定值

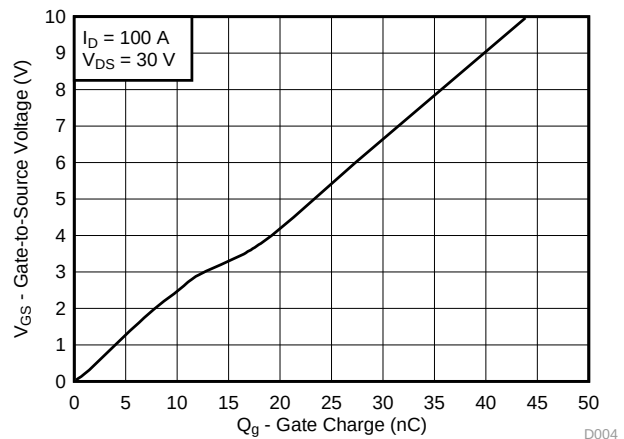
$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源极电压	60	V
V_{GS}	栅源极电压	± 20	V
I_D	持续漏极电流 (受封装限制)	200	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	170	
	持续漏极电流 (受芯片限制), $T_C = 100^\circ\text{C}$ 时测得	120	
I_{DM}	脉冲漏极电流 ⁽¹⁾	400	A
P_D	功率耗散	200	W
T_J , T_{stg}	工作结温, 储存温度	-55 至 175	$^\circ\text{C}$
E_{AS}	雪崩能量, 单一脉冲 $I_D = 75\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	281	mJ

(1) 最大 $R_{\theta JC} = 0.6^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

1	特性	1	5.3	Typical MOSFET Characteristics	4
2	应用范围	1	6	器件和文档支持	7
3	说明	1	6.1	社区资源	7
4	修订历史记录	2	6.2	商标	7
5	Specifications	3	6.3	静电放电警告	7
5.1	Electrical Characteristics	3	6.4	术语表	7
5.2	Thermal Information	3	7	机械、封装和可订购信息	8
			7.1	KCS 封装尺寸	8

4 修订历史记录

日期	修订版本	注释
2015 年 6 月	*	首次发布。

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _D = 250 μA	60			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 48 V			1	μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.5	1.8	2.2	V
R _{DS(on)}	Drain-to-source on-resistance	V _{GS} = 4.5 V, I _D = 100 A		4.0	5.1	mΩ
		V _{GS} = 10 V, I _D = 100 A		3.3	4.0	mΩ
g _{fs}	Transconductance	V _{DS} = 30 V, I _D = 100 A		198		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 30 V, f = 1 MHz		3900	5070	pF
C _{oss}	Output capacitance			570	740	pF
C _{rss}	Reverse transfer capacitance			11	14	pF
R _G	Series gate resistance			1.3	2.6	Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 30 V, I _D = 100 A		21	27	nC
Q _g	Gate charge total (10 V)			44	57	nC
Q _{gd}	Gate charge gate-to-drain			6.9		nC
Q _{gs}	Gate charge gate-to-source			10		nC
Q _{g(th)}	Gate charge at V _{th}			7.3		nC
Q _{oss}	Output charge		V _{DS} = 30 V, V _{GS} = 0 V		63	
t _{d(on)}	Turn on delay time	V _{DS} = 30 V, V _{GS} = 10 V, I _{DS} = 100 A, R _G = 0 Ω		6		ns
t _r	Rise time			5		ns
t _{d(off)}	Turn off delay time			18		ns
t _f	Fall time			21		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 100 A, V _{GS} = 0 V		0.9	1.0	V
Q _{rr}	Reverse recovery charge	V _{DS} = 30 V, I _F = 100 A, di/dt = 300 A/μs		148		nC
t _{rr}	Reverse recovery time			53		ns

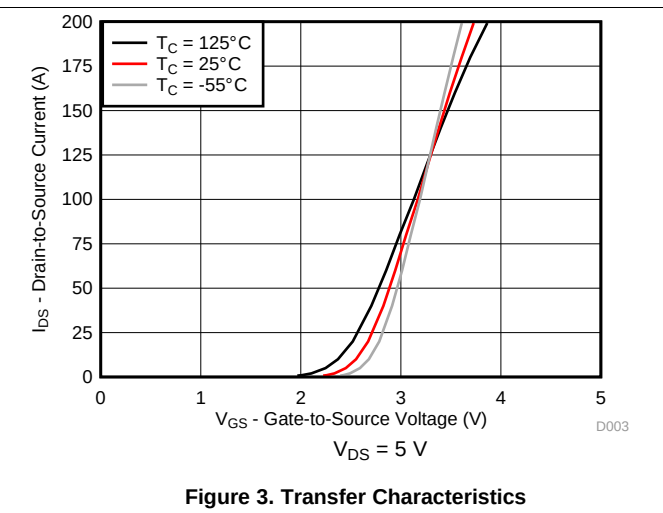
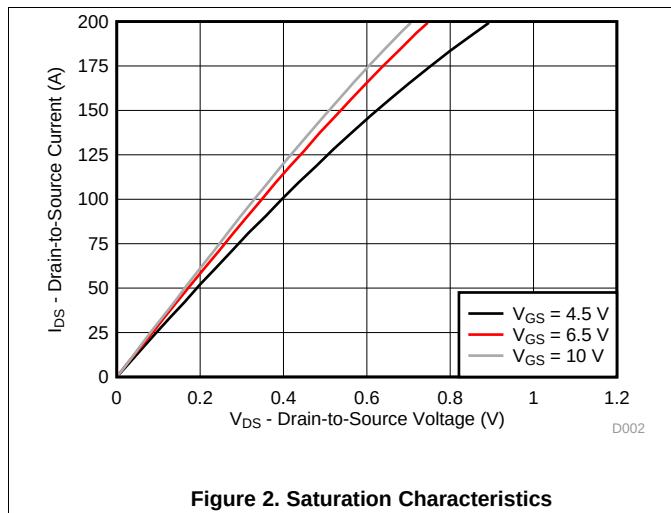
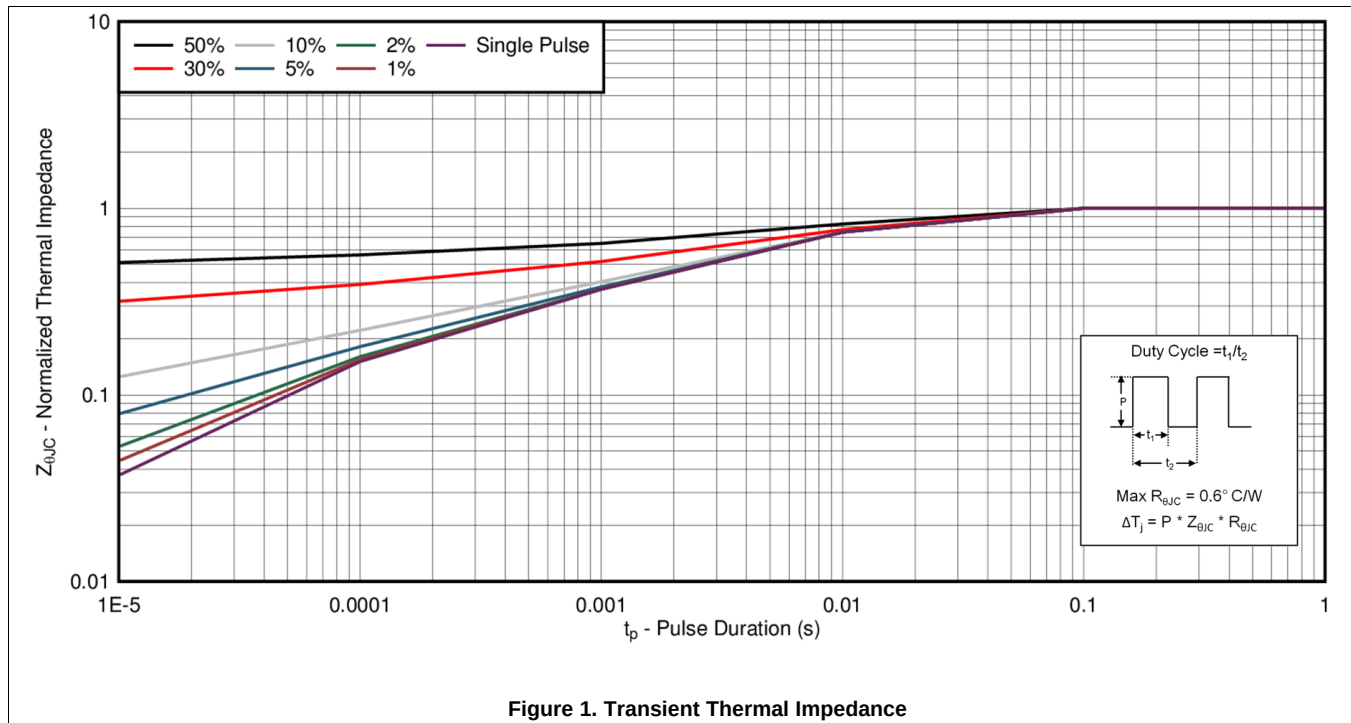
5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.6	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C}/\text{W}$

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

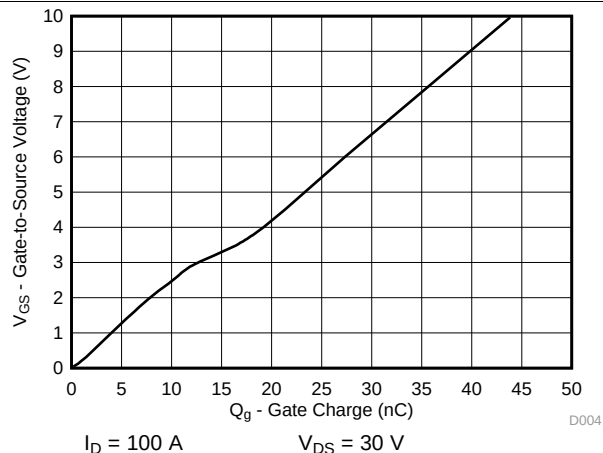


Figure 4. Gate Charge

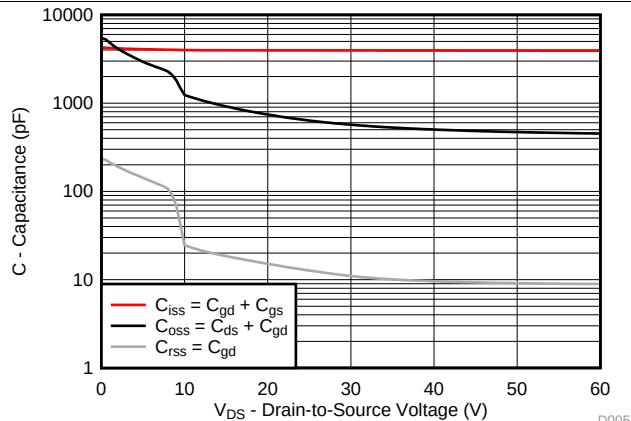


Figure 5. Capacitance

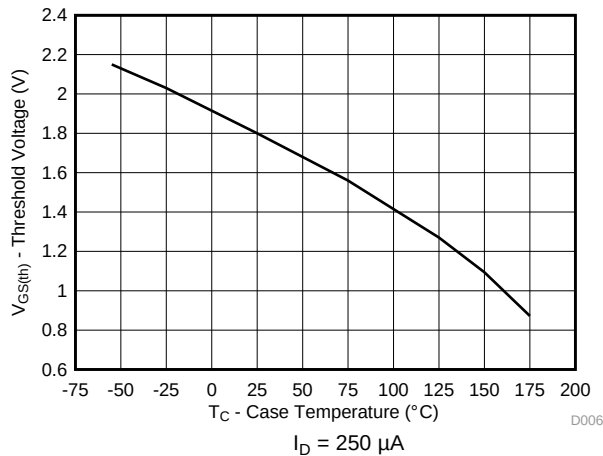


Figure 6. Threshold Voltage vs Temperature

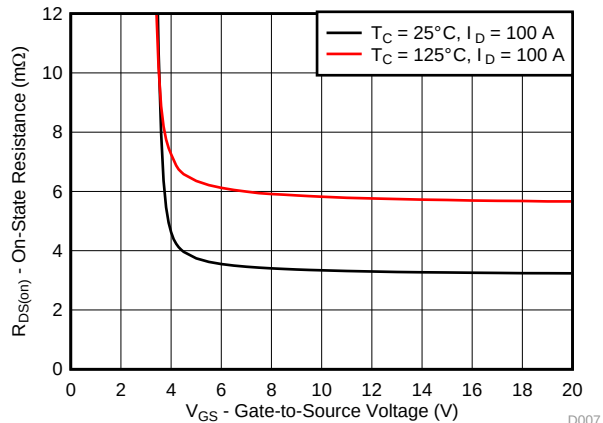


Figure 7. On-State Resistance vs Gate-to-Source Voltage

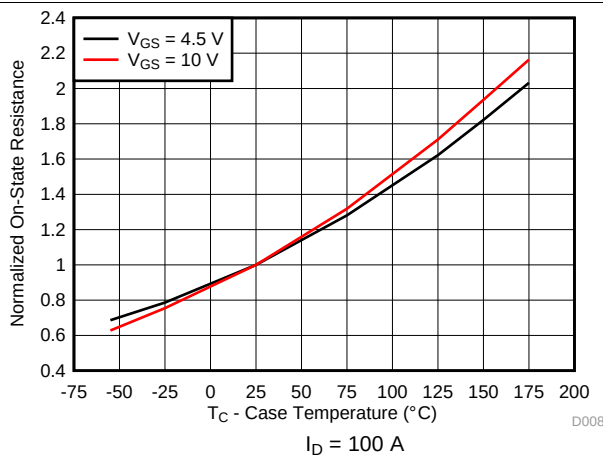


Figure 8. Normalized On-State Resistance vs Temperature

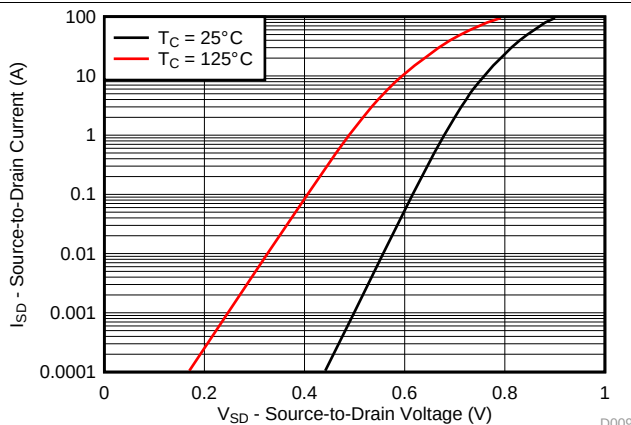


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

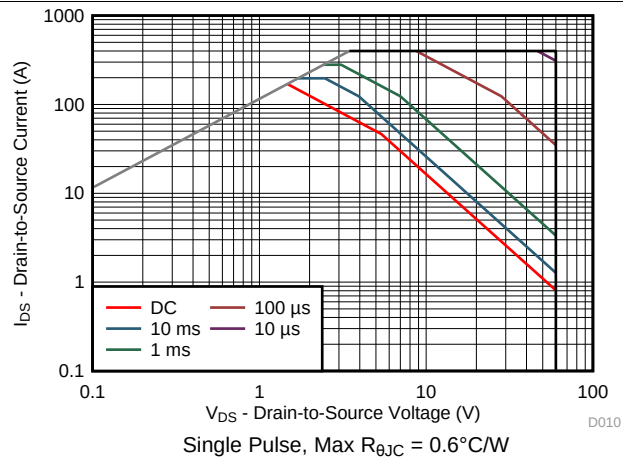


Figure 10. Maximum Safe Operating Area

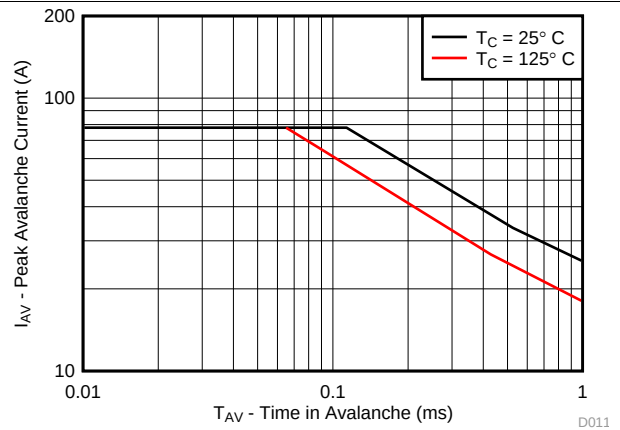


Figure 11. Single Pulse Unclamped Inductive Switching

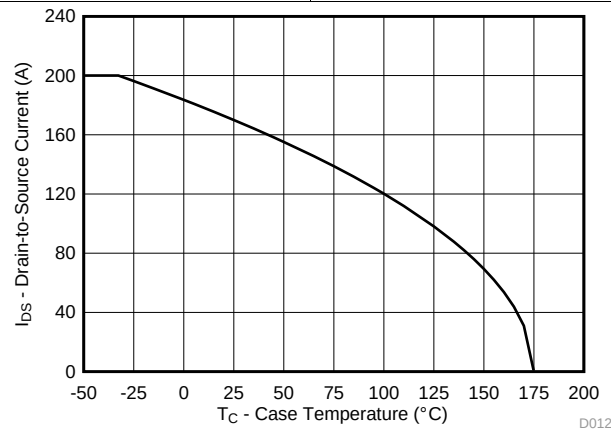


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 商标

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6.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.4 术语表

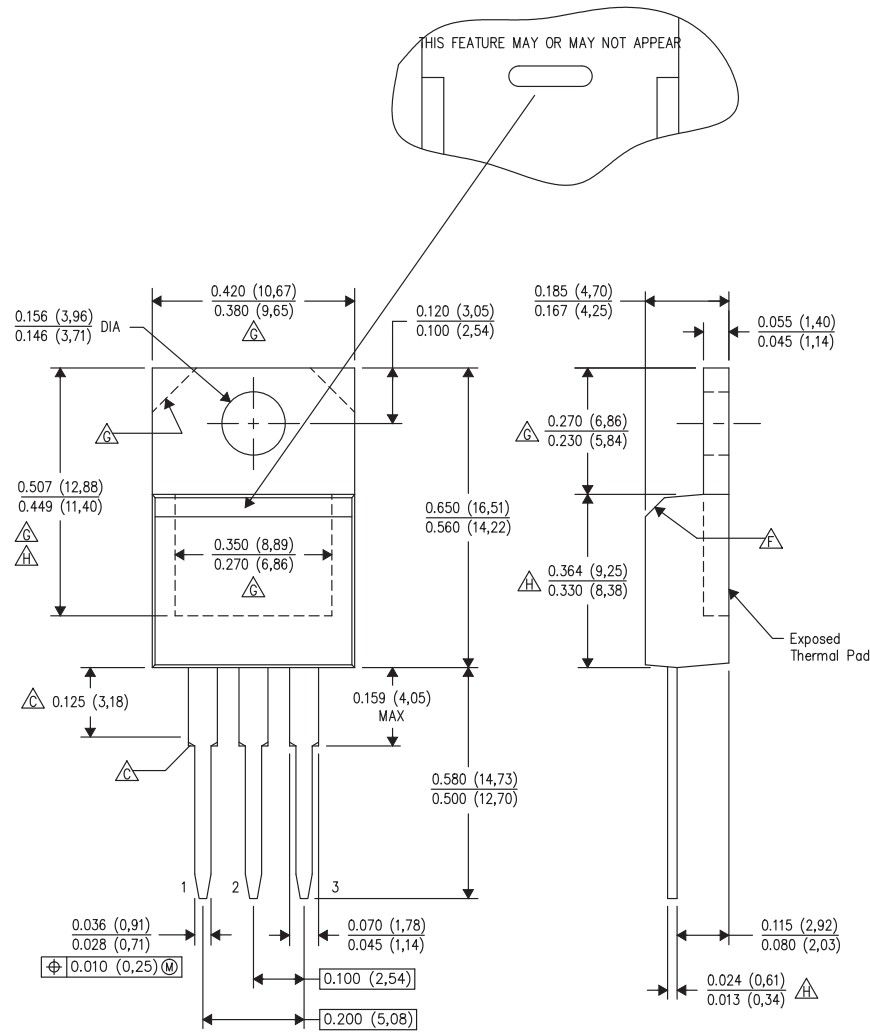
[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

7.1 KCS 封装尺寸



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Lead dimensions are not controlled within this area. Chamfer may or may not appear
 - D. All lead dimensions apply before solder dip.
 - E. The center lead is in electrical contact with the mounting tab.
 - F. The chamfer is optional.
 - G. Thermal pad contour optional within these dimensions.
 - H. Falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

引脚配置

位置	名称
引脚 1	栅极
引脚 2 / 标签	漏极
引脚 3	源极

重要声明

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	产品		应用
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放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com.cn/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com.cn/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18542KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD18542KCS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

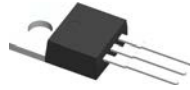
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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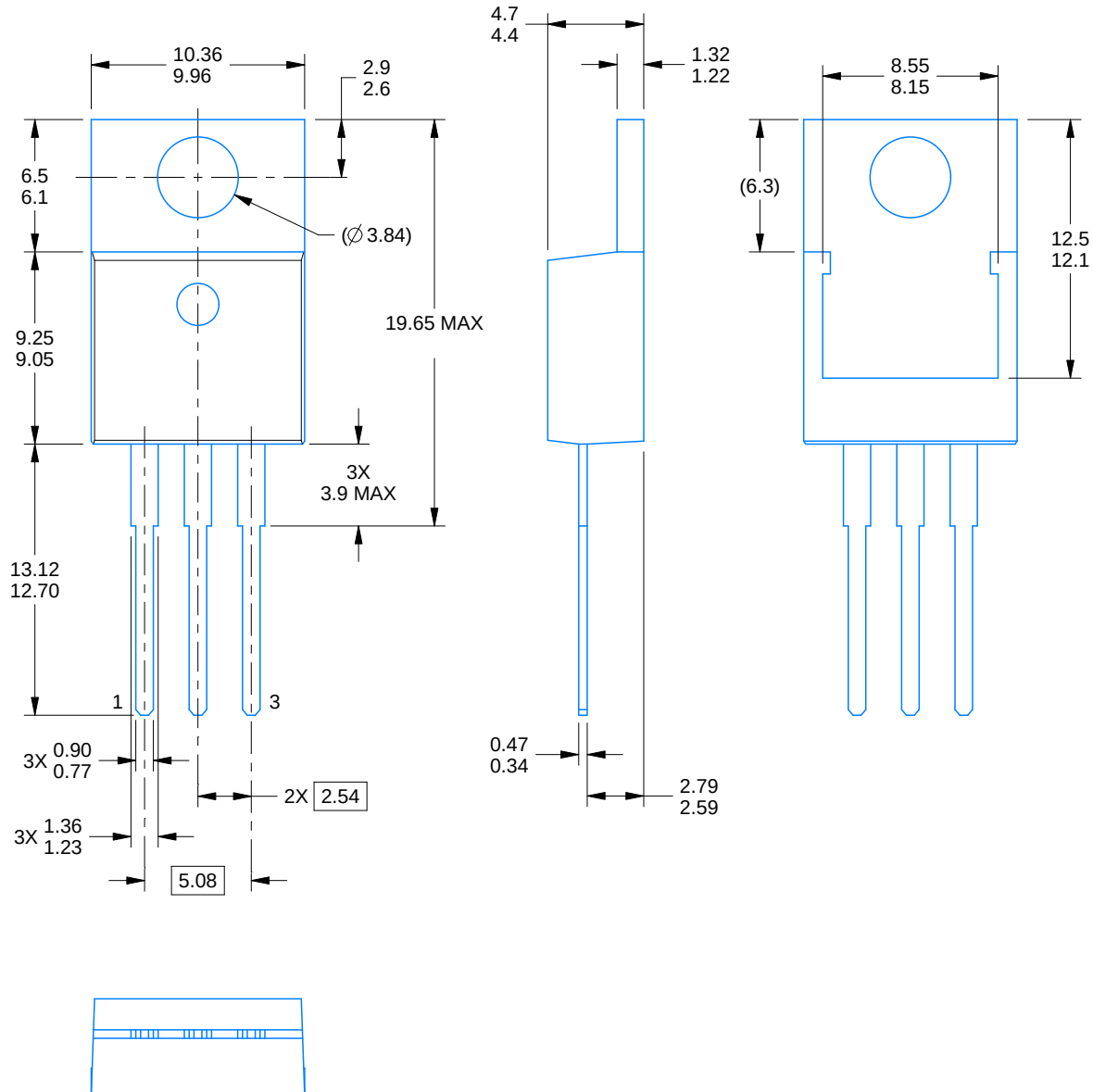


PACKAGE OUTLINE

KCS0003B

TO-220 - 19.65 mm max height

TO-220



4222214/B 08/2018

NOTES:

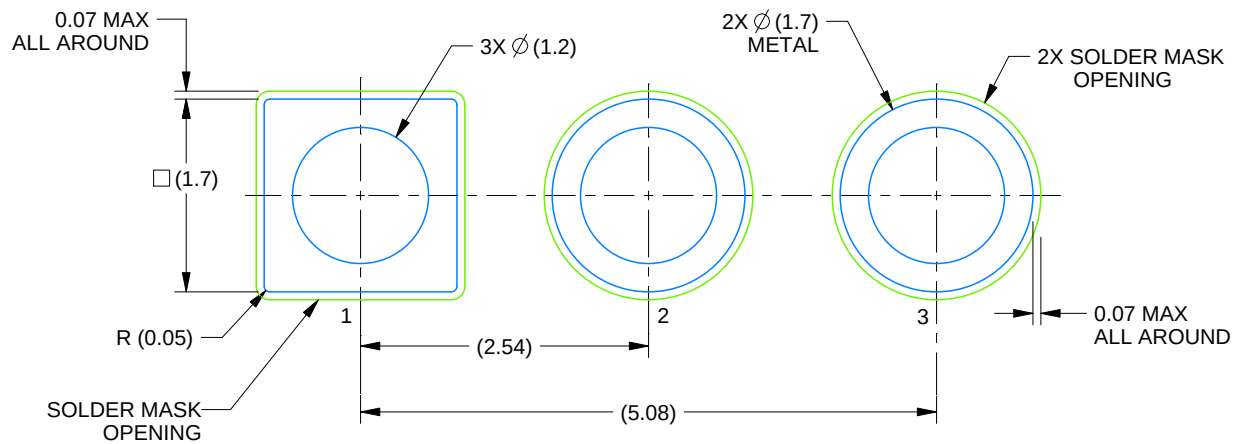
1. Dimensions are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

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