

CSD87355Q5D 同步降压 NexFET™ 电源块

1 特性

- 半桥电源块
- 25A 电流时系统效率达 92.5%
- 工作电流高达 45A
- 高频工作（高达 1.5MHz）
- 高密度 SON 5mm × 6mm 封装
- 针对 5V 栅极驱动进行了优化
- 低开关损耗
- 超低电感封装
- 符合 RoHS 标准
- 无卤素
- 无铅引脚镀层

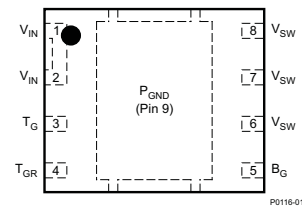
2 应用范围

- 同步降压转换器
 - 高频 应用
 - 高电流、低占空比 应用
- 多相位同步降压转换器
- 负载点 (POL) 直流 - 直流转换器
- IMVP、VRM 和 VRD 电感式触控不锈钢键盘参考设计

3 说明

CSD87355Q5D NexFET™ 电源块是面向同步降压应用的优化设计方案，能够以 5mm × 6mm 的小巧外形提供高电流、高效率以及高频率性能。该产品针对 5V 栅极驱动应用进行了优化，在与外部控制器/驱动器的任一 5V 栅极驱动配套使用时，可提供一套灵活的解决方案来实现高密度电源。

顶视图

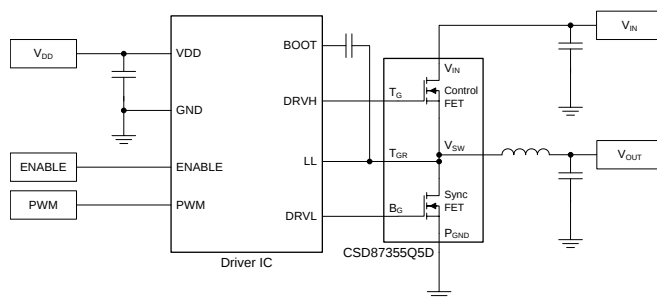


订购信息⁽¹⁾

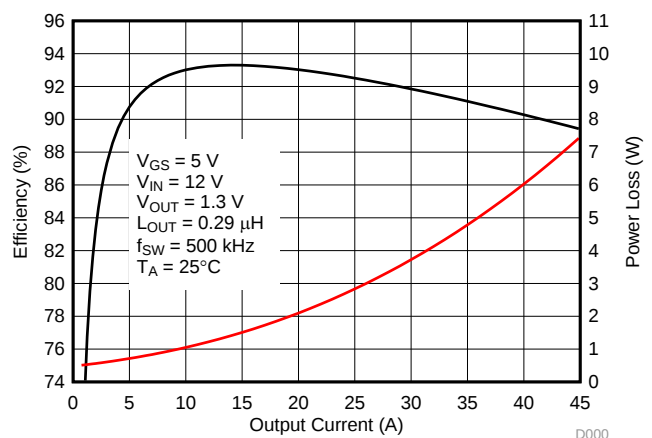
器件	介质	数量	封装	出货
CSD87355Q5D	13 英寸卷带	2500	5mm x 6mm 小外形尺寸无引线 (SON) 塑料封装	卷带
CSD87355Q5DT	7 英寸卷带	250		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

典型电路



典型电源块效率与功率损耗



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4 修订历史记录

Changes from Original (March 2016) to Revision A	Page
• Added footnote for $Z_{DS(ON)}$ in the <i>Electrical Characteristics</i> table.	4
• 已删除 Q5D 卷带封装信息 部分.....	19

5 Specifications

5.1 Absolute Maximum Ratings

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	V_{IN} to P_{GND}	–0.8	30	V
	T_G to T_{GR}	–8	10	V
	B_G to P_{GND}	–8	10	V
Pulsed current rating, I_{DM} ⁽²⁾			120	A
Power dissipation, P_D			12	W
Avalanche energy E_{AS}	Sync FET, $I_D = 89\text{ A}$, $L = 0.1\text{ mH}$		396	mJ
	Control FET, $I_D = 50\text{ A}$, $L = 0.1\text{ mH}$		125	mJ
Operating junction temperature, T_J		–55	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Pulse duration $\leq 50\text{ }\mu\text{s}$. Duty cycle ≤ 0.01 .

5.2 Handling Ratings

	MIN	MAX	UNIT
T_{stg} Storage temperature range	–55	150	$^\circ\text{C}$

5.3 Recommended Operating Conditions

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

	MIN	MAX	UNIT
V_{GS} Gate drive voltage	4.5	10	V
V_{IN} Input supply voltage		27	V
f_{SW} Switching frequency $C_{BST} = 0.1\text{ }\mu\text{F}$ (min)	200	1500	kHz
Operating current		45	A
T_J Operating temperature		125	$^\circ\text{C}$

5.4 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

	THERMAL METRIC	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (min Cu) ⁽¹⁾⁽²⁾			102	$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance (max Cu) ⁽¹⁾⁽²⁾			50	$^\circ\text{C/W}$
$R_{\theta JC}$	Junction-to-case thermal resistance (top of package) ⁽²⁾			20	$^\circ\text{C/W}$
	Junction-to-case thermal resistance (P_{GND} pin) ⁽²⁾			2	$^\circ\text{C/W}$

- (1) Device mounted on FR4 material with 1 inch^2 (6.45 cm^2) Cu.
- (2) $R_{\theta JC}$ is determined with the device mounted on a 1 inch^2 (6.45 cm^2), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inches $\times$ 1.5 inches ($3.81\text{ cm} \times 3.81\text{ cm}$), 0.06 inch (1.52 mm) thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.

5.5 Power Block Performance

 $T_A = 25^\circ\text{C}$ (unless otherwise noted)

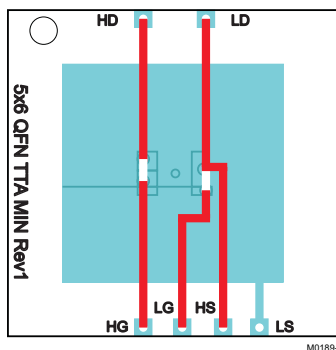
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power loss, P_{LOSS} ⁽¹⁾	$V_{IN} = 12\text{ V}$, $V_{GS} = 5\text{ V}$, $V_{OUT} = 1.3\text{ V}$, $I_{OUT} = 25\text{ A}$, $f_{SW} = 500\text{ kHz}$, $L_{OUT} = 0.29\text{ }\mu\text{H}$, $T_J = 25^\circ\text{C}$		2.8		W
V_{IN} quiescent current, I_{QVIN}	T_G to $T_{GR} = 0\text{ V}$, B_G to $P_{GND} = 0\text{ V}$		10		μA

- (1) Measurement made with six $10\text{ }\mu\text{F}$ (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across V_{IN} to P_{GND} pins and using a high current 5 V driver IC.

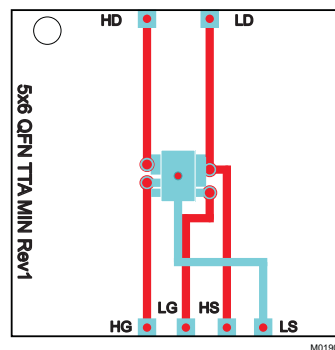
5.6 Electrical Characteristics

 $T_A = 25^{\circ}\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	Q1 CONTROL FET			Q2 SYNC FET			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC CHARACTERISTICS									
BV _{DSS}	Drain-to-source voltage	V _{GS} = 0 V, I _{DS} = 250 μA	30			30			V
I _{DSS}	Drain-to-source leakage current	V _{GS} = 0 V, V _{DS} = 24 V	1			1			μA
I _{GSS}	Gate-to-source leakage current	V _{DS} = 0 V, V _{GS} = +10 / –8 V	100			100			nA
V _{GS(th)}	Gate-to-source threshold voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	1.00 1.90			0.75 1.20			V
Z _{DS(ON)} ⁽¹⁾	Drain-to-source ON impedance	V _{IN} = 12 V, V _{GS} = 5 V, V _{OUT} = 1.3 V, I _{OUT} = 25 A, f _{SW} = 500 kHz, L _{OUT} = 0.29 μH	3.9			0.9			mΩ
g _{fs}	Transconductance	V _{DS} = 3 V, I _{DS} = 20 A	90			151			S
DYNAMIC CHARACTERISTICS									
C _{ISS}	Input capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz	1430 1860			3570 4640			pF
C _{OSS}	Output capacitance		716 930			1730 2240			pF
C _{RSS}	Reverse transfer capacitance		25 32			52 67			pF
R _G	Series gate resistance		0.6 1.2			0.7 1.4			Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 15 V, I _{DS} = 20 A	10.5 13.7			24.3 31.5			nC
Q _{gd}	Gate charge – gate-to-drain		2.3			4.1			nC
Q _{gs}	Gate charge – gate-to-source		3.2			5.6			nC
Q _{g(th)}	Gate charge at V _{th}		1.7			2.8			nC
Q _{OSS}	Output charge	V _{DS} = 15 V, V _{GS} = 0 V	18			40			nC
t _{d(on)}	Turn on delay time	V _{DS} = 15 V, V _{GS} = 4.5 V, I _{DS} = 20 A, R _G = 2 Ω	8			10			ns
t _r	Rise time		18			14			ns
t _{d(off)}	Turn off delay time		13			27			ns
t _f	Fall time		3			6			ns
DIODE CHARACTERISTICS									
V _{SD}	Diode forward voltage	I _{DS} = 20 A, V _{GS} = 0 V	0.8 1.0			0.8 1.0			V
Q _{rr}	Reverse recovery charge	V _{dd} = 17 V, I _F = 20 A, di/dt = 300 A/μs	43			82			nC
t _{rr}	Reverse recovery time		23.8			32.3			ns

(1) Equivalent based on application testing. See [Application and Implementation](#) section for details.


Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2 oz. (0.071-mm thick)
Cu.



Max $R_{\theta JA} = 102^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2 oz. (0.071-mm thick)
Cu.

5.7 Typical Power Block Device Characteristics

$T_J = 125^\circ\text{C}$, unless stated otherwise. The Typical Power Block System Characteristic curves 图 3, , and 图 4 are based on measurements made on a PCB design with dimensions of 4" (W) $\times$ 3.5" (L) $\times$ 0.062" (H) and 6 copper layers of 1-oz. copper thickness. See [Application and Implementation](#) for detailed explanation.

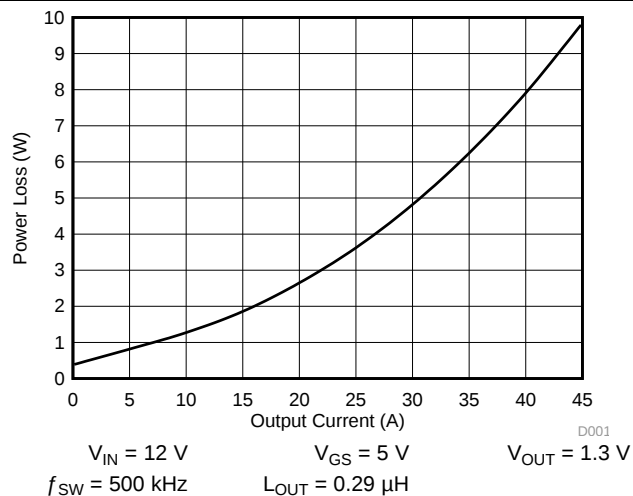


图 1. Power Loss vs Output Current

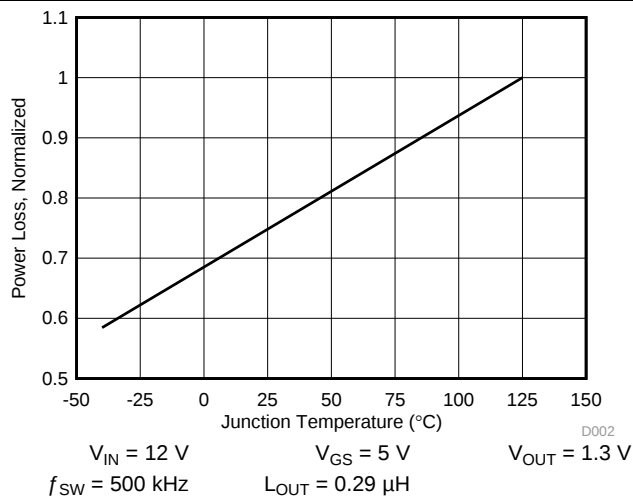


图 2. Normalized Power Loss vs Temperature

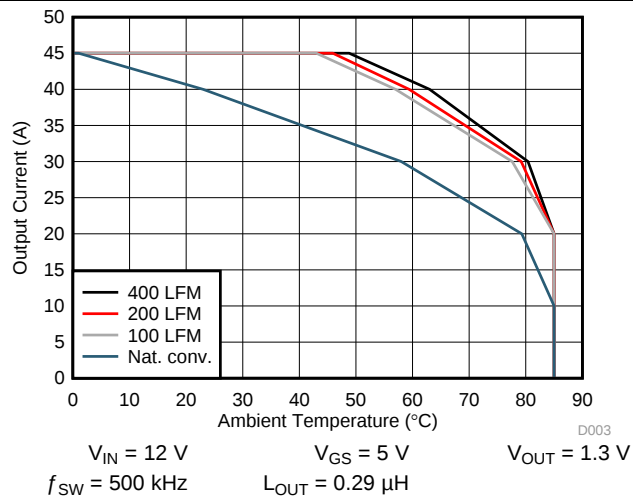


图 3. Safe Operating Area (SOA) – Thermal Airflow Measurement PCB Vertical Mount

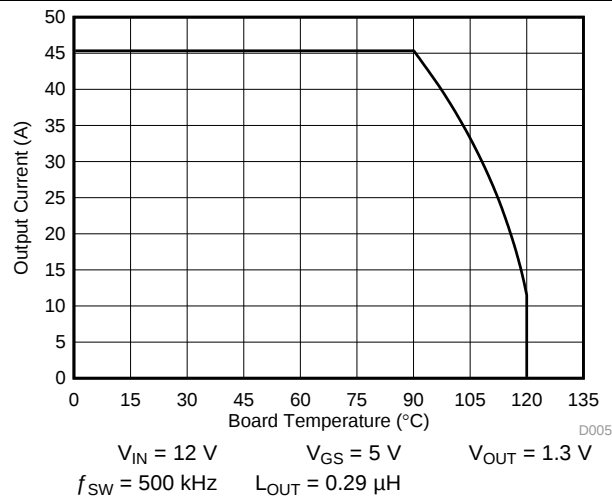
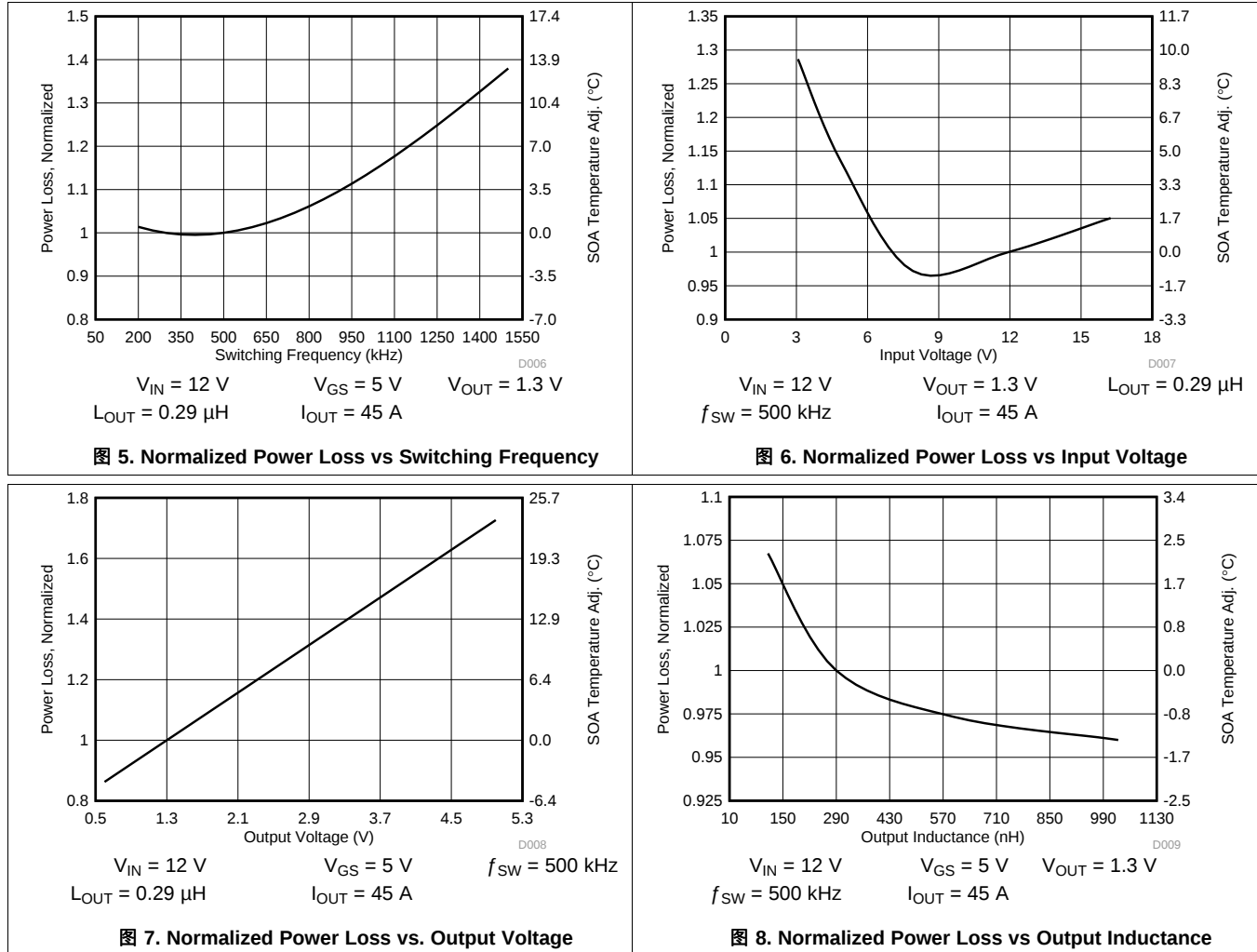


图 4. Typical Safe Operating Area (SOA)

Typical Power Block Device Characteristics (接下页)

$T_J = 125^\circ\text{C}$, unless stated otherwise. The Typical Power Block System Characteristic curves 图 3, , and 图 4 are based on measurements made on a PCB design with dimensions of 4" (W) $\times$ 3.5" (L) $\times$ 0.062" (H) and 6 copper layers of 1-oz. copper thickness. See [Application and Implementation](#) for detailed explanation.



5.8 Typical Power Block MOSFET Characteristics

$T_A = 25^\circ\text{C}$, unless stated otherwise.

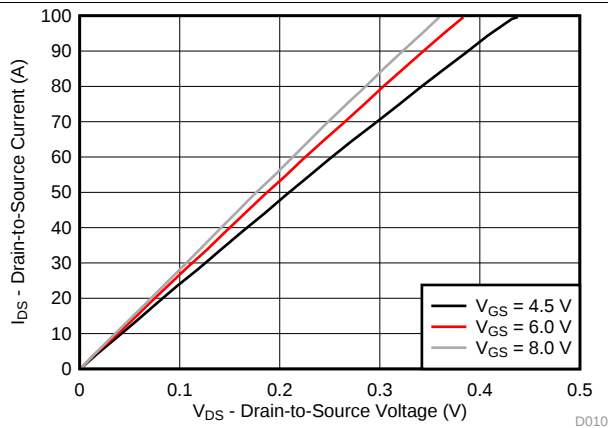


图 9. Control MOSFET Saturation

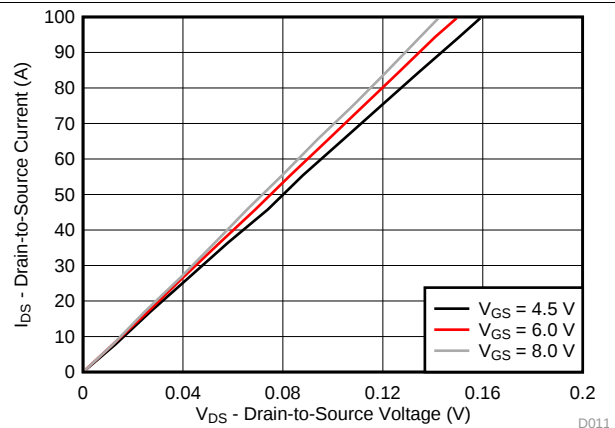


图 10. Sync MOSFET Saturation

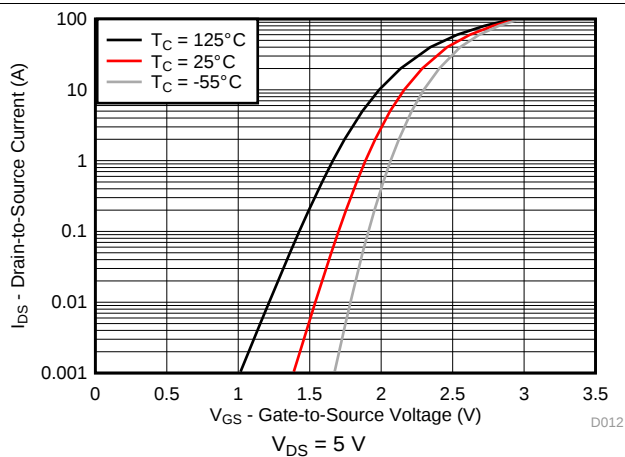


图 11. Control MOSFET Transfer

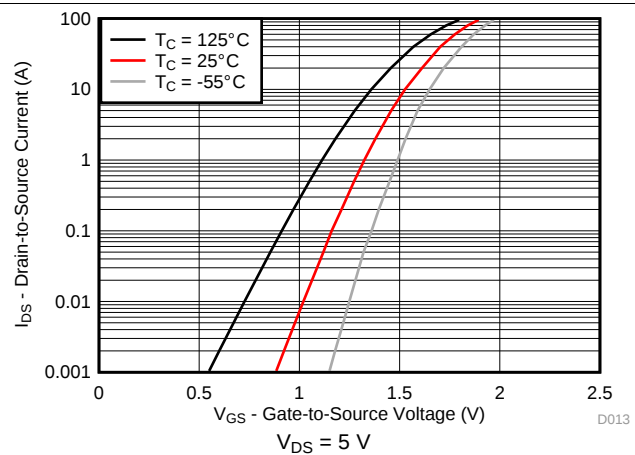


图 12. Sync MOSFET Transfer

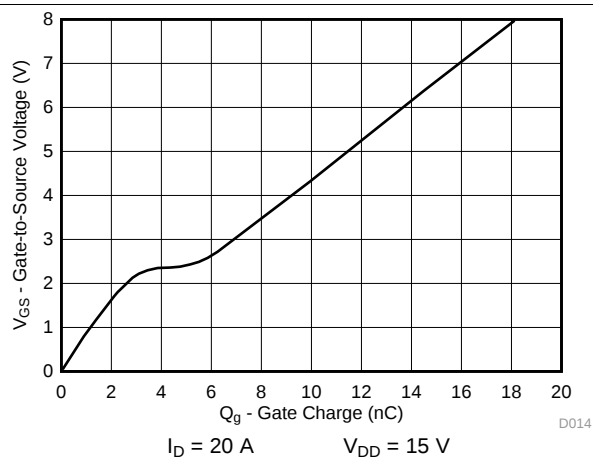


图 13. Control MOSFET Gate Charge

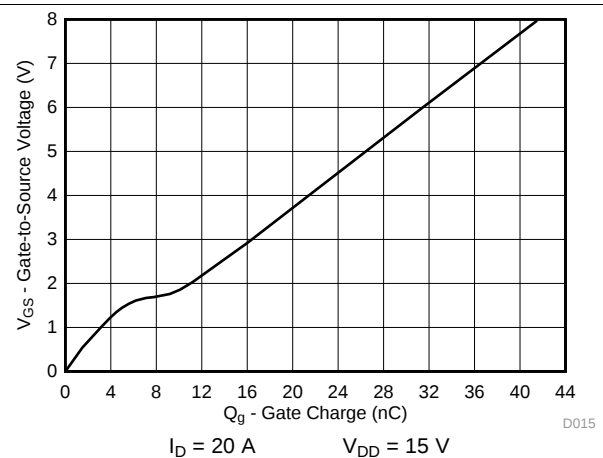


图 14. Sync MOSFET Gate Charge

Typical Power Block MOSFET Characteristics (接下页)

$T_A = 25^\circ\text{C}$, unless stated otherwise.

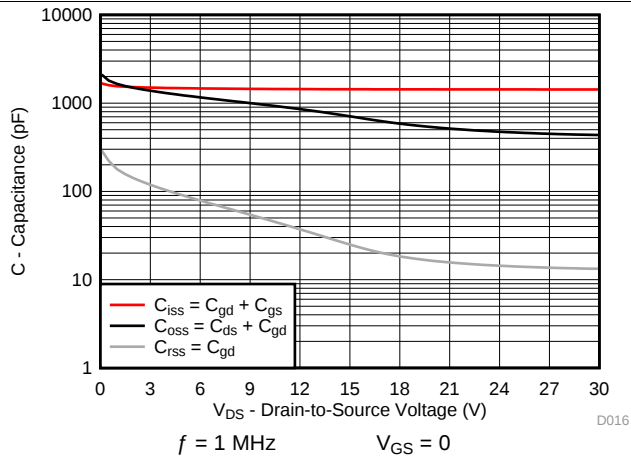


图 15. Control MOSFET Capacitance

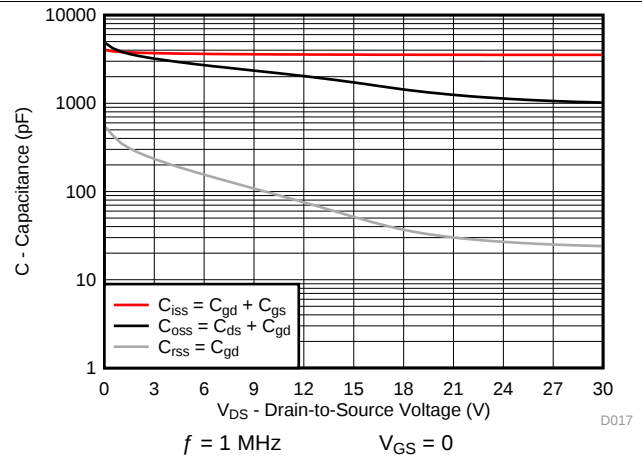


图 16. Sync MOSFET Capacitance

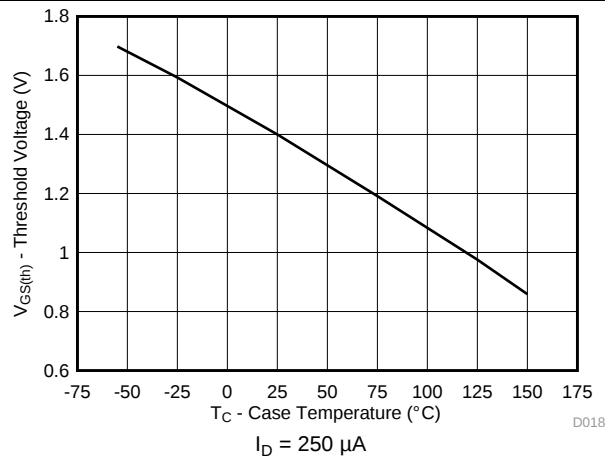


图 17. Control MOSFET $V_{GS(th)}$

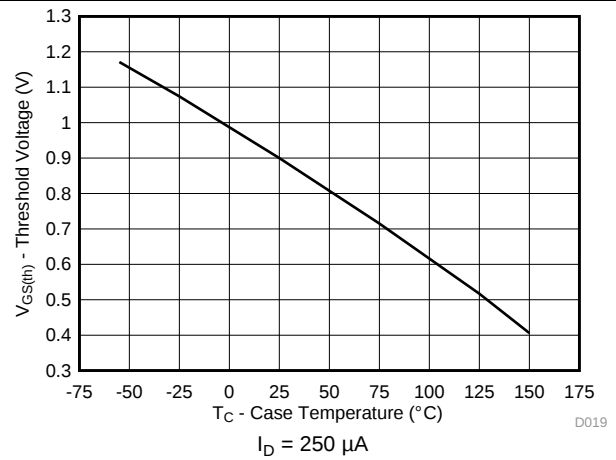


图 18. Sync MOSFET $V_{GS(th)}$

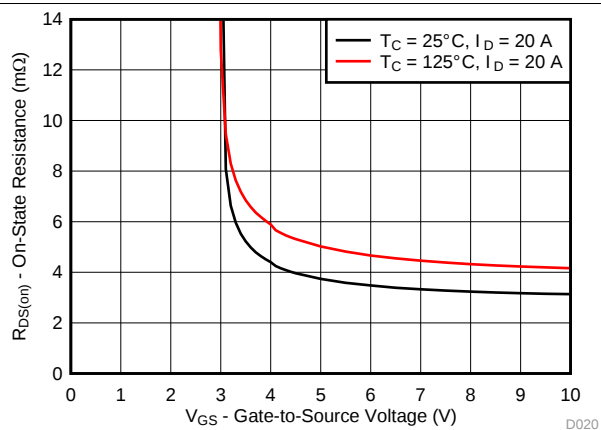


图 19. Control MOSFET $R_{DS(on)}$ vs V_{GS}

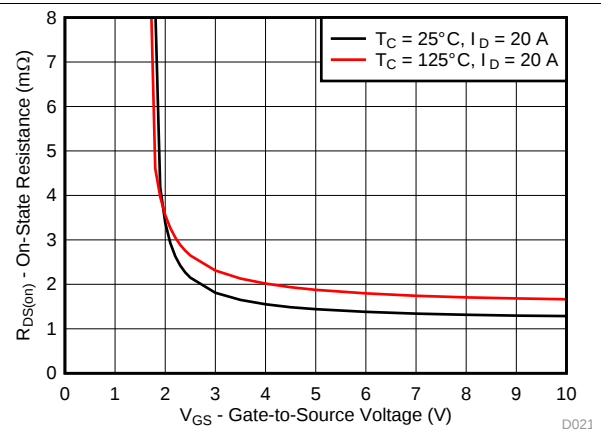


图 20. Sync MOSFET $R_{DS(on)}$ vs V_{GS}

Typical Power Block MOSFET Characteristics (接下页)

$T_A = 25^\circ\text{C}$, unless stated otherwise.

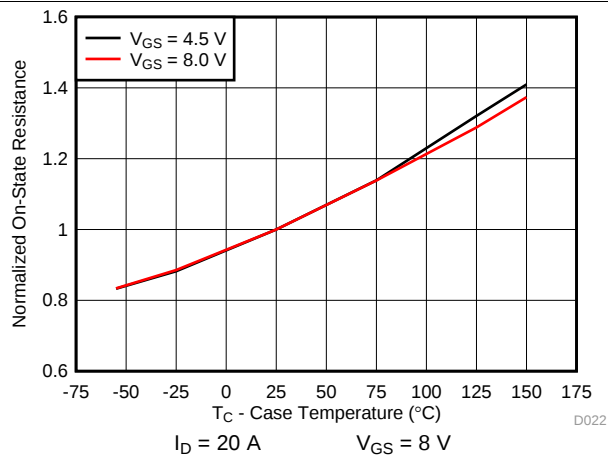


图 21. Control MOSFET Normalized $R_{DS(ON)}$

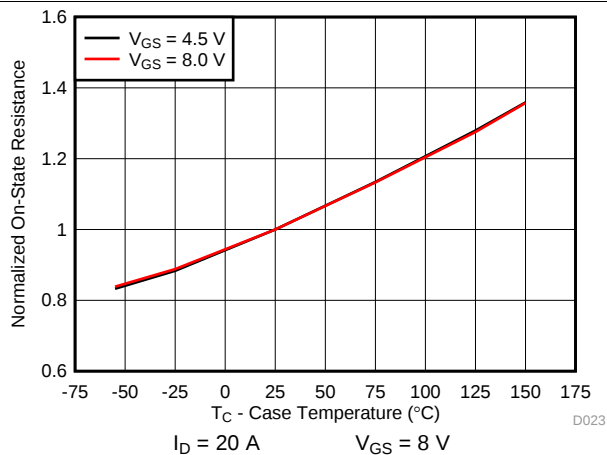


图 22. Sync MOSFET Normalized $R_{DS(ON)}$

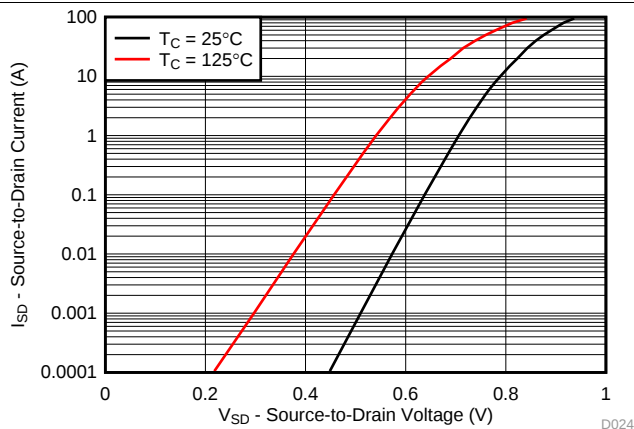


图 23. Control MOSFET Body Diode

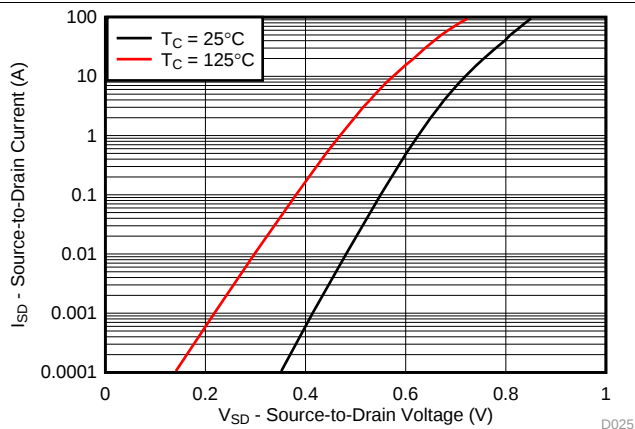


图 24. Sync MOSFET Body Diode

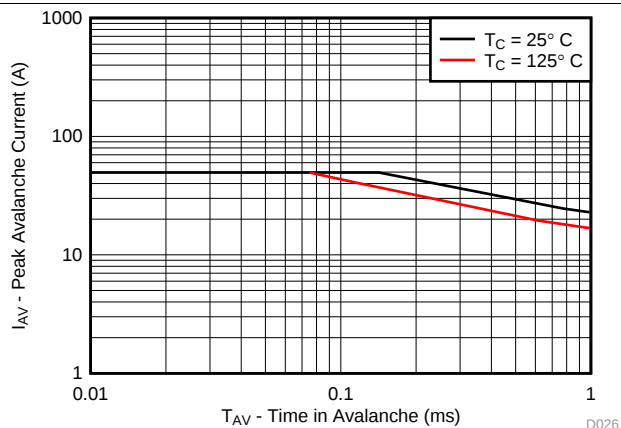


图 25. Control MOSFET Unclamped Inductive Switching

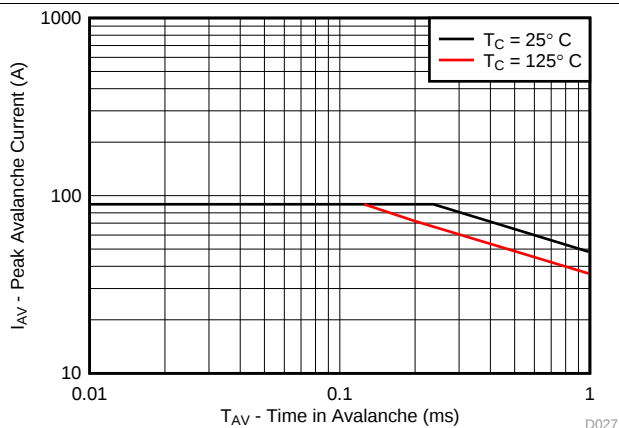


图 26. Sync MOSFET Unclamped Inductive Switching

6 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

6.1 Application Information

The CSD87355Q5D NexFET power block is an optimized design for synchronous buck applications using 5-V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a new rating method is needed which is tailored towards a more systems centric environment. System level performance curves such as Power Loss, Safe Operating Area, and normalized graphs allow engineers to predict the product performance in the actual application.

6.1.1 Equivalent System Performance

Many of today's high performance computing systems require low power consumption in an effort to reduce system operating temperatures and improve overall system efficiency. This has created a major emphasis on improving the conversion efficiency of today's Synchronous Buck Topology. In particular, there has been an emphasis in improving the performance of the critical Power Semiconductor in the Power Stage of this application (see 图 27). As such, optimization of the power semiconductors in these applications, needs to go beyond simply reducing $R_{DS(ON)}$.

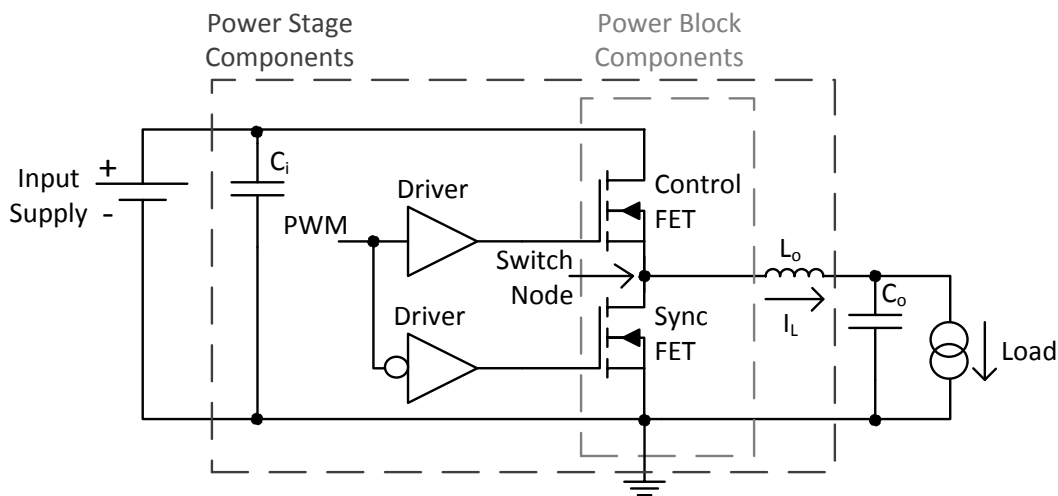


图 27.

Application Information (接下页)

The CSD87355Q5D is part of TI's Power Block product family which is a highly optimized product for use in a synchronous buck topology requiring high current, high efficiency, and high frequency. It incorporates TI's latest generation silicon which has been optimized for switching performance, as well as minimizing losses associated with Q_{GD} , Q_{GS} , and Q_{RR} . Furthermore, TI's patented packaging technology has minimized losses by nearly eliminating parasitic elements between the Control FET and Sync FET connections (see 图 28). A key challenge solved by TI's patented packaging technology is the system level impact of Common Source Inductance (CSI). CSI greatly impedes the switching characteristics of any MOSFET which in turn increases switching losses and reduces system efficiency. As a result, the effects of CSI need to be considered during the MOSFET selection process. In addition, standard MOSFET switching loss equations used to predict system efficiency need to be modified in order to account for the effects of CSI. Further details behind the effects of CSI and modification of switching loss equations are outlined in TI's Application Note [SLPA009](#).

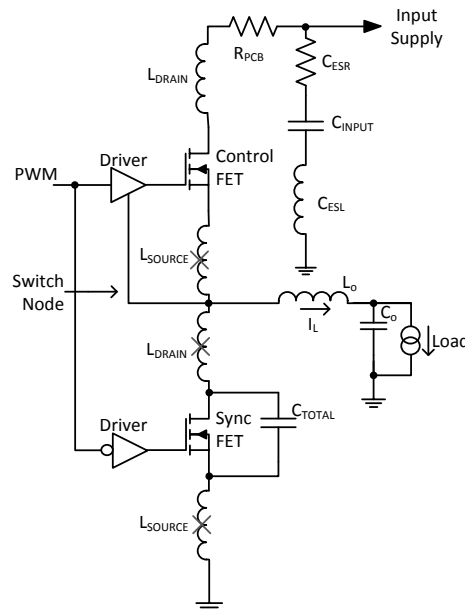


图 28.

The combination of TI's latest generation silicon and optimized packaging technology has created a benchmarking solution that outperforms industry standard MOSFET chipsets of similar $R_{DS(ON)}$ and MOSFET chipsets with lower $R_{DS(ON)}$. 图 29 and 图 30 compare the efficiency and power loss performance of the CSD87355Q5D versus industry standard MOSFET chipsets commonly used in this type of application. This comparison purely focuses on the efficiency and generated loss of the power semiconductors only. The performance of CSD87355Q5D clearly highlights the importance of considering the Effective AC On-Impedance ($Z_{DS(ON)}$) during the MOSFET selection process of any new design. Simply normalizing to traditional MOSFET $R_{DS(ON)}$ specifications is not an indicator of the actual in-circuit performance when using TI's Power Block technology.

Application Information (接下页)

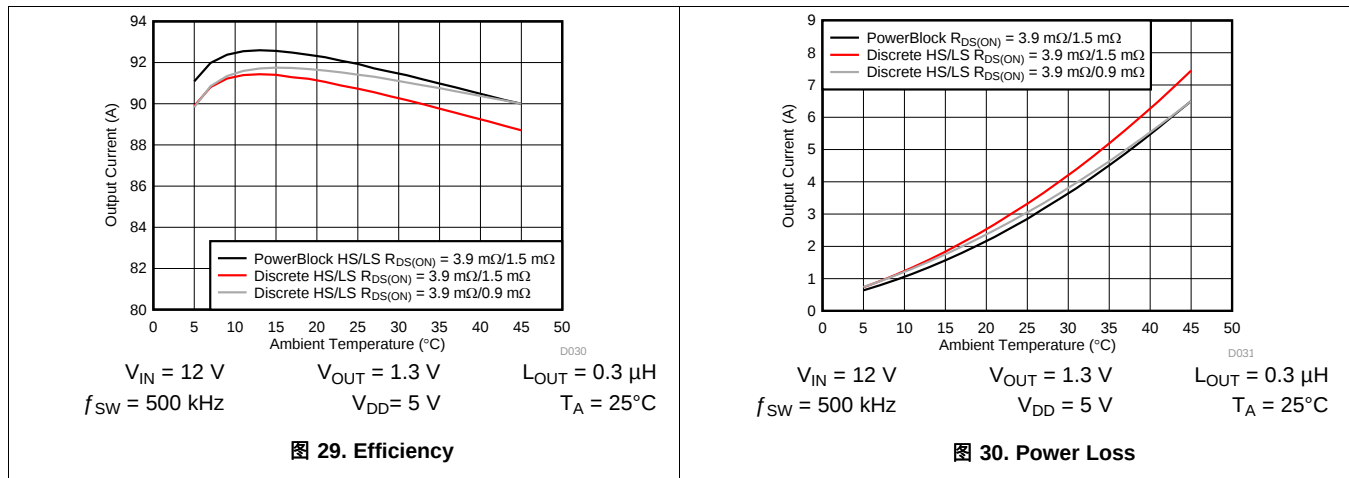


表 1 compares the traditional DC measured $R_{DS(ON)}$ of CSD87355Q5D versus its $Z_{DS(ON)}$. This comparison takes into account the improved efficiency associated with TI's patented packaging technology. As such, when comparing TI's Power Block products to individually packaged discrete MOSFETs or dual MOSFETs in a standard package, the in-circuit switching performance of the solution must be considered. In this example, individually packaged discrete MOSFETs or dual MOSFETs in a standard package would need to have DC measured $R_{DS(ON)}$ values that are equivalent to CSD87355Q5D's $Z_{DS(ON)}$ value in order to have the same efficiency performance at full load. Mid to light-load efficiency will still be lower with individually packaged discrete MOSFETs or dual MOSFETs in a standard package.

表 1. Comparison of $R_{DS(ON)}$ vs $Z_{DS(ON)}$

PARAMETER	HS		LS		UNIT
	TYP	MAX	TYP	MAX	
Effective AC On-Impedance $Z_{DS(ON)}$ ($V_{GS} = 5\text{ V}$)	3.9	-	0.9	-	mΩ
DC Measured $R_{DS(ON)}$ ($V_{GS} = 4.5\text{ V}$)	3.9	4.7	1.5	1.8	mΩ

6.1.2 Power Loss Curves

MOSFET centric parameters such as $R_{DS(ON)}$ and Q_{gd} are needed to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. 图 1 plots the power loss of the CSD87355Q5D as a function of load current. This curve is measured by configuring and running the CSD87355Q5D as it would be in the final application (see 图 31). The measured power loss is the CSD87355Q5D loss and consists of both input conversion loss and gate drive loss. 公式 1 is used to generate the power loss curve.

$$(V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) = \text{Power Loss} \quad (1)$$

The power loss curve in 图 1 is measured at the maximum recommended junction temperatures of 125°C under isothermal test conditions.

6.1.3 Safe Operating Curves (SOA)

The SOA curves in the CSD87355Q5D data sheet provides guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. 图 3 to 图 4 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4" (W) × 3.5" (L) × 0.062" (T) and 6 copper layers of 1-oz. copper thickness.

6.1.4 Normalized Curves

The normalized curves in the CSD87355Q5D data sheet provides guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of system conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change in system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

6.2 Typical Application

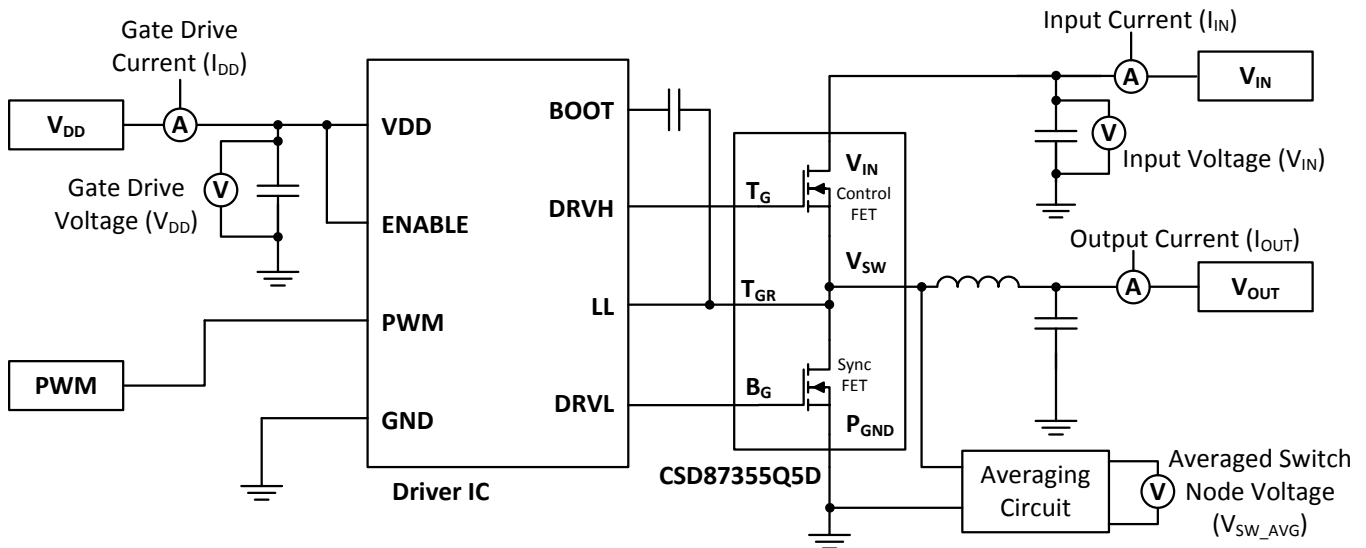


图 31.

Typical Application (接下页)

6.2.1 Design Example: Calculating Power Loss and SOA

The user can estimate product loss and SOA boundaries by arithmetic means (see [Operating Conditions](#)). Though the Power Loss and SOA curves in this data sheet are taken for a specific set of test conditions, the following procedure will outline the steps the user should take to predict product performance for any set of system conditions.

6.2.2 Operating Conditions

- Output Current = 25 A
- Input Voltage = 7 V
- Output Voltage = 1.4 V
- Switching Frequency = 800 kHz
- Inductor = 0.2 μ H

6.2.2.1 Calculating Power Loss

- Power Loss at 25 A = 3.62 W (图 1)
- Normalized Power Loss for input voltage ≈ 0.99 (图 6)
- Normalized Power Loss for output voltage ≈ 1.02 (图 7)
- Normalized Power Loss for switching frequency ≈ 1.06 (图 5)
- Normalized Power Loss for output inductor ≈ 1.03 (图 8)
- **Final calculated Power Loss = $3.62 \text{ W} \times 0.99 \times 1.02 \times 1.06 \times 1.03 \approx 3.99 \text{ W}$**

6.2.2.2 Calculating SOA Adjustments

- SOA adjustment for input voltage $\approx -0.24^\circ\text{C}$ (图 6)
- SOA adjustment for output voltage $\approx 0.63^\circ\text{C}$ (图 7)
- SOA adjustment for switching frequency $\approx 2.12^\circ\text{C}$ (图 5)
- SOA adjustment for output inductor $\approx 0.91^\circ\text{C}$ (图 8)
- **Final calculated SOA adjustment = $-0.24 + 0.63 + 2.12 + 0.91 \approx 3.42^\circ\text{C}$**

In the previous design example, the estimated power loss of the CSD87355Q5D would increase to 4 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 3.4°C . 图 32 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 3.4°C . In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.

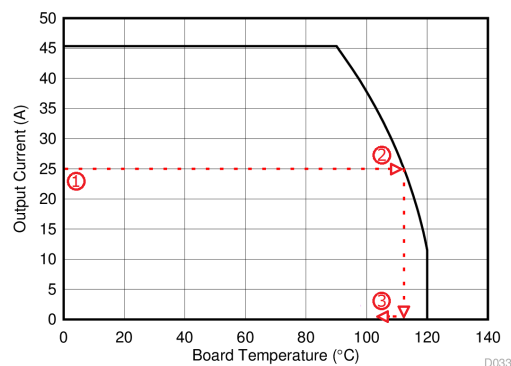


图 32. Power Block SOA

7 Layout

7.1 Layout Guidelines

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. The following sections provide a brief description on how to address each parameter.

7.1.1 Electrical Performance

The Power Block has the ability to switch voltages at rates greater than 10 kV/μs. Take special care with the PCB layout design and placement of the input capacitors, Driver IC, and output inductor.

- The placement of the input capacitors relative to the Power Block's VIN and PGND pins should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, ceramic input capacitors need to be placed as close as possible to the VIN and PGND pins (see [Figure 33](#)). The example in [Figure 33](#) uses 6 × 10-μF ceramic capacitors (TDK Part # C3216X5R1C106KT or equivalent). Notice there are ceramic capacitors on both sides of the board with an appropriate amount of vias interconnecting both layers. In terms of priority of placement next to the Power Block, C5, C7, C19, and C8 should follow in order.
- The Driver IC should be placed relatively close to the Power Block Gate pins. T_G and B_G should connect to the outputs of the Driver IC. The T_{GR} pin serves as the return path of the high-side gate drive circuitry and should be connected to the Phase pin of the IC (sometimes called LX, LL, SW, PH, etc.). The bootstrap capacitor for the Driver IC will also connect to this pin.
- The switching node of the output inductor should be placed relatively close to the Power Block VSW pins. Minimizing the node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level.
- In the event the switch node waveform exhibits ringing that reaches undesirable levels, the use of a Boost Resistor or RC snubber can be an effective way to reduce the peak ring level. The recommended Boost Resistor value will range between 1 Ω to 4.7 Ω depending on the output characteristics of Driver IC used in conjunction with the Power Block. The RC snubber values can range from 0.5 Ω to 2.2 Ω for the R and 330 pF to 2200 pF for the C. Refer to TI App Note [SLUP100](#) for more details on how to properly tune the RC snubber values. The RC snubber should be placed as close as possible to the Vsw node and PGND see [Figure 33](#).⁽¹⁾

7.1.2 Thermal Considerations

The Power Block has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in [Figure 33](#) uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

8 器件和文档支持

8.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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8.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.4 Glossary

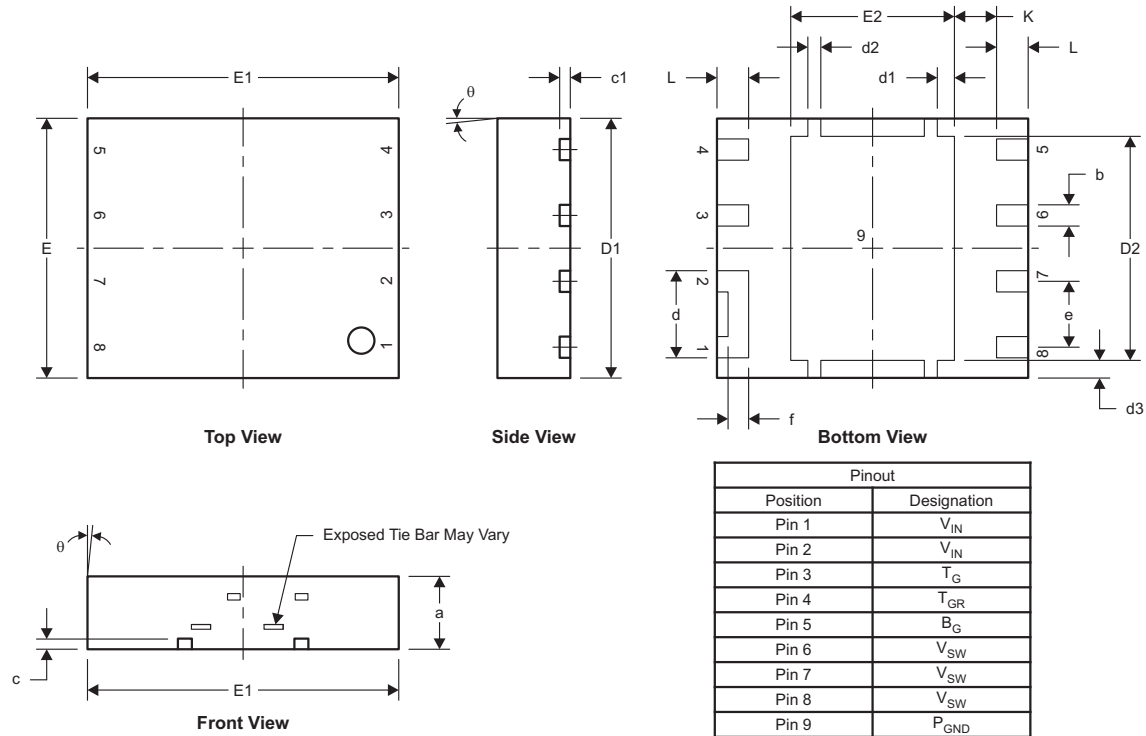
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

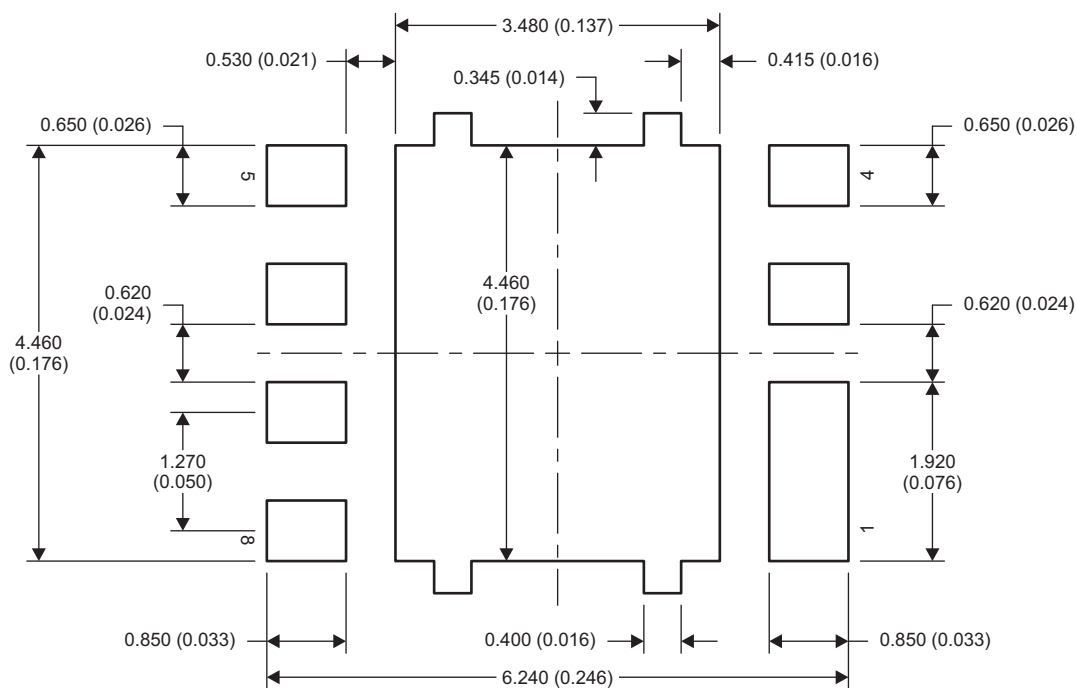
9.1 Q5D 封装尺寸



M0187-01

DIM	毫米		英寸	
	最小值	最大值	最小值	最大值
a	1.40	1.5	0.055	0.059
b	0.360	0.460	0.014	0.018
c	0.150	0.250	0.006	0.010
c1	0.150	0.250	0.006	0.010
d	1.630	1.730	0.064	0.068
d1	0.280	0.380	0.011	0.015
d2	0.200	0.300	0.008	0.012
d3	0.291	0.391	0.012	0.015
D1	4.900	5.100	0.193	0.201
D2	4.269	4.369	0.168	0.172
E	4.900	5.100	0.193	0.201
E1	5.900	6.100	0.232	0.240
E2	3.106	3.206	0.122	0.126
e	1.27 典型值		0.050	
f	0.396	0.496	0.016	0.020
L	0.510	0.710	0.020	0.028
θ	0.00	—	—	—
K	0.812		0.032	

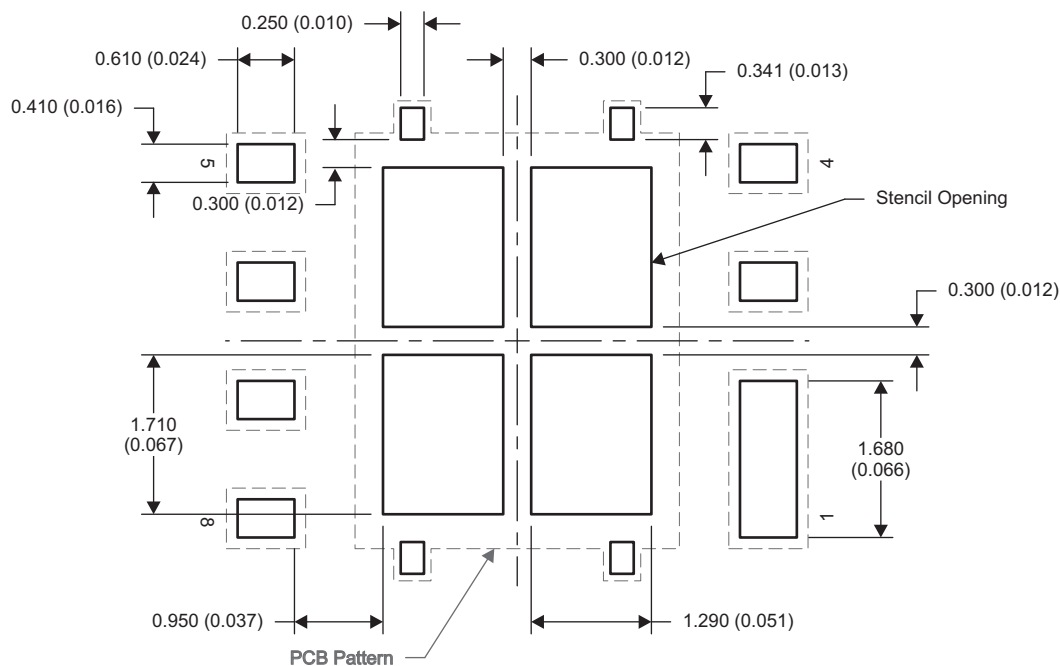
9.2 焊盘布局建议



M0188-01

NOTE: 尺寸单位为 mm (英寸)。

9.3 模板建议



M0208-01

NOTE: 尺寸单位为 mm (英寸)。

如需了解针对 PCB 设计的建议电路布局，请参阅应用手册 [SLPA005](#) – 《通过 PCB 布局技巧来减少振铃》。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87355Q5D	ACTIVE	LSON-CLIP	DQY	8	2500	RoHS-Exempt & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D	Samples
CSD87355Q5DT	ACTIVE	LSON-CLIP	DQY	8	250	RoHS-Exempt & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	87355D	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87355Q5D	LSON-CLIP	DQY	8	2500	330.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2
CSD87355Q5DT	LSON-CLIP	DQY	8	250	180.0	12.4	5.3	6.3	1.8	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87355Q5D	LSON-CLIP	DQY	8	2500	367.0	367.0	35.0
CSD87355Q5DT	LSON-CLIP	DQY	8	250	182.0	182.0	20.0

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