配备铜缆和光纤接口的 **DP83869HM** 高抗扰性 **10/100/1000** 以太网物理层收发器

1 特性

- 多种工作模式
  - 支持媒介：铜缆和光纤
  - 可在铜缆和光纤之间进行切换
  - 在 RGMII 与 SGMII 之间建立桥接
- 最高环境温度 125ºC
- 超过了 8kV IEC61000-4-2 ESD
- 低 RGMII 延迟
  - 对于 1000Base-T，总延迟 ≤ 384ns
  - 对于 100Base-TX，总延迟 ≤ 361ns
- 低功耗
  - 对于 1000Base-X，< 150mW
  - 对于 1000Base-T，< 500mW
- 符合时间敏感网络 (TSN) 标准
- 适用于 SyncE 的恢复时钟输出
- 可选同步时钟输出：25MHz 和 125MHz
- 1000Base-X、100Base-FX 与 SFP MSA 规范兼容
- 通过 SFD 支持 IEEE1588
- 支持局域网唤醒
- 可配置的 IO 电压：1.8V、2.5V 和 3.3V
- SGMII、RGMII、MII MAC 接口
- 巨型帧支持 1000M 和 100M 速度
- 电缆诊断
  - TDR
  - BIST
- 可编程 RGMII 终端阻抗
- 集成 MDI 终端电阻器
- 快速链路丢弃模式
- 与 IEEE 802.3 1000Base-T、100Base-TX、10Base-Te、1000Base-X、100Base-FX 兼容

2 应用

- 工业工厂自动化
- 电网基础设施
- 电机和运动控制
- 测试和测量
- 楼宇自动化

3 说明

DP83869HM 器件是一款集成了 PMD 子层的稳健耐用型全功能千兆位物理层 (PHY) 收发器，支持 10BASE-Te、100BASE-TX 和 1000BASE-T 以太网协议。DP83869 还支持 1000BASE-X 和 100BASE-FX 光纤协议。DP83869HM 经优化可提供 ESD 保护，超过了 8kV IEC 61000-4-2 标准（直接接触）。该器件通过简化 GMII (RGMII) 和 SGMII 连接到 MAC 层。在 100M 模式中，该器件允许设计人员使用 MII 以实现低延迟。RGMII/MII 上的可编程集成终端阻抗有助于降低系统 BOM。

DP83869HM 支持托管模式下的媒介转换。在此模式下，DP83869HM 可以运行 1000BASE-X 至 1000BASE-T 和 100BASE-FX 至 100BASE-TX 转换。

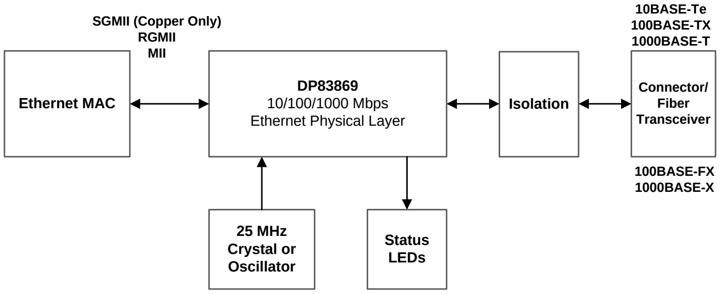
DP83869HM 还支持从 RGMII 到 SGMII 和从 SGMII 到 RGMII 的桥接转换。DP83869HM 符合 TSN 标准，可实现低延迟。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
DP83869HM	VQFN (48)	7.00mm × 7.00mm

[1] 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

标准以太网系统方框图



English Data Sheet: SNLS614

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2018) to Revision A	**Page**
• 将器件状态从“预告信息”更改成了“生产数据”	1

5 （说明 （续））

DP83869HM 还可为 MAC 生成 IEEE 1588 同步帧检测指示。这样可以减少时间同步中的抖动，并帮助系统解决数据包传输和接收中的不对称延迟。

标准以太网系统方框图显示在第一页上。设计人员还可以在媒介转换器模式、RGMII 到 SGMII 桥接 应用以及 SGMII-RGMII 桥接 应用中使用 DP83869。

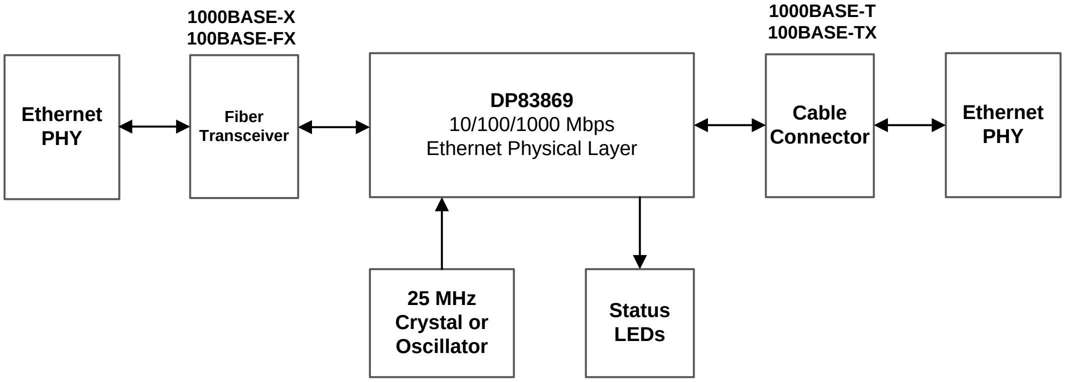


图 **1.** 媒介转换器系统方框图

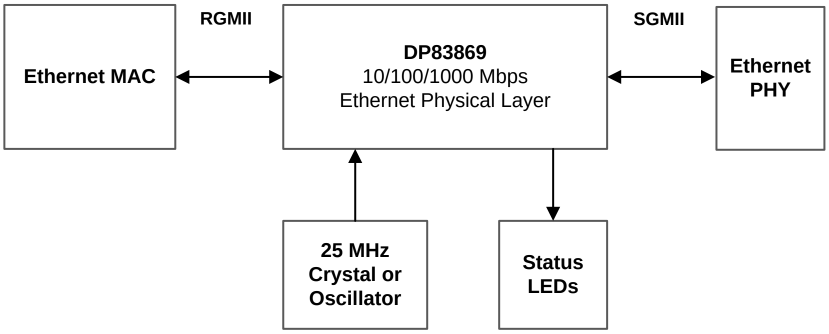


图 **2. RGMII-SGMII** 桥接系统方框图

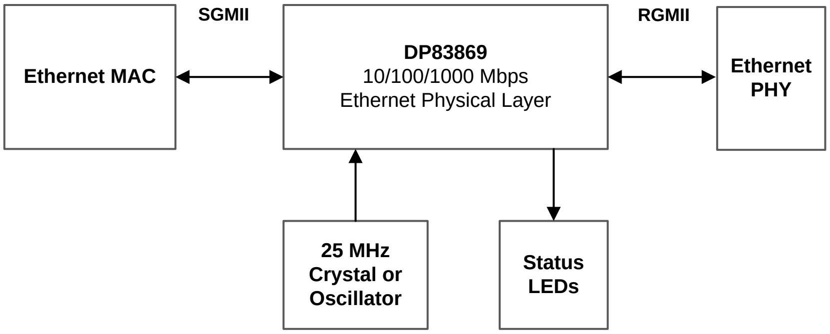


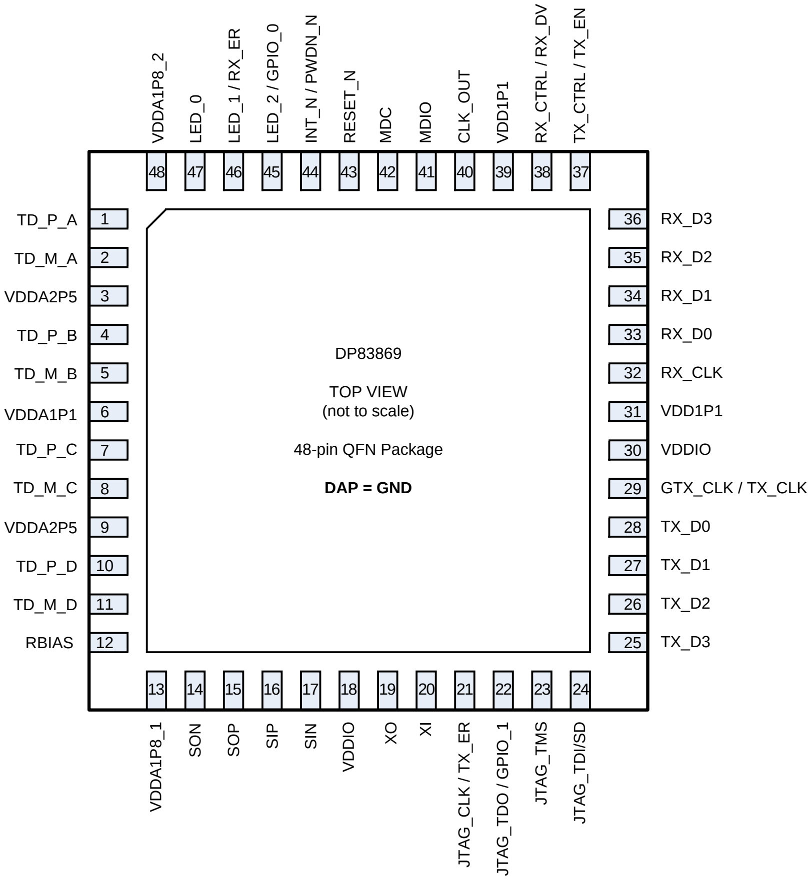
图 **3. SGMII-RGMII** 桥接系统方框图

6 器件比较表

器件	桥接模式	温度	温度等级
DP83869HM	是	-40°C 至 +125ºC	高温

7 Pin Configuration and Functions

RGZ Package
(48-Pin VQFN)
Top View



RGZ Package (VQFN) Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	TD_P_A	I/O	Analog	Differential Transmit and Receive Signals
2	TD_M_A	I/O	Analog	Differential Transmit and Receive Signals
3	VDDA2P5	I	Power	2.5-V Analog Supply (+/-5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
4	TD_P_B	I/O	Analog	Differential Transmit and Receive Signals
5	TD_M_B	I/O	Analog	Differential Transmit and Receive Signals
6	VDD1P1	I	Power	1.1-V Analog Supply (+/-10%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
7	TD_P_C	I/O	Analog	Differential Transmit and Receive Signals
8	TD_M_C	I/O	Analog	Differential Transmit and Receive Signals
9	VDDA2P5	I	Power	2.5-V Analog Supply (+/-5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
10	TD_P_D	I/O	Analog	Differential Transmit and Receive Signals
11	TD_M_D	I/O	Analog	Differential Transmit and Receive Signals
12	RBIAS	I	—	Bias Resistor Connection. An 11-kΩ ±1% resistor should be connected from RBIAS to GND.
13	VDDA1P8_1	I	Power	No external supply is required for this pin in two-supply mode. When unused, no connections should be made to these pins. In three-supply mode, an external 1.8-V(±5%) supply can be connected to these pins. When using an external supply, each pin requires a 1-µF and 0.1-µF capacitor to GND.
14	SON	O	Analog	Differential SGMII or Fiber Data Output: This signal carries data from the PHY to the MAC, fiber transceiver, or link partner in SGMII and fiber modes. This pin should be AC-coupled to the distant device through a 0.1-µF capacitor. This pin provides LVDS signals, additional components may be required for the optical transceiver.
15	SOP	O	Analog	Differential SGMII or Fiber Data Output: This signal carries data from the PHY to the MAC, fiber transceiver, or link partner in SGMII and fiber modes. This pin should be AC-coupled to the distant device through a 0.1-µF capacitor. This pin provides LVDS signals, additional components may be required for the optical transceiver
16	SIP	I	Analog	Differential SGMII or Fiber Data Input: This signal carries data from the MAC, fiber transceiver, or link partner, to the PHY in SGMII and fiber modes. This pin should be AC-coupled to the distant device through a 0.1-µF capacitor. This pin accepts LVDS signals, additional components may be required for the optical transceiver
17	SIN	I	Analog	Differential SGMII or Fiber Data Input: This signal carries data from the MAC, fiber transceiver, or link partner, to the PHY in SGMII and fiber modes. This pin should be AC-coupled to the distant device through a 0.1-µF capacitor. This pin accepts LVDS signals, additional components may be required for the optical transceiver
18	VDDIO	I	Power	I/O Power: 1.8V (±5%), 2.5V (±5%) or 3.3V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND
19	XO	O	Clock	CRYSTAL OSCILLATOR OUTPUT: Second terminal for 25-MHz crystal. Must be left floating if a clock oscillator is used.
20	XI	I	Clock	CRYSTAL OSCILLATOR INPUT: 25-MHz oscillator or crystal input.
21	JTAG_CLK/TX_ER	I	WPU	JTAG TEST CLOCK: IEEE 1149.1 Test Clock input, primary clock source for all test logic input and output controlled by the testing entity. MII Mode: In MII mode, this pin will be configured as TX_ER pin and will be sourced from MAC to PHY. Use of this pin is optional.
22	JTAG_TDO/GPIO_1	O	—	JTAG TEST DATA OUTPUT: IEEE 1149.1 Test Data Output pin, the most recent test results are scanned out of the device via TDO. General Purpose I/O: This signal provides a multi-function configurable I/O. Please refer to the GPIO_MUX_CTRL register for details.
23	JTAG_TMS	I	WPU	JTAG TEST MODE SELECT: IEEE 1149.1 Test Mode Select pin, the TMS pin sequences the Tap Controller (16-state FSM) to select the desired test instruction. TI recommends that the user apply 3 clock cycles with JTAG_TMS high to reset the JTAG.
24	JTAG_TDI/SD	I	WPU	JTAG TEST DATA INPUT: IEEE 1149.1 Test Data Input pin, test data is scanned into the device through the TDI. SD: In 1000Base-X and 100Base-FX mode, this pin will act as Signal Detect. This should be connected to Signal Detect of optical transceiver.

RGZ Package (VQFN) Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
25	TX_D3	I	WPD	TRANSMIT DATA: Signal TX_D[3:0] carries data from the MAC to the PHY in RGMII mode and MII mode. Data is synchronous to the transmit clock. In RGMII mode GTX_CLK is the transmit clock and in MII mode TX_CLK is the transmit clock.
26	TX_D2	I	WPD	
27	TX_D1	I	WPD	
28	TX_D0	I	WPD	
29	GTX_CLK/TX_CLK	I/O	WPD	RGMII TRANSMIT CLOCK: This continuous clock signal is sourced from the MAC layer to the PHY. Nominal frequency is 125 MHz in 1000-Mbps mode. This pin will be Input in RGMII mode. MII TRANSMIT CLOCK: In MII mode, this pin provides a 25-MHz reference clock for 100-Mbps speed and a 2.5-MHz reference clock for 10-Mbps speed. This pin will be output in MII mode. This pin will be GTX_CLK by default and can be changed to TX_CLK by register configurations.
30	VDDIO	I	Power	I/O Power: 1.8 V (±5%), 2.5 V (±5%) or 3.3 V (±5%). Each pin requires a 1-µF and 0.1-µF capacitor to GND
31	VDD1P1	I	Power	1.1-V Analog Supply (±10%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
32	RX_CLK	O	Strap, WPD	RECEIVE CLOCK: Provides the recovered receive clocks for different modes of operation: 125 MHz in 1000-Mbps RGMII mode.
33	RX_D0	O	Strap, WPD	RECEIVE DATA: Signal RX_D[3:0] carries data from the PHY to the MAC in RGMII mode and in MII mode. Symbols received on the cable are decoded and presented on these pins synchronous to RX_CLK.
34	RX_D1	O	Strap, WPD	
35	RX_D2	O	Strap, WPD	
36	RX_D3	O	Strap, WPD	
37	TX_CTRL/TX_EN	I	WPD	TRANSMIT CONTROL: In RGMII mode, TX_CTRL combines the transmit enable and the transmit error signal inputs from the MAC using both clock edges. TX_EN: In MII mode, this pin will function as TX_EN.
38	RX_CTRL/RX_DV	O	WPD	RECEIVE CONTROL: In RGMII mode, the receive data available and receive error are combined (RXDV_ER) using both rising and falling edges of the receive clock (RX_CLK). RX_DV: In MII mode, this pin will function as RX_DV.
39	VDD1P1	I	Power	1.1-V Analog Supply (±10%). Each pin requires a 1-µF and 0.1-µF capacitor to GND.
40	CLK_OUT	O	Clock	CLOCK OUTPUT: Output clock
41	MDIO	I/O	—	MANAGEMENT DATA I/O: Bi-directional management instruction/data signal that may be sourced by the management station or the PHY. This open-drain pin requires a 1.5-kΩ pull-up resistor.
42	MDC	I	—	MANAGEMENT DATA CLOCK: Synchronous clock to the MDIO serial management input/output data. This clock may be asynchronous to the MAC transmit and receive clocks. The maximum clock rate is 25-MHz. There is no minimum clock rate.
43	RESET_N	I	—	RESET_N: This pin is an active-low reset input that initializes or re-initializes all the internal registers of the DP83869. Asserting this pin low for at least 720 ns will force a reset process to occur. It is in IO voltage domain. Reset can be controlled by host controller. If that is not possible then a 100-Ω resistor and 47-uF capacitor are required to be connected in series between RESET_N pin and Ground. Refer to *Reset Operation* section of datasheet.
44	INT_N/PWDN_N	I/O	—	INTERRUPT / POWER DOWN: The default function of this pin is POWER DOWN. POWER DOWN: This is an Active Low Input. Asserting this signal low enables the power-down mode of operation. In this mode, the device powers down and consumes minimum power. Register access is available through the Management Interface to configure and power up the device. INTERRUPT: The interrupt pin is an open-drain, active low output signal indicating an interrupt condition has occurred. Register access is required to determine which event caused the interrupt. TI recommends using an external 2.2-kΩ resistor connected to the VDDIO supply. When register access is disabled through pin option, the interrupt will be asserted for 500 ms before self-clearing.
45	LED_2/GPIO_0	I/O	Strap, WPD	LED_2:This pin is part of the VDDIO voltage domain. General Purpose I/O: This signal provides a multi-function configurable I/O. Please refer to the GPIO_MUX_CTRL register for details.
46	LED_1/RX_ER	O	Strap, WPD	LED_1: This pin is part of the VDDIO voltage domain. MII Mode: In MII mode this pin will be configured as RX_ER. This pin is asserted high synchronously to rising edge of RX_CLK. Use of this pin is optional.

RGZ Package (VQFN) Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
47	LED_0	O	Strap, WPD	LED_0: This pin is part of the VDDIO voltage domain.
48	VDDA1P8_2	I	Power	No external supply is required for this pin in two-supply mode. When unused, no connections should be made to these pins. In three-supply mode, an external 1.8-V(±5%) supply can be connected to these pins. When using an external supply, each pin requires a 1-µF and 0.1-µF capacitor to GND.

Pin Functionality definitions are given below

- I: Input
- O: Output
- I/O: Input/Output
- Strap: Multifunctional bootstrap pins
- WPD: Weak Pull Down Resistor (internal)
- WPU: Weak Pull Up Resistor (internal)
- Power: Power Supply Pins
- Analog: Analog pins

表 1. Pin States-1

PIN NO	PIN NAME	RESET		COPPER MODE					
				MII		RGMII		SGMII	
		PIN STATE	PULL/HI-Z	PIN STATE	PULL/HI-Z	PIN STATE	PULL/HI-Z	PIN STATE	PULL/HI-Z
14	SON	O	Hi-Z	O	Hi-Z	O	Hi-Z	O	50Ω
15	SOP	O	Hi-Z	O	Hi-Z	O	Hi-Z	O	50Ω
16	SIP	I	Hi-Z	I	Hi-Z	I	Hi-Z	I	50Ω
17	SIN	I	Hi-Z	I	Hi-Z	I	Hi-Z	I	50Ω
21	JTAG_CLK/ TX_ER	I	PU	I	PU	I	PU	I	PU
22	JTAG_TDO / GPIO_1	I	PD	O	Hi-Z	O	Hi-Z	O	Hi-Z
23	JTAG_TMS	I	PU	I	PU	I	PU	I	PU
24	JTAG_TDI / SD	I	PU	I	PU	I	PU	I	PU
25	TX_D3	I	PD	I	PD	I	PD	I	PD
26	TX_D2	I	PD	I	PD	I	PD	I	PD
27	TX_D1	I	PD	I	PD	I	PD	I	PD
28	TX_D0	I	PD	I	PD	I	PD	I	PD
29	GTX_CLK / TX_CLK	I	PD	O	PD	I	PD	I	PD
32	RX_CLK	I	PD	O	Hi-Z	O (125MHz)	Hi-Z	I	PD
33	RX_D0	I	PD	O	Hi-Z	O	Hi-Z	I	PD
34	RX_D1	I	PD	O	Hi-Z	O	Hi-Z	I	PD
35	RX_D2	I	PD	O	Hi-Z	O	Hi-Z	I	PD
36	RX_D3	I	PD	O	Hi-Z	O	Hi-Z	I	PD
37	TX_CTRL / TX_EN	I	PD	I	PD	I	PD	I	PD
38	RX_CTRL / RX_DV	I	PD	O	Hi-Z	O	Hi-Z	I	Hi-Z
40	CLK_OUT	O (25MHz)	Hi-Z	O (25MHz)	Hi-Z	O (25MHz)	Hi-Z	O (25MHz)	Hi-Z
41	MDIO	I	Hi-Z	I/O	Hi-Z	I/O	Hi-Z	I/O	Hi-Z
42	MDC	I	Hi-Z	I	Hi-Z	I	Hi-Z	I	Hi-Z
43	RESET_N	I	PU	I	PU	I	PU	I	PU
44	INT_N / PWDN_N	I	PU	I/O	PU/OD-PU	I/O	PU/OD-PU	I/O	PU/OD-PU
45	LED_2 / GPIO_0	I	PD	I/O	Hi-Z	I/O	Hi-Z	I/O	Hi-Z
46	LED_1 / RX_ER	I	PD	O	Hi-Z	O	Hi-Z	O	Hi-Z
47	LED_0	I	PD	O	Hi-Z	O	Hi-Z	O	Hi-Z

表 2. Pin States-2

PIN NO	PIN NAME	MEDIA CONVERTOR		BRIDGE MODE			
				RGMII TO SGMII		SGMII TO RGMII	
		PIN STATE	PULL/HI-Z	PIN STATE	PULL/HI-Z	PIN STATE	PULL/HI-Z
14	SON	O	50Ω	O	50Ω	O	50Ω
15	SOP	O	50Ω	O	50Ω	O	50Ω
16	SIP	I	50Ω	I	50Ω	I	50Ω
17	SIN	I	50Ω	I	50Ω	I	50Ω
21	JTAG_CLK/ TX_ER	I	PU	I	PU	I	PU
22	JTAG_TDO / GPIO_1	O	Hi-Z	O	Hi-Z	O	Hi-Z
23	JTAG_TMS	I	PU	I	PU	I	PU
24	JTAG_TDI / SD	I	PU	I	PU	I	PU
25	TX_D3	I	PD	I	PD	I	PD
26	TX_D2	I	PD	I	PD	I	PD
27	TX_D1	I	PD	I	PD	I	PD
28	TX_D0	I	PD	I	PD	I	PD
29	GTX_CLK / TX_CLK	I	PD	I	PD	I	PD
32	RX_CLK	I	PD	O	Hi-Z	O	Hi-Z
33	RX_D0	I	PD	O	Hi-Z	O	Hi-Z
34	RX_D1	I	PD	O	Hi-Z	O	Hi-Z
36	RX_D2	I	PD	O	Hi-Z	O	Hi-Z
36	RX_D3	I	PD	O	Hi-Z	O	Hi-Z
37	TX_CTRL / TX_EN	I	PD	I	PD	I	PD
38	RX_CTRL / RX_DV	I	PD	O	Hi-Z	O	Hi-Z
40	CLK_OUT	O (25MHz)	Hi-Z	O (25MHz)	Hi-Z	O (25MHz)	Hi-Z
41	MDIO	I/O	Hi-Z	I/O	Hi-Z	I/O	Hi-Z
42	MDC	I	Hi-Z	I	Hi-Z	I	Hi-Z
43	RESET_N	I	PU	I	PU	I	PU
44	INT_N / PWDN_N	I/O	PU/OD-PU	I/O	PU/OD-PU	I/O	PU/OD-PU
45	LED_2 / GPIO_0	I/O	Hi-Z	I/O	Hi-Z	I/O	Hi-Z
46	LED_1 / RX_ER	O	Hi-Z	O	Hi-Z	O	Hi-Z
47	LED_0	O	Hi-Z	O	Hi-Z	O	Hi-Z

表 3. Pin States-3

PIN NO	PIN NAME	IEEE PWDN		MII ISOLATE	
		PIN STATE	PULL/HI-Z	PIN STATE	PULL/HI-Z
14	SON	O	50Ω	O	50Ω
15	SOP	O	50Ω	O	50Ω
16	SIP	I	50Ω	I	50Ω
17	SIN	I	50Ω	I	50Ω
21	JTAG_CLK/ TX_ER	I/O	PU	I	PU
22	JTAG_TDO / GPIO_1	O	Hi-Z	O	Hi-Z
23	JTAG_TMS	I	PU	I	PU
24	JTAG_TDI / SD	I	PU	I	PU
25	TX_D3	I	PD	I	PD
26	TX_D2	I	PD	I	PD
27	TX_D1	I	PD	I	PD
28	TX_D0	I	PD	I	PD
29	GTX_CLK / TX_CLK	I	PD	I	PD
32	RX_CLK	O (2.5MHz)	Hi-Z	I	PD
33	RX_D0	O	Hi-Z	I	PD
34	RX_D1	O	Hi-Z	I	PD
36	RX_D2	O	Hi-Z	I	PD
36	RX_D3	O	Hi-Z	I	PD
37	TX_CTRL / TX_EN	I	PD	I	PD
38	RX_CTRL / RX_DV	O	Hi-Z	I	PD
40	CLK_OUT	O (25MHz)	Hi-Z	O (25MHz)	Hi-Z
41	MDIO	I	Hi-Z	I	Hi-Z
42	MDC	I	Hi-Z	I	Hi-Z
43	RESET_N	I	PD	I	PU
44	INT_N / PWDN_N	I/O	PU/OD-PU	I/O	PU/OD-PU
45	LED_2 / GPIO_0	O	Hi-Z	O	Hi-Z
46	LED_1 / RX_ER	O	Hi-Z	O	Hi-Z
47	LED_0	O	Hi-Z	O	Hi-Z

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Supply voltage	VDD1P1	-0.3	1.4	V
	VDD1P8	-0.3	2.16	V
	VDD2P5	-0.3	3	V
	VDDIO (3V3)	-0.3	3.8	V
	VDDIO (2V5)	-0.3	3	V
	VDDIO (1V8)	-0.3	2.1	V
Pins	MDI	-0.3	6.5	V
Pins	MAC Interface, MDIO, MDC, GPIO	-0.3	VDDIO + 0.3	V
Pins	INT/PWDN, RESET	-0.3	VDDIO + 0.3	V
Pins	JTAG	-0.3	VDDIO + 0.3	V
Storage temperature	Tstg	-60	150	C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

Parameter				VALUE	UNIT
$V_{(ESD)}$	V(ESD) Electrostatic discharge	Human-body model (HBM), perANSI/ESDA/JEDEC JS-001(1)	All pins except MDI	+/-2500	V
			MDI pins(2)	+/-8000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	All Pins	+/-1500	
		IEC 61000-4-2 contact discharge	MDI pins	+/-8000	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 500 V HBM is possible with the necessary precautions. Pins listed as ±8 kV and/or ± 2 kV may actually have higherperformance.
(2) MDI Pins tested as per IEC 61000-4-2 standards.
(3) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process. Manufacturing withless than 250 V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		MIN	NOM	MAX	UNIT
VDDIO	Digital Supply Voltage, 1.8V operation	1.71	1.8	1.89	V
	Digital Supply Voltage, 2.5V operation	2.375	2.5	2.625	
	Digital Supply Voltage, 3.3V operation	3.15	3.3	3.45	
VDD1P1	Digital Supply	0.99	1.1	1.21	V
VDDA1P8	Analog Supply	1.71	1.8	1.89	V
VDDA2P5	Analog Supply	2.375	2.5	2.625	V
T_A	Operating Ambient Temperature (DP83869HM)	-40		125	℃

8.4 Thermal Information

THERMAL METRIC[1]		48PIN VQFN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	7.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1000Base-X/SGMII INPUT						
	Input differential voltage tolerance	SI_P and SI_N, AC coupled	0.35	0.5	2.0	V
	Receiver differential input impedance (DC)		80	100	120	Ohm
	Frequency tolerance	SI_P and SI_N, AC coupled	-100		+100	ppm
1000Base-X OUTPUT						
	Clock signal duty cycle	SO_P and SO_N, AC coupled, 0101010101 pattern	48		52	%
	Vod fall time (20%-80%)	SO_P and SO_N, AC coupled, 0101010101 pattern	100		200	ps
	Vod rise time (20%-80%)	SO_P and SO_N, AC coupled, 0101010101 pattern	100		200	ps
	Total Ouput Jitter	SO_P and SO_N, AC coupled		192		ps
	Output Differential Voltage (Configuration bits for 0.6V - 1.27V; Default at 1.1V)	SO_P and SO_N, AC coupled	1060	1100	1140	mV
100Base-FX OUTPUT						
	Clock signal duty cycle at 625MHz	SO_P and SO_N, AC coupled			55	%
	Vod fall time (20%-80%)	SO_P and SO_N, AC coupled			330	ps
	Vod rise time (20%-80%)	SO_P and SO_N, AC coupled			330	ps
	Jitter	SO_P and SO_N, AC coupled			192	ps
	Output Differential Voltage (Configuration bits for 0.6V - 1.8V)	SO_P and SO_N, AC coupled	450		910	mV
SGMII OUTPUT						
	Clock signal duty cycle @625MHz	SO_P and SO_N, AC coupled, 0101010101 pattern	48		52	%
	Vod fall time (20%-80%)	SO_P and SO_N, AC coupled, 0101010101 pattern	100		200	ps
	Vod rise time (20%-80%)	SO_P and SO_N, AC coupled, 0101010101 pattern	100		200	ps
	Output Jitter	SO_P and SO_N, AC coupled			300	ps
	Output Differential Voltage (Configuration bits for 0.6V - 1.27V; Default at 1.1V)	SO_P and SO_N, AC coupled	1060	1100	1140	mV
IEEE Tx CONFORMANCE (1000BaseT)						
	Output Differential Voltage	Normal Mode, All channels	0.67	0.745	0.82	V
IEEE Tx CONFORMANCE (100BaseTx)						
	Output Differential Voltage	Normal Mode, Channels A and B	0.95	1.00	1.05	V
IEEE Tx CONFORMANCE (10BaseTe)						
	Output Differential Voltage			1.75		V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER CONSUMPTION Copper mode (100m cable, 50% utilization)						
Total	RGMII to Copper (1G)	Room Temperature, Nominal supply voltages		483		mW
	RGMII to Copper (100M)			215		mW
	RGMII to Copper (10M)			260		mW
	MII to Copper (100M)			212		mW
	MII to Copper (10M)			261		mW
	SGMII to Copper (1G)			496		mW
	SGMII to Copper (100M)			251		mW
	SGMII to Copper (10M)			294		mW
POWER CONSUMPTION Fiber mode (50% utilization)						
Total	RGMII to 1000Base-X	Room Temperature, Nominal supply voltages		142		mW
	RGMII to 100Base-FX			111		mW
	MII to 100Base-FX			107		mW
POWER CONSUMPTION R2S mode (50% utilization)						
Total	RGMII to SGMII (1G)	Room Temperature, Nominal supply voltages		142		mW
	RGMII to SGMII (100M)			120		mW
	RGMII to SGMII (10M)			117		mW
POWER CONSUMPTION S2R mode (50% utilization)						
Total	SGMII to RGMII (1G)	Room Temperature, Nominal supply voltages		142		mW
	SGMII to RGMII (100M)			121		mW
	SGMII to RGMII (10M)			117		mW
POWER CONSUMPTION Cu-Fiber mode (100m cable, 50% utilization)						
Total	1000Base-TX to 1000Base-FX	Room Temperature, Nominal supply voltage		495		mW
	100Base-TX to 100Base-FX			243		mW
POWER CONSUMPTION Low power modes						
Total	IEEE Power Down	Room Temperature, Nominal Voltages		76		mW
	Active Sleep			165		mW
	RESET			82		mW
BOOTSTRAP DC CHARACTERISTICS (4 Level) (PHY address pins)						
V_{MODE0}	Mode 0 Strap Voltage Range		0		0.093 x VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range		0.136 x VDDIO		0.184 x VDDIO	V
V_{MODE2}	Mode 2 Strap Voltage Range		0.219 x VDDIO		0.280 x VDDIO	V
V_{MODE3}	Mode 3 Strap Voltage Range		0.6 x VDDIO		0.888 x VDDIO	V
BOOTSTRAP DC CHARACTERISTICS (2 Level)						
V_{MODE0}	Mode 0 Strap Voltage Range		0		0.18 x VDDIO	V
V_{MODE1}	Mode 1 Strap Voltage Range		0.5 x VDDIO		0.88 x VDDIO	V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IO CHARACTERISTICS						
V_{IH}	High Level Input Voltage	VDDIO = 3.3V ±5%	2			V
V_{IL}	Low Level Input Voltage	VDDIO = 3.3V ±5%			0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 3.3V ±5%	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 3.3V ±5%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 2.5V ±5%	1.7			V
V_{IL}	Low Level Input Voltage	VDDIO = 2.5V ±5%			0.7	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 2.5V ±5%	2			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 2.5V ±5%			0.4	V
V_{IH}	High Level Input Voltage	VDDIO = 1.8V ±5%	0.65*VDDIO			V
V_{IL}	Low Level Input Voltage	VDDIO = 1.8V ±5%			0.35*VDDIO	V
V_{OH}	High Level Output Voltage	I_{OH} = -2mA, VDDIO = 1.8V ±5%	VDDIO-0.45			V
V_{OL}	Low Level Output Voltage	I_{OL} = 2mA, VDDIO = 1.8V ±5%			0.45	V
I_{IH}	Input High Current	T_A = -40℃ to 125℃, VIN=VDDIO	-20		20	µA
I_{IL}	Input Low Current	T_A = -40℃ to 125℃, VIN=GND	-20		20	µA
Iozh	Tri-state Output High Current	T_A = -40℃ to 125℃, VOUT=VDDIO	-20		20	µA
Iozl	Tri-state Output Low Current	T_A = -40℃ to 125℃, VOUT=GND	-20		20	µA
R_{pulldn}	Internal Pull Down Resistor		6.75	9	11.25	kΩ
XI V_{IH}	High Level Input Voltage		1.2		VDDIO	V
XI V_{IL}	Low Level Input Voltage				0.6	V
C_{IN}	Input Capacitance XI			1		pF
C_{IN}	Input Capacitance INPUT PINS			5		pF
C_{OUT}	Output Capacitance XO			1		pF
C_{OUT}	Output Capacitance OUTPUT PINS			5		pF
R_{series}	Integrated MAC Series Termination Resistor	RX_D[3:0], RX_ER, RX_DV, RX_CLK		50		Ω

8.6 Timing Requirements

PARAMETER		MIN	NOM	MAX	UNIT
POWER-UP TIMING (2, 3 supply mode)					
T1	Last Supply power up To Reset Release: External or via R-C network	200			ms
T2	Powerup to SMI ready: Post power-up stabilization time prior to MDC preamble for register access		200		ms
T3	Powerup to Strap latchin: Hardware configuration pins transition to output drivers		200		ms
RESET TIMING					
T1	Reset to SMI ready: Post reset stabilization time prior to MDC preamble for register access	30			us
T3	RESET PULSE Width: Miminum Reset pulse width to be able to reset	720			ns
T4	Reset to FLP		1750		ms
T4	Reset to 100M signaling (strapped mode)		194		us
T4	Reset to 1G signaling (strapped mode)		194		us
T4	Reset to Fiber 100M signaling		248		us
T4	Reset to Fiber 1G ANEG signaling		235		us
T4	Reset to Fiber 1G Forced signaling		235		us
T4	Reset to MAC clock (Cu mode)		195		us
T4	Reset to MAC clock (Fi mode)		248		us
T4	Reset to MAC clock (S2R)		248		us
T4	Reset to MAC clock (R2S)		248		us
COPPER LINK TIMING					
T1	Loss of Idles to Link LED low in Fast link down mode (100M)		4.3	10	us
	Loss of Idles to Link LED low in Fast link down mode (1000M)		7	10	us
MII TIMING (100M)					
T1	TX_CLK High / Low Time	16	20	24	ns
T2	TX_D[3:0], TX_ER, TX_EN Setup to TX_CLK	10			ns
T3	TX_D[3:0], TX_ER, TX_EN Hold from TX_CLK	0			ns
T1	RX_CLK High / Low Time	16	20	24	ns
T2	RX_D[3:0], RX_ER, RX_DV Delay from RX_CLK rising	10		30	ns
RGMII OUTPUT TIMING (1G)					
T_{skewT}	Data to Clock Output Skew (Non-Delay Mode)	-600		600	ps
T_{skewR}	Data to Clock Output Setup (Delay Mode)	1	1.8	2.6	ns
T_{cyc}	Clock Cycle Duration	7.2	8	8.8	ns
	Duty Cycle	45	50	55	%
	Rise / Fall Time (20% to 80%)			0.75	ns
RGMII INPUT TIMING (1G)					
T_{setupR}	TX data to clock input setup (Non-Delay Mode)	1			ns
T_{holdR}	TX clock to data input hold (Non-Delay Mode)	1			ns
	TX data to clock input setup (Delay Mode, 2ns delay)	-1			ns
	TX clock to data input hold (Delay Mode, 2ns delay)	3			ns
SMI TIMING					
T1	MDC to MDIO (Output) Delay Time	0		10	ns
T2	MDIO (Input) to MDC Setup Time	10			ns
T3	MDIO (Input) to MDC Hold Time	10			ns
T4	MDC Frequency		2.5	25	MHz

Timing Requirements (continued)

PARAMETER		MIN	NOM	MAX	UNIT
OUTPUT CLOCK TIMING (25MHz clockout)					
	Frequency (PPM)	-100		100	-
	Duty Cycle	40		60	%
	Rise Time			5000	ps
	Fall Time			5000	ps
	Frequency		25		MHz
	Jitter (Long Term)			375	ps
OUTPUT CLOCK TIMING (SyncE 125/5 MHz recovered clock)					
	Frequency (PPM)	-100		100	ppm
	Duty Cycle	40		60	%
	Rise time			2500	ps
	Fall Time			2500	ps
	Jitter (Long Term)			1000	ps
25MHz INPUT CLOCK tolerance					
	Frequency Tolerance	-100		+100	ppm
	Rise / Fall Time (10%-90%)			8	ns
	Jitter Tolerance (Accumulated)		75		ps
	Duty Cycle	40		60	%
TRANSMIT LATENCY TIMING					
Copper	RGMII to Cu (100M): Rising edge TX_CLK with assertion TX_CTRL to SSD symbol on MDI		169		ns
Copper	RGMII to Cu (1G): Roundtrip Latency (Transmit + Receive)			384	ns
RECEIVE LATENCY TIMING					
Copper	Cu to RGMII (100M): SSD symbol on MDI to a) Rising edge of RX_DV with assertion of RX_CTRL b) Rising edge of RX_DV with assertion of RX_Dx		192		ns

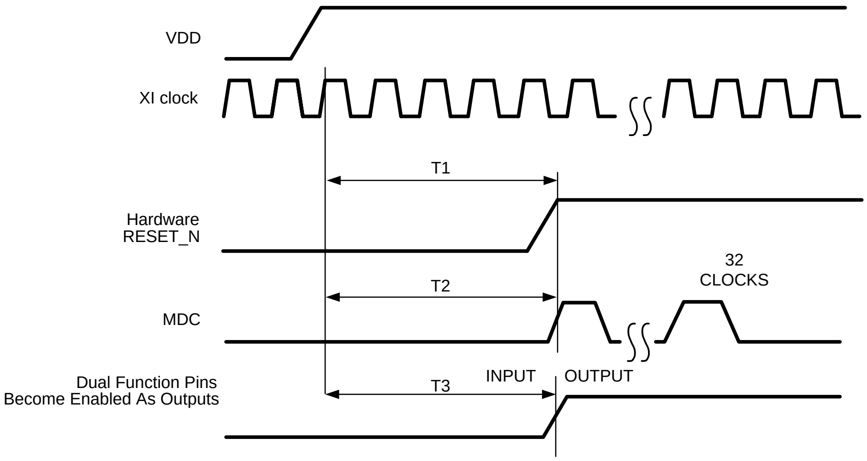


图 4. Power-Up Timing

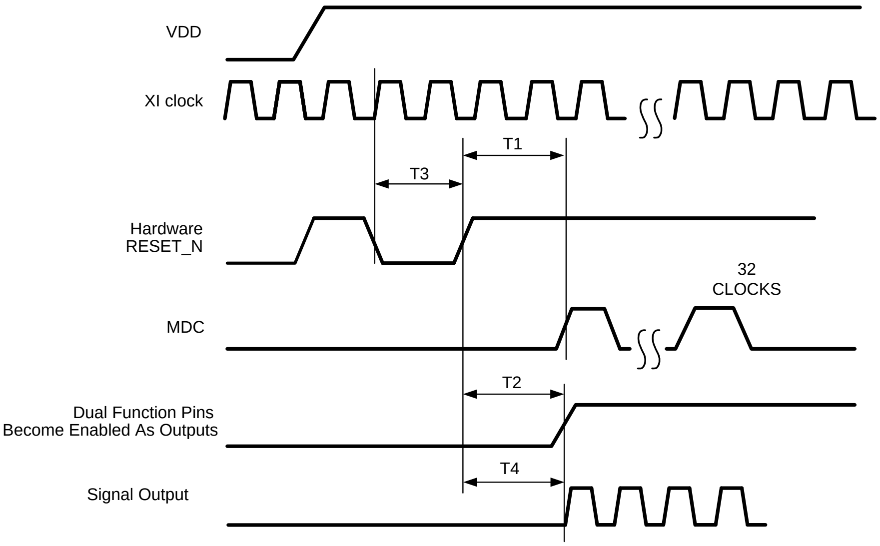


图 5. Reset Timing

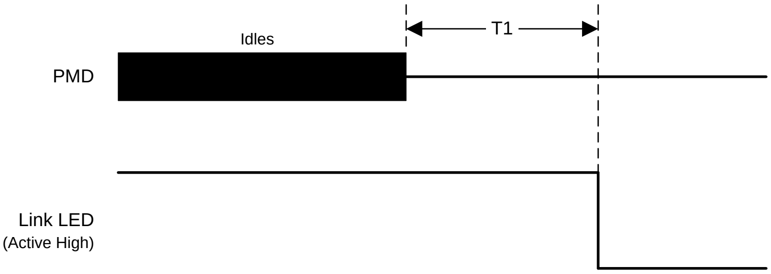


图 6. Copper Link Timing

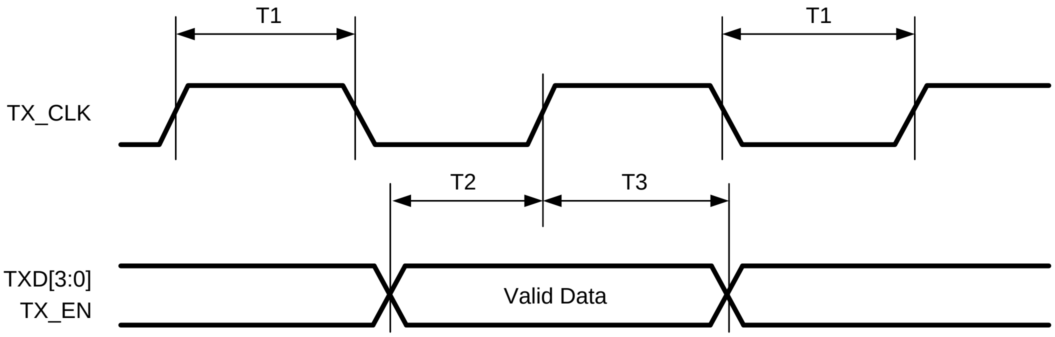


图 7. 100-Mbps MII Transmit Timing

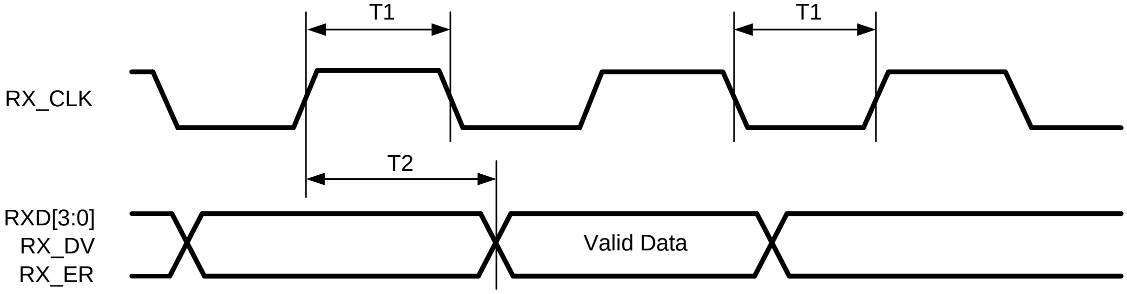


图 8. 100-Mbps MII Receive Timing

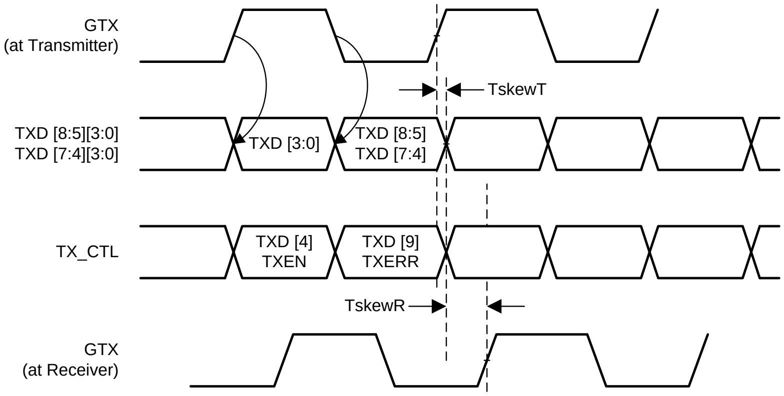


图 9. RGMII Transmit Multiplexing and Timing Diagram

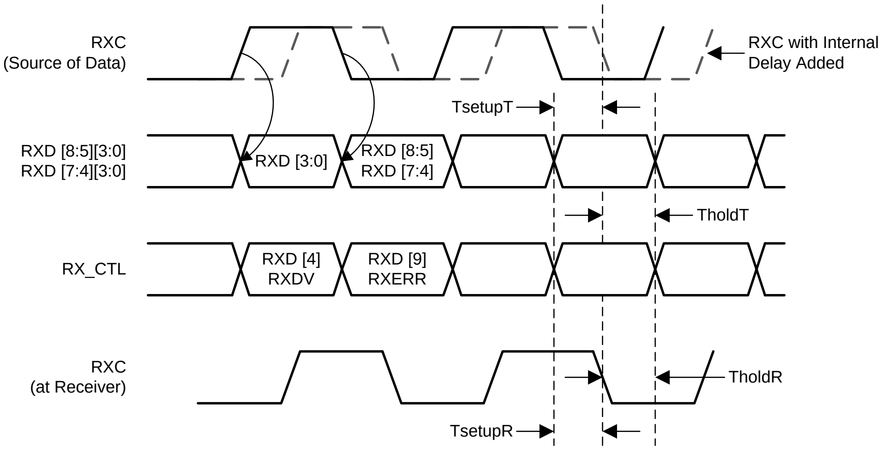


图 10. RGMII Receive Multiplexing and Timing Diagram

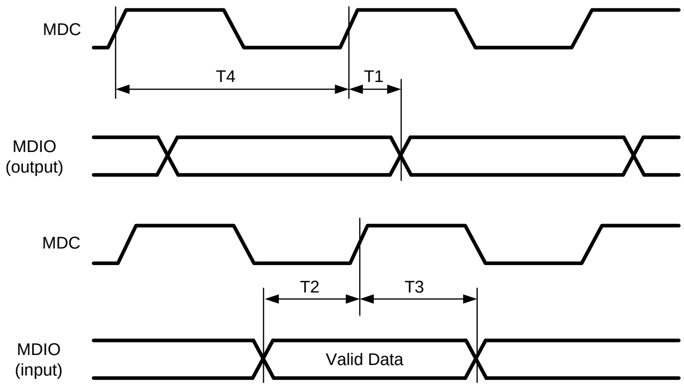
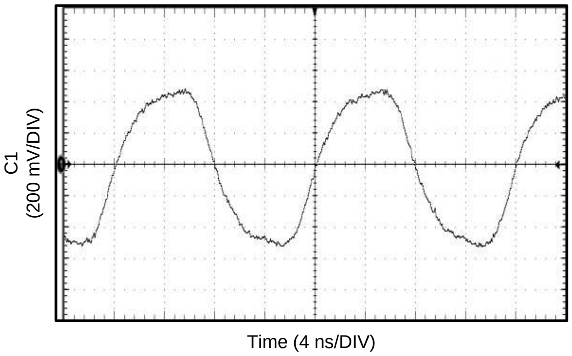


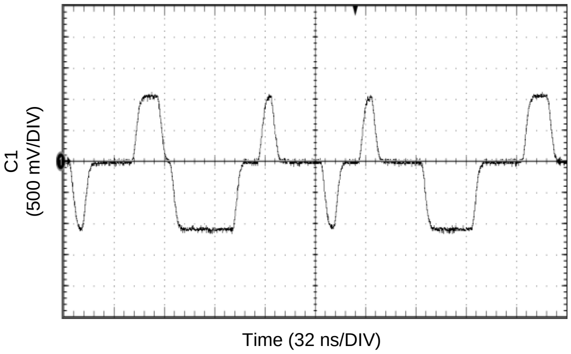
图 11. Serial Management Interface Timing

8.7 Typical Characteristics



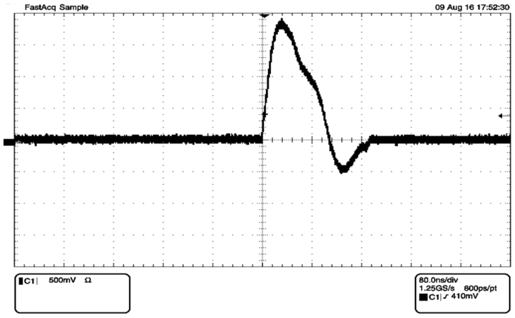
mV/Div	**ns/Div**
200 mV	4 ns

图 12. 1000Base-T Signal



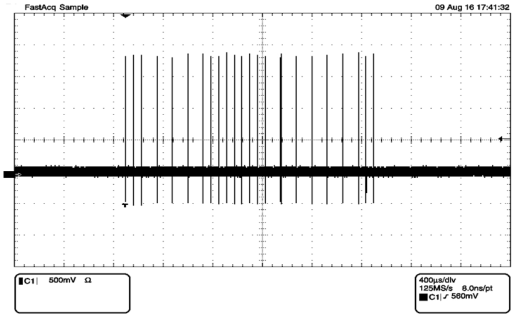
mV/Div	**ns/Div**
500 mV	32 ns

图 13. 100Base-TX Signal



mV/Div	**ns/Div**
500 mV	80 ns

图 14. 10Base-Te Link Pulse



mV/Div	**µs/Div**
500 mV	400 µs

图 15. Auto-Negotiation FLP

9 Detailed Description

9.1 Overview

The DP83869HM is a fully-featured Gigabit Physical Layer transceiver with support for Fiber and Copper Ethernet standards. It can support IEEE802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T Copper Ethernet protocols, along with 100BASE-FX and 1000BASE-X Fiber Ethernet protocols.

The DP83869HM is designed for easy implementation of 10-Mbps, 100-Mbps, and 1000-Mbps Ethernet LANs. In Copper mode, the PHY can interface with twisted-pair media through magnetics. In Fiber Mode, it can interface with Fiber Optic Transceivers. This device interfaces directly to the MAC layer through the Reduced GMII (RGMII) or Serial GMII (SGMII). SGMII is available only in copper Ethernet mode. MII mode is supported for 10M and 100M speeds.

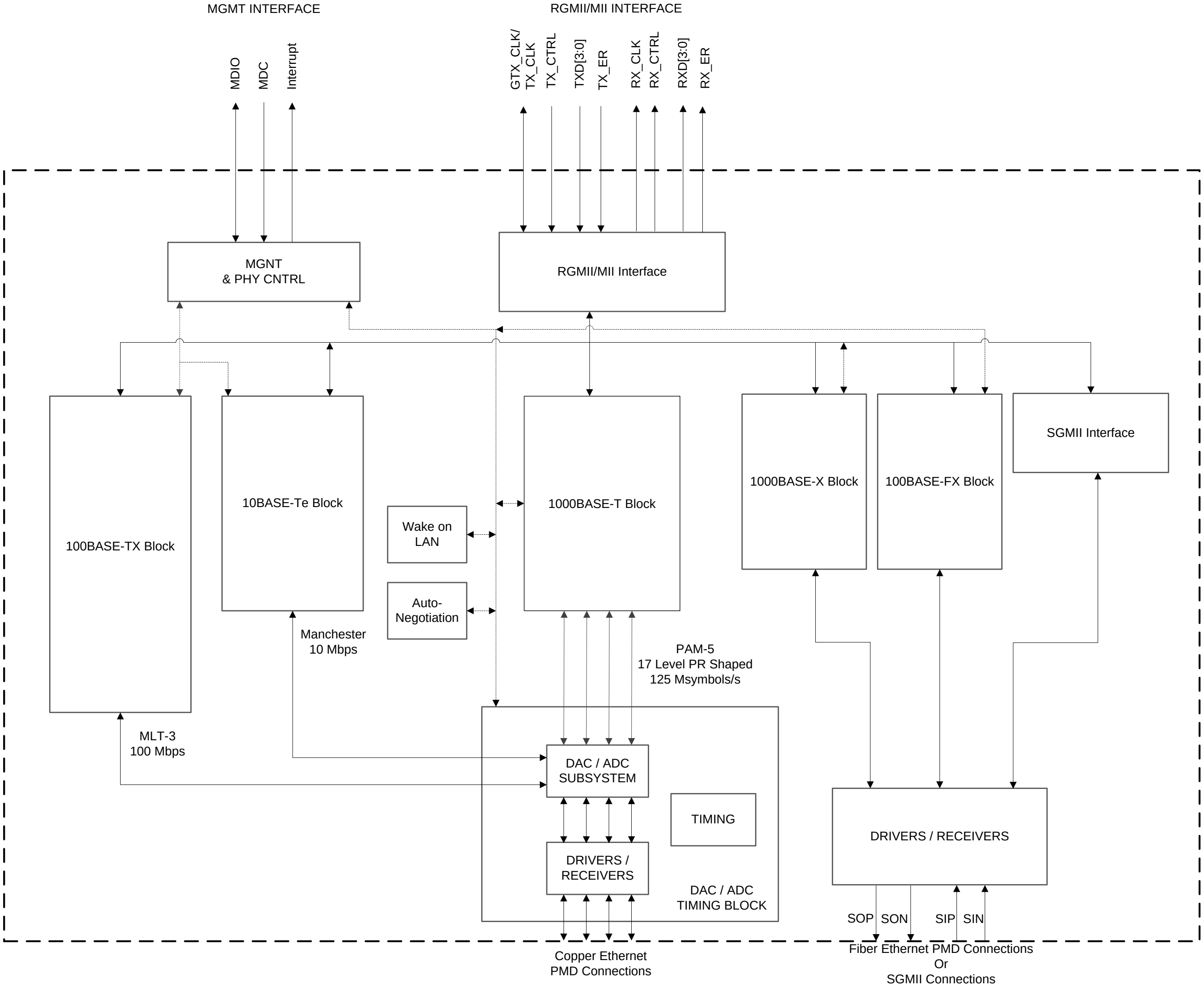
The DP83869HM supports media convertor mode to interface between copper and fiber Ethernet interface. Media convertor is available for 100M and 1000M speeds.

The DP83869HM can also support bridge mode to interface between SGMII and RGMII.

The DP83869HM offers low latency. It provides IEEE 1588 Start of Frame Delimiter indication. It has option to provide recovered clock for synchronous Ethernet application.

The DP83869HM has a TDR cable diagnostic feature for fault detection on the Ethernet cable.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 WoL (Wake-on-LAN) Packet Detection

Wake-on-LAN provides a mechanism to detect specific frames and notify the connected MAC through either a register status change, GPIO indication, or an interrupt flag. The WoL feature within the DP83869HM allows for connected devices placed above the Physical Layer to remain in a low power state until frames with the qualifying credentials are detected. Supported WoL frame types include: Magic Packet, Magic Packet with SecureOn, and Custom Pattern Match. When a qualifying WoL frame is received, the DP83869HM WoL logic circuit is able to generate a user-defined event (either pulses or level change) through any of the GPIO pins or a status interrupt flag to inform a connected controller that a wake event has occurred.

The Wake-on-LAN feature includes the following functionality:

- Identification of magic packets in all supported speeds
- Wake-up interrupt generation upon receiving a valid magic packet
- CRC checking of magic packets to prevent interrupt generation for invalid packets

In addition to the basic magic packet support, the DP83869HM also supports:

- Magic packets that include a SecureOn password
- Pattern match – one configurable 64-byte pattern of that can wake up the MAC similar to magic packet
- Independent configuration for Wake on Broadcast and Unicast packet types.

9.3.1.1 Magic Packet Structure

When configured for Magic Packet mode, the DP83869HM scans all incoming frames addressed to the node for a specific data sequence. This sequence identifies the frame as a Magic Packet frame.

注

The Magic Packet should be byte aligned.

A Magic Packet frame must also meet the basic requirements for the LAN technology chosen, such as SOURCE ADDRESS, DESTINATION ADDRESS (which may be the receiving station’s IEEE address or a BROADCAST address), and CRC.

The specific Magic Packet sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions, followed by a SecureOn password if security is enabled. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream is defined as 6 bytes of FFh.

Feature Description (接下页)

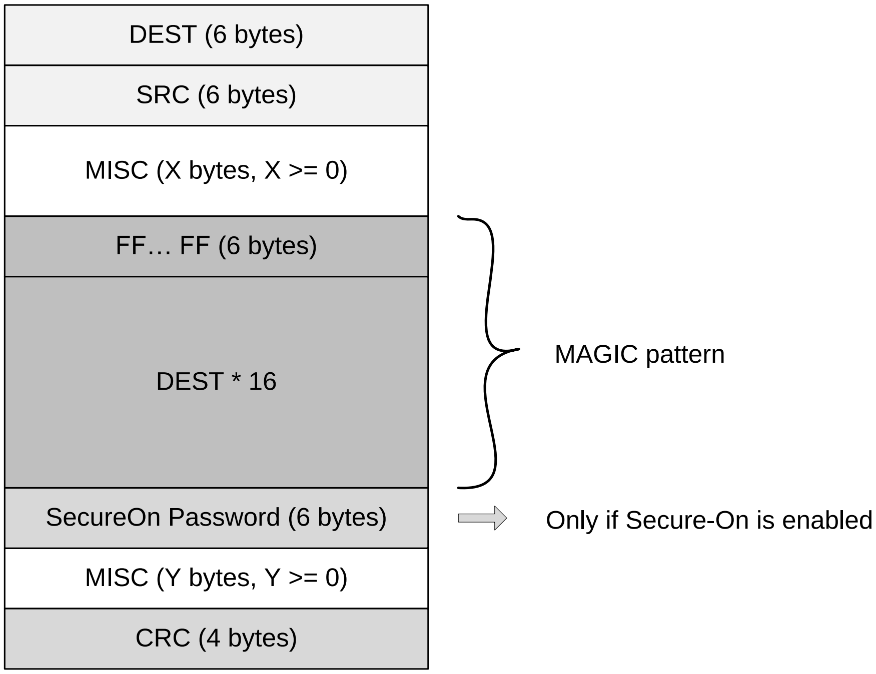


图 16. Magic Packet Structure

9.3.1.2 Magic Packet Example

The following is an example Magic Packet for a Destination Address of 11h 22h 33h 44h 55h 66h and a SecureOn Password 2Ah 2Bh 2Ch 2Dh 2Eh 2Fh:

```
  DESTINATION SOURCE MISC FF FF FF FF FF FF 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22
 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66
 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44
 55 66 11 22 33 44 55 66 2A 2B 2C 2D 2E 2F MISC CRC
```

9.3.1.3 Wake-on-LAN Configuration and Status

Wake-on-LAN functionality is configured through the RXFCFG register (address 0x0134). Wake-on-LAN status is reported in the RXFSTS register (address 0x0135).

9.3.2 Start of Frame Detect for IEEE 1588 Time Stamp

The DP83869HM supports an IEEE 1588 indication pulse at the SFD (start frame delimiter) for the receive and transmit paths. The pulse can be delivered to various pins. The pulse indicates the actual time the symbol is presented on the lines (for transmit), or the first symbol received (for receive). The exact timing of the pulse can be adjusted through register. Each increment of phase value is an 8-ns step.

Feature Description (接下页)

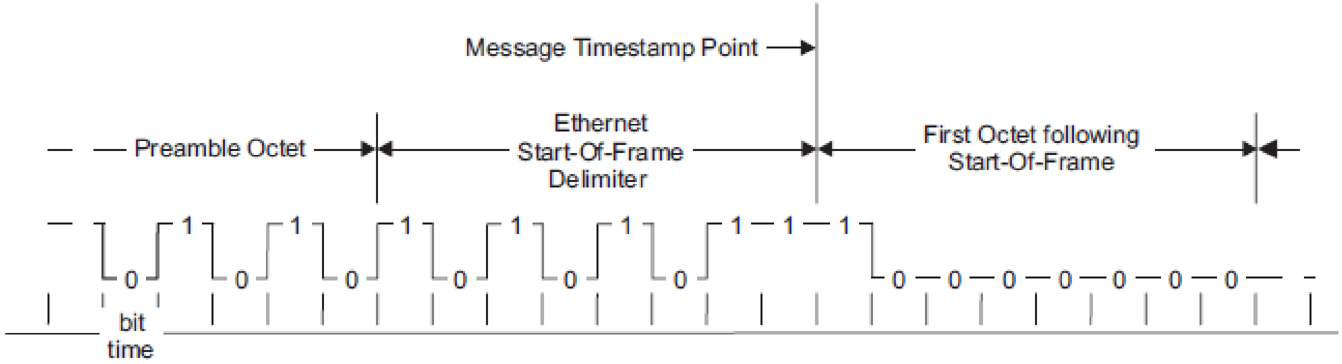


图 17. IEEE 1588 Message Timestamp Point

The SFD pulse output can be configured using the GPIO Mux Control register GPIO_MUX_CTRL (register address 0x01E0). The ENHANCED_MAC_SUPPORT bit in RXCFG (register address 0x0134) must also be set to allow output of the SFD.

9.3.2.1 SFD Latency Variation and Determinism

Time stamping packet transmission and reception using the RX_CTRL and TX_CTRL signals of RGMII is not accurate enough for latency sensitive protocols. SFD pulses offers system designers a method to improve the accuracy of packet time stamping. The SFD pulse, while varying less than RGMII signals inherently, still exhibits latency variation due to the defined architecture of 1000BASE-T. This section provides a method to determine when an SFD latency variation has occurred and how to compensate for the variation in system software to improve timestamp accuracy.

In the following section the terms baseline latency and SFD variation are used. Baseline latency is the time measured between the TX_SFD pulse to the RX_SFD pulse of a connected link partner, assuming an Ethernet cable with all 4 pairs perfectly matched in propagation time. In the scenario where all 4 pairs being perfectly matched, a 1000BASE-T PHY will not have to align the 4 received symbols on the wire and will not introduce extra latency due to alignment.

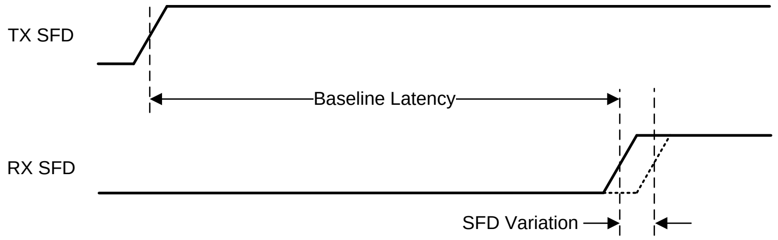


图 18. Baseline Latency and SFD Variation in Latency Measurement

SFD variation is additional time added to the baseline latency before the RX_SFD pulse when the PHY must introduce latency to align the 4 symbols from the Ethernet cable. Variation can occur when a new link is established either by cable connection, auto-negotiation restart, PHY reset, or other external system effects. During a single, uninterrupted link, the SFD variation will remain constant.

The DP83869HM can limit and report the variation applied to the SFD pulse while in the 1000-Mb operating mode. Before a link is established in 1000-Mb mode, the Sync FIFO Control Register (register address 0x00E9) must be set to value 0xDF22. The below SFD variation compensation method can only be applied after the Sync FIFO Control Register has been initialized and a new link has been established. It is acceptable to set the Sync FIFO Control register value and then perform a software restart by setting the SW_RESTART bit[14] in the Control Register (register address 0x001F) if a link is already present.

Feature Description (接下页)

9.3.2.1.1 1000-Mb SFD Variation in Master Mode

When the DP83869HM is operating in 1000-Mb master mode, variation of the RX_SFD pulse can be estimated using the Skew FIFO Status register (register address 0x0055) bit[7:4]. The value read from the Skew FIFO Status register bit[7:4] must be multiplied by 8 ns to estimate the RX_SFD variation added to the baseline latency.

Example: While operating in master 1000-Mb mode, a value of 0x2 is read from the Skew FIFO register bit[7:4]. 2 × 8 ns = 16 ns is subtracted from the TX_SFD to RX_SFD measurement to determine the baseline latency.

9.3.2.1.2 1000-Mb SFD Variation in Slave Mode

When the DP83869HM is operating in 1000-Mb slave mode, the variation of the RX_SFD pulse can be determined using the Skew FIFO Status register (register address 0x0055) bit[3:0].The value read from the Skew FIFO Status register bit[3:0] should be multiplied by 8ns to estimate the RX_SFD variation added to the baseline latency.

Example: While operating in slave 1000-Mb mode, a value of 0x1 is read from the Skew FIFO register bit[3:0]. 1 × 8 ns = 8 ns is subtracted from the TX_SFD to RX_SFD measurement to determine the baseline latency.

9.3.2.1.3 100-Mb SFD Variation

The latency variation in 100-Mb mode of operation is determined by random process and does not require any register readout or system level compensation of SFD pulses.

9.3.3 Clock Output

The DP83869HM has several internal clocks, including the local reference clock, the Ethernet transmit clock, and the Ethernet receive clock. An external crystal or oscillator provides the stimulus for the local reference clock. The local reference clock acts as the central source for all clocking in the device.

The local reference clock is embedded into the transmit network packet traffic and is recovered from the network packet traffic at the receiver node. The receive clock is recovered from the received Ethernet packet data stream and is locked to the transmit clock in the partner.

Using the I/O Configuration register (address 0x0170), the DP83869HM can be configured to output these internal clocks through the CLK_OUT pin. By default, the output clock is synchronous to the XI oscillator / crystal input. The default output clock is suitable for use as the reference clock of another DP83869HM device. Through registers, the output clock can be configured to be synchronous to the receive data at the 125-MHz data rate or at the divide by 5 rate of 25 MHz. It can also be configured to output the line driver transmit clock. When operating in 1000Base-T mode, the output clock can be configured for any of the four transmit or receive channels.

It is important to note that when clock output of DP83869HM is being used as a clock input for another device, for e.g. two DP83869HM in daisy chain, then the primary DP83869HM should not be reset via the RESET pin. If reset is required then it should be performed via software. The output clock can be disabled using the CLK_O_DISABLE bit of the I/O Configuration register.

9.3.4 Loopback Mode

There are several options for Loopback that test and verify various functional blocks within the PHY. Enabling loopback mode allows in-circuit testing of the digital and analog data paths. Generally, the DP83869HM may be configured to one of the Near-end loopback modes or to the Far-end (reverse) loopback. MII Loopback is configured using the BMCR (register address 0x0000). All other loopback modes are enabled using the BIST_CONTROL (register address 0x16). Except where otherwise noted, loopback modes are supported for all speeds (10/100/1000) and all MAC interfaces (SGMII and RGMII).

Feature Description (接下页)

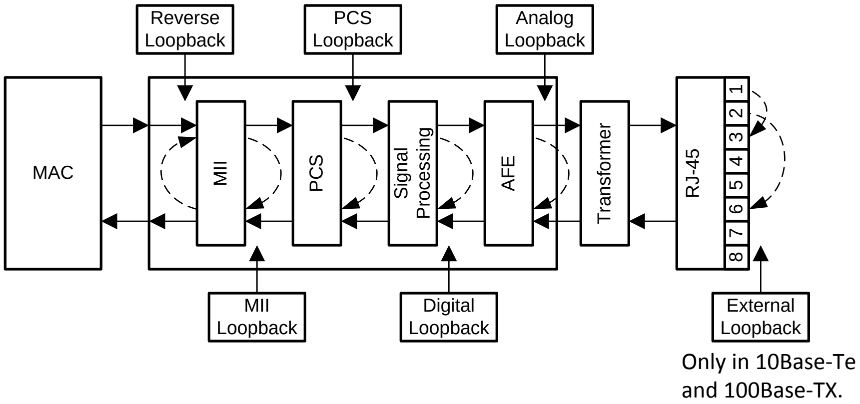


图 19. Loopbacks

9.3.4.1 Near-End Loopback

Near-end loopback provides the ability to loop the transmitted data back to the receiver through the digital or analog circuitry. The point at which the signal is looped back is selected using loopback control bits with several options being provided.

When configuring loopback modes, the Loopback Configuration Register (LOOPCR), address 0x00FE, should be set to 0xE720.

To maintain the desired operating mode, Auto-Negotiation should be disabled before selecting the Near-End Loopback mode. This constraint does not apply for external-loopback mode.

Auto-MDIX should be disabled before selecting the Near-End Loopback mode. MDI or MDIX configuration should be manually configured.

9.3.4.1.1 MII Loopback

MII Loopback is the shallowest loop through the PHY. It is a useful test mode to validate communications between the MAC and the PHY. While in MII Loopback mode, the data is looped back and can be configured through the register to transmit onto the media. In 100Base-TX mode after MII loopback is enabled through register 0x00, it is necessary to write 0x0004 to register 0x16 for proper operation of MII Loopback.

9.3.4.1.2 PCS Loopback

PCS Loopback occurs in the PCS layer of the PHY. No signal processing is performed when using PCS Loopback.

9.3.4.1.3 Digital Loopback

Digital Loopback includes the entire digital transmit – receive path. Data is looped back prior to the analog circuitry.

9.3.4.1.4 Analog Loopback

Analog Loopback includes the entire analog transmit-receive path. For proper operation in Analog Loopback mode, attach 100-Ω terminations to the copper side when operating in Copper mode and 100-Ω termination on fiber side when operating in Fiber mode.

9.3.4.1.5 External Loopback

When operating in 10BASE-Te or 100Base-T mode, signals can be looped back at the RJ-45 connector by wiring the transmit pins to the receive pins. Due to the nature of the signaling in 1000Base-T mode, this type of external loopback is not supported. Analog loopback provides a way to loop data back in the analog circuitry when operating in 1000Base-T mode.

Feature Description (接下页)

9.3.4.1.6 Far-End (Reverse) Loopback

Far-end (Reverse) Loopback is a special test mode to allow testing the PHY from the link-partner side. In this mode, data that is received from the link partner passes through the PHY's receiver is looped back at the MAC interface and is transmitted back to the link partner. While in Reverse Loopback mode, all data signals that come from the MAC are ignored. Through register configuration, data can also be transmitted onto the MAC Interface.

The availability of Loopback depends on the operational mode of the PHY. The Link Status in these loopback modes is also affected by the operational mode. 表 4 lists out the exceptions where Loopbacks are not available.

表 4. Loopback Availability Exception

OP MODE	LOOPBACK	EXCEPTION
Copper	PCS	10M
Fiber	MII	100M
	PCS	100M
	Analog	100M, 1000M
SGMII to RGMII	PCS	10M, 100M, 1000M
	Digital	10M, 100M, 1000M
	Analog	10M, 100M, 1000M
	External	10M, 100M, 1000M
RGMII to SGMII	PCS	10M, 100M, 1000M
	External	10M, 100M, 1000M
Media Convertor	MII	100M, 1000M
	Analog	100M on Fiber Interface
	External	100M on Fiber Interface
		100M, 1000M on Copper Interface

9.3.5 BIST Configuration

The device incorporates an internal PRBS Built-In Self Test (BIST) circuit to accommodate in-circuit testing or diagnostics. The BIST circuit can be used to test the integrity of the transmit and receive data paths. The BIST can be performed using both internal loopback (digital or analog) or external loopback using a cable fixture. The BIST simulates pseudo-random data transfer scenarios in format of real packets and Inter-Packet Gap (IPG) on the lines. The BIST allows full control of the packet lengths and of the IPG.

The BIST is implemented with independent transmit and receive paths, with the transmit block generating a continuous stream of a pseudo-random sequence. The device generates a 15-bit pseudo-random sequence for the BIST. The received data is compared to the generated pseudo-random data by the BIST Linear Feedback Shift Register (LFSR) to determine the BIST pass or fail status. The number of error bytes that the PRBS checker received is stored in the PRBS_TX_CHK_CTRL register (0x39). The status of whether the PRBS checker is locked to the incoming receive bit stream, whether the PRBS has lost sync, and whether the packet generator is busy, can be read from the GEN_STATUS2 register (0x17h). While the lock and sync indications are required to identify the beginning of proper data reception, for any link failures or data corruption, the best indication is the contents of the error counter in the PRBS_TX_CHK_CTRL register (0x39). The number of received bytes are stored in PRBS_TX_CHK_BYTE_CNT (0x3A).

The PRBS test can be put in a continuous mode by using the BIST_CONTROL register (0x16h). In continuous mode, when one of the PRBS counters reaches the maximum value, the counter starts counting from zero again. PRBS mode is not applicable in Bridge Modes and should not be used.

9.3.6 Interrupt

The DP83869HM can be configured to generate an interrupt when changes of internal status occur. The interrupt allows a MAC to act upon the status in the PHY without polling the PHY registers. The interrupt source can be selected through the interrupt registers, MICR (0x0012) and FIBER_INT_EN (0x0C18). The interrupt status can be read from ISR (0x0013) and FIBER_INT_STTS (0x0C19) registers. Some interrupts are enabled by default and can be disabled through register access. Both the interrupt status registers must be read in order to clear pending interrupts. Until the pending interrupts are cleared, new interrupts may not be routed to the interrupt pin.

9.3.7 Power-Saving Modes

DP83869HM supports four power saving modes. The details are provided below.

9.3.7.1 IEEE Power Down

The PHY is powered down but access to the PHY through MDIO-MDC pins is retained. This mode can be activated by asserting external PWDN pin or by setting bit 11 of BMCR (Register 0x00).

The PHY can be taken out of this mode by a power cycle, software reset, or by clearing the bit 11 in BMCR register. However, the external PWDN pin should be deasserted. If the PWDN pin is kept asserted then the PHY remains in power down.

9.3.7.2 Active Sleep

In this mode, all the digital and analog blocks are powered down. The PHY is automatically powered up when a link partner is detected. This mode is useful for saving power when the link partner is down or inactive, but PHY cannot be powered down. In Active Sleep mode, the PHY still routinely sends NLP to the link partner. This mode can be active by writing binary 10 to bits [9:8] for PHYCR (Register 0x10). Sleep mode cannot be used when Auto-MDIX is on.

9.3.7.3 Passive Sleep

This is just like Active sleep except the PHY does not send NLP. This mode can be activated by writing binary 11 to bits [9:8] PHYCR (Register 0x10). Sleep mode cannot be used when Auto-MDIX is on.

9.3.8 Mirror Mode

In some applications, the orientation of the cable connector can require Copper PMD traces to cross over each other. This complicates the board layout. The DP83869HM can resolve this issue by implementing mirroring of the ports inside the device.

In 10/100 operation, the mapping of the port mirroring is shown in 表 5. When using mirror mode in 100-Mbps mode, TI recommends that the user read register 0xA1 and write the same value in register 0xA0.

表 5. Mirror Port Configurations in 10/100 Operation

MDI MODE	MIRROR PORT CONFIGURATION
MDI	A → D
	B → C
MDIX	A → D
	B → C

In Gigabit operation, the mapping of the port mirroring is shown in 表 6.

表 6. Mirror Port Configurations in Gigabit Operation

MDI MODE	MIRROR PORT CONFIGURATION
MDI or MDIX	A → D
	B → C
	C → B
	D → A

Mirror mode can be enabled through strap or through register configuration using the Port Mirror Enable bit in the CFG4 register (address 0x0031). In Mirror mode, the polarity of the signals is also reversed.

9.3.9 Speed Optimization

Speed optimization, also known as link downshift, enables fallback to 100M operation after multiple consecutive failed attempts at Gigabit link establishment. Such a case could occur if cabling with only four wires (two twisted pairs) were connected instead of the standard cabling with eight wires (four twisted pairs).

The number of failed link attempts before falling back to 100M operation is configurable. By default, four failed link attempts are required before falling back to 100M.

In enhanced mode, fallback to 100M can occur after one failed link attempt if energy is not detected on the C and D channels. Speed optimization also supports fallback to 10M if link establishment fails in Gigabit and in 100M mode.

Speed optimization can be enabled through register configuration.

9.3.10 Cable Diagnostics

With the vast deployment of Ethernet devices, the need for reliable, comprehensive and user-friendly cable diagnostic tool is more important than ever. The wide variety of cables, topologies, and connectors deployed results in the need to non-intrusively identify and report cable faults. The DP83869HM offers Time Domain Reflectometry (TDR) for Cable Diagnostics.

9.3.10.1 TDR

The DP83869HM uses Time Domain Reflectometry (TDR) to determine the quality of the cables, connectors, and terminations in addition to estimating the cable length. Some of the possible problems that can be diagnosed include opens, shorts, cable impedance mismatch, bad connectors, termination mismatches, cross faults, cross shorts, and any other discontinuities along the cable.

The DP83869HM transmits a test pulse of known amplitude down each of the two pairs of an attached cable. The transmitted signal continues down the cable and reflects from each cable imperfection, fault, bad connector, and from the end of the cable itself. After the pulse transmission, the DP83869HM measures the return time and amplitude of all these reflected pulses. This technique enables measuring the distance and magnitude (impedance) of non-terminated cables (open or short), discontinuities (bad connectors), improperly-terminated cables, and crossed pairs wires with ±1-m accuracy.

The DP83869HM also uses data averaging to reduce noise and improve accuracy. The DP83869HM can record up to five reflections within the tested pair. If more than 5 reflections are recorded, the DP83869HM saves the first 5 of them. If a cross fault is detected, the TDR saves the first location of the cross fault and up to 4 reflections in the tested channel. The DP83869HM TDR can measure cables beyond 100 m in length.

For all TDR measurements, the transformation between time of arrival and physical distance is done by the external host using minor computations (such as multiplication, addition, and lookup tables). The host must know the expected propagation delay of the cable, which depends, among other things, on the cable category (for example, CAT5, CAT5e, or CAT6).

TDR measurement is allowed in the DP83869HM in the following scenarios:

- While Link partner is disconnected – cable is unplugged at the other side
- Link partner is connected but remains *quiet* (for example, in power-down mode)
- TDR could be automatically activated when the link fails or is dropped by setting bit 7 of register 0x0009 (CFG1). The results of the TDR run after the link fails are saved in the TDR registers.

Software could read these registers at any time to apply post processing on the TDR results. This mode is designed for cases when the link is dropped due to cable disconnections. After a link failure, for instance, the line is quiet to allow a proper function of the TDR.

9.3.11 Fast Link Drop

The DP83869HM includes advanced link-down capabilities that support various real-time applications. The link down mechanism is configurable and includes enhanced modes that allow extremely fast reaction times to link drops.

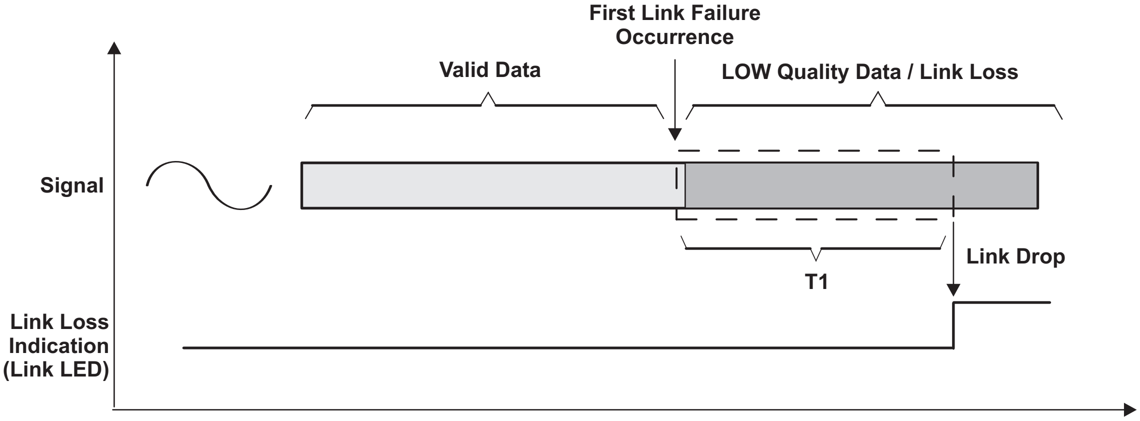


图 20. Fast Link Drop Mechanism

As described in 图 20, the link loss mechanism is based on a time window search period in which the signal behavior is monitored. The T1 window is set by default to reduce typical link drops to less than 1 ms in 100M and 0.5 ms in 1000M mode.

The DP83869HM supports enhanced modes that shorten the window called Fast Link Down mode. In this mode, the T1 window is shortened significantly, in most cases less than 10 μs. In this period of time, there are several criteria allowed to generate link loss event and drop the link:

1. Loss of descrambler sync
2. Receive errors
3. MLT3 errors
4. Mean Squared Error (MSE)
5. Energy loss

The Fast Link Down functionality allows the use of each of these options separately or in any combination. Note that because this mode enables extremely quick reaction time, it is more exposed to temporary bad link quality scenarios.

9.3.12 Jumbo Frames

Conventional Ethernet frames have a maximum size of about 1518 bytes. Jumbo Frames are special packets with size higher than 1518 bytes, often ranging into several thousands of bytes. Jumbo frames allow Ethernet systems to transfer large chunks of data in a single frame reducing the processor overhead and increasing bandwidth efficiency. DP83869 supports Jumbo frames in 1000Mbps and 100Mbps speeds.

9.4 Device Functional Modes

9.4.1 Copper Ethernet

9.4.1.1 1000BASE-T

The DP83869HM supports the 1000BASE-T standard as defined by the IEEE 802.3 standard. In 1000M mode, the PHY will use four MDI channels for communication. The 1000BASE-T can work in Auto-Negotiation mode. The PHY can be configured in 1000BASE-T through the register settings (*Register Configuration for Operational Modes*) or strap settings (*Strap for DP83869HM Functional Mode Selection*).

9.4.1.2 100BASE-TX

The DP83869HM supports the 100BASE-TX standard as defined by the IEEE 802.3 standard. In 100M mode, the PHY will use two MDI channels for communication. The 100BASE-TX can work in Auto-Negotiation mode or in force mode. The PHY can be configured in 100BASE-TX through the register settings (*Register Configuration for Operational Modes*) or strap settings (*Strap for DP83869HM Functional Mode Selection*). When using DP83869 in force 100Base-TX mode, it is required to enable Robust Auto-MDIX feature from register 0x1E.

9.4.1.3 10BASE-Te

The DP83869HM supports the 10BASE-Te standard as defined by the IEEE 802.3 standard. In 100M mode, the PHY will use two MDI channels for communication. The 10BASE-Te can work in Auto-Negotiation mode or in force mode. The PHY can be configured in 10BASE-Te through the register settings (*Register Configuration for Operational Modes*) or strap settings (*Strap for DP83869HM Functional Mode Selection*).

9.4.2 Fiber Ethernet

9.4.2.1 1000BASE-X

The DP83869HM supports the 1000Base-X Fiber Ethernet protocol as defined in IEEE 802.3 standard. In 1000M Fiber mode, the PHY will use two differential channels for communication. In fiber mode, the speed is not decided through auto-negotiation. Both sides of the link must be configured to the same operating speed. The PHY can be configured to operate in 1000BASE-X through the register settings (*Register Configuration for Operational Modes*) or strap settings (*Strap for DP83869HM Functional Mode Selection*).

In 1000Base-X Fiber applications, a MAC will often read the link status of the PHY before initiating data transfer. In rare cases, MAC intervention is required to ensure 1000Base-X link up. It is recommended to use the application note *DP83869 1000Base-X Link Detection (SNLA305)* for identifying 1000Base-X link. This approach is not needed in 100BASE-FX mode.

9.4.2.2 100BASE-FX

The DP83869HM supports the 100Base-FX Fiber Ethernet protocol as defined in IEEE 802.3 standard. In 100M Fiber mode, the PHY will use two differential channels for communication. In fiber mode, the speed is not decided through auto-negotiation. Both sides of the link must be configured to the same operating speed. The PHY can be configured to operate in 100BASE-X through register settings (*Register Configuration for Operational Modes*) or strap settings (*Strap for DP83869HM Functional Mode Selection*).

9.4.3 Serial GMII (SGMII)

The Serial Gigabit Media Independent Interface (SGMII) provides a means of conveying network data and port speed between a 100/1000 PHY and a MAC with significantly less signal pins (4 or 6 pins) than required for GMII (24 pins) or RGMII (12 pins). The SGMII interface uses 1.25-Gbps LVDS differential signaling which has the added benefit of reducing EMI emissions relative to GMII or RGMII.

Because the internal clock and data recovery circuitry (CDR) of DP83869HM can detect the transmit timing of the SGMII data, TX_CLK is not required. The DP83869HM will support only 4-wire SGMII mode. Two differential pairs are used for the transmit and receive connections. Clock and data recovery are performed in the MAC and in the PHY, so no additional differential pair is required for clocking.

Device Functional Modes (接下页)

The 1.25-Gbps rate of SGMII is excessive for 100-Mbps and 10-Mbps operation. When operating in 100-Mbps mode, the PHY *elongates* the frame by replicating each frame byte 10 times and when in 10-Mbps mode the PHY *elongates* the frame by replicating each frame byte 100 times. This frame elongation takes place *above* the IEEE 802.3 PCS layer, thus the start of frame delimiter only appears once per frame.

The SGMII interface includes Auto-Negotiation capability. Auto-Negotiation provides a mechanism for control information to be exchanged between the PHY and the MAC. This allows the interface to be automatically configured based on the media speed mode resolution on the MDI side. In MAC loopback mode, the SGMII speed is determined by the MDI speed selection. The SGMII interface works in both Auto-Negotiation and forced speed mode during the MAC loopback operation. SGMII Auto-Negotiation is the default mode of the operation.

The SGMII Auto-Negotiation process can be disabled and the SGMII speed mode can be forced to the MDI resolved speed. The SGMII forced speed mode can be enabled with the MDI auto-negotiation or MDI manual speed mode. SGMII Auto-Negotiation can be disabled through the SGMII_AUTONEG_EN register bit in the CFG2 register (address 0x0014).

The 10M_SGMII_RATE_ADAPT bit (bit 7) of 10M_SGMII_CFG register (0x016F) needs to be cleared for enabling 10M SGMII operation.

SGMII is enabled through a resistor strap option. See *Strap Configuration* for details.

All SGMII connections must be AC-coupled through an 0.1-µF capacitor.

The connection diagrams for 4-wire SGMII is shown in 图 21.

注

MII Isolate (bit 10 in register 0x0000) will not isolate SGMII pins. SGMII can be disabled through register 0x01DF for isolating SGMII pins.

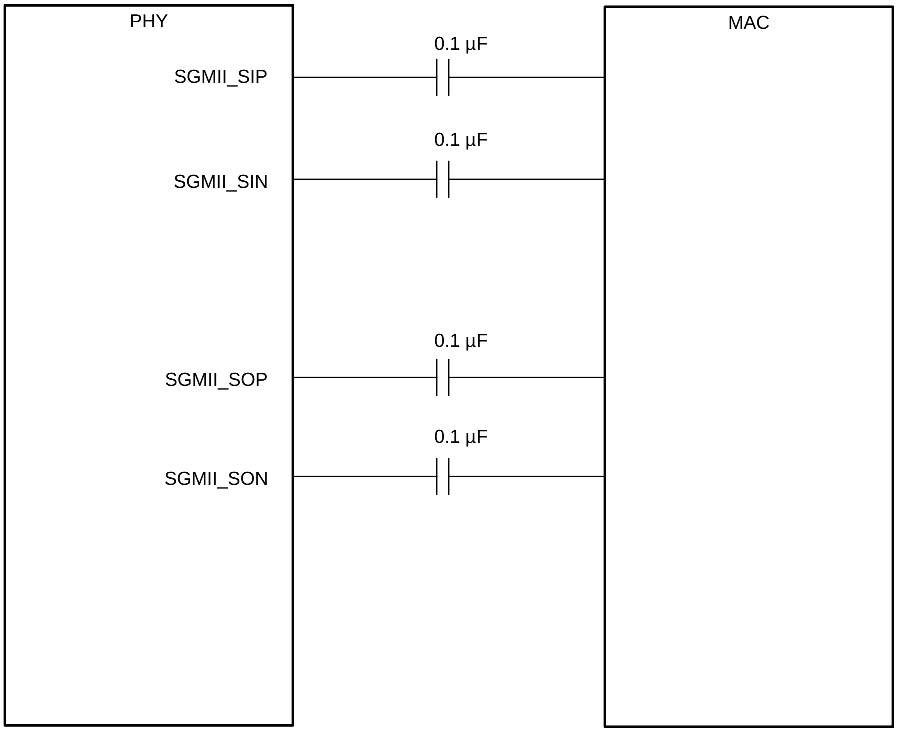


图 21. SGMII 4-Wire Connections

Device Functional Modes (接下页)

9.4.4 Reduced GMII (RGMII)

The Reduced Gigabit Media Independent Interface (RGMII) is designed to reduce the number of pins required to interconnect the MAC and PHY (12 pins for RGMII relative to 24 pins for GMII). To accomplish this goal, the data paths and all associated control signals are reduced and are multiplexed. Both rising and trailing edges of the clock are used. For Gigabit operation, the GTX_CLK and RX_CLK clocks are 125 MHz, and for 10- and 100-Mbps operation, the clock frequencies are 2.5 MHz and 25 MHz, respectively.

For more information about RGMII timing, see the *RGMII Interface Timing Budgets* application report (SNLA243).

9.4.4.1 1000-Mbps Mode Operation

All RGMII signals are positive logic. The 8-bit data is multiplexed by taking advantage of both clock edges. The lower 4 bits are latched on the positive clock edge and the upper 4 bits are latched on trailing clock edge. The control signals are multiplexed into a single clock cycle using the same technique.

To reduce power consumption of RGMII interface, (TX_EN - TX_ERR) and (RX_DV - RX_ERR) are encoded in a manner that minimizes transitions during normal network operation. TX_CTRL pin will denote TX_EN on rising edge of GTX_CLK and will denote a logic derivative of TX_EN and TX_ERR on the falling edge of GTX_CLK. RX_CTRL will denote RX_DV on rising edge of RX_CLK and will denote a logic derivative of RX_DV and RX_ERR on the falling edge of RX_CLK. The encoding for the TX_ERR and RX_ERR is given in 公式 1 and 公式 2:

TX_ERR = GMII_TX_ER (XOR) GMII_TX_EN

where

- GMII_TX_ER and GMII_TX_EN are logical equivalent signals in GMII standard. (1)

RX_ERR = GMII_RX_ER (XOR) GMII_RX_DV

where

- GMII_RX_ER, and GMII_RX_DV are logical equivalent signals in GMII standard. (2)

When receiving a valid frame with no error, *RX_CTRL = True* is generated as a logic high on the rising edge of RX_CLK and *RX_CTRL = False* is generated as a logic high at the falling edge of RX_CLK. When no frame is being received, *RX_CTRL = False* is generated as a logic low on the rising edge of RX_CLK and *RX_CTRL = False* is generated as a logic low on the falling edge of RX_CLK.

The TX_CTRL is treated in a similar manner. During normal frame transmission, the signal stays at a logic high for both edges of GTX_CLK and during the period between frames where no error is indicated, the signal stays low for both edges.

9.4.4.2 1000-Mbps Mode Timing

The DP83869HM provides configurable clock skew for the GTX_CLK and RX_CLK to optimize timing across the interface. The transmit and receive paths can be optimized independently. Both the transmit and receive path support 16 programmable RGMII delay modes through register configuration.

The timing paths can either be configured for Aligned mode or Shift mode. In Aligned mode, no clock skew is introduced. In Shift mode, the clock skew can be introduced in 0.5-ns increments or in 0.25-ns increments (through register configuration). Configuration of the Aligned mode or Shift mode is accomplished through the RGMII Control Register (RGMIICTL), address 0x0032. In Shift mode, the clock skew can be adjusted using the RGMII Delay Control Register (RGMIIDCTL), address 0x0086. By default RGMII shift mode will be activated. Both transmit and receive signals will be delayed by 2ns.

9.4.4.3 10- and 100-Mbps Mode

When the RGMII interface is operating in the 100-Mbps mode, the RGMII clock rate is reduced to 25 MHz. For 10-Mbps operation, the clock is further reduced to 2.5 MHz. In the RGMII 10/100 mode, the transmit clock RGMII TX_CLK is generated by the MAC and the receive clock RGMII RX_CLK is generated by the PHY. During the packet receiving operation, the RGMII RX_CLK may be stretched on either the positive or negative pulse to accommodate the transition from the free-running clock to a data synchronous clock domain. When the speed of the PHY changes, a similar stretching of the positive or negative pulses is allowed. No glitch is allowed on the clock signals during clock speed transitions.

Device Functional Modes (接下页)

This interface operates at 10- and 100-Mbps speeds the same way it does at 1000-Mbps mode with the exception that the data may be duplicated on the falling edge of the appropriate clock.

The MAC holds the RGMII TX_CLK low until it has ensured that it is operating at the same speed as the PHY.

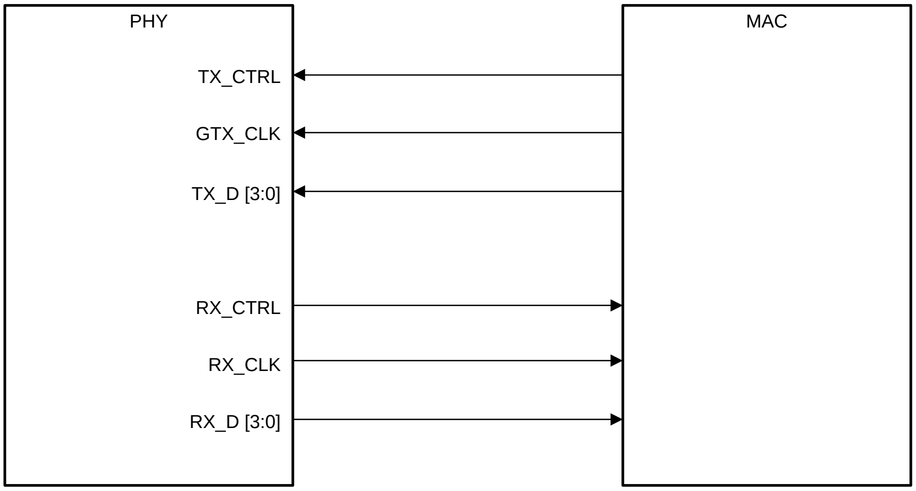


图 22. RGMII Connections

9.4.5 Media Independent Interface (MII)

DP83869HM also supports MII mode when the PHY is working in 100M and 10M speeds. The user will have to ensure that the PHY links in either 100-Mbps or 10-Mbps mode. MII mode cannot be used in 1000-Mbps mode. When using auto-negotiation to resolve MDI speed, TI recommends to turn off the gigabit speed advertisement through register 0x0009 to ensure that the PHY does not link up at 1000-Mbps speed. The Media Independent Interface is a synchronous 4-bit wide nibble data interface that connects the PHY to the MAC in 100BASE-FX, 100BASE-TX and 10BASE-Te modes. The MII is fully compliant with IEEE 802.3-2002 clause 22.

The MII signals are summarized in 表 7:

表 7. MII Signals

FUNCTION	PINS
Data Signals	TX_D[3:0]
	RX_D[3:0]
Transmit and Receive Signals	TX_EN, TX_ER
	RX_DV, RX_ER

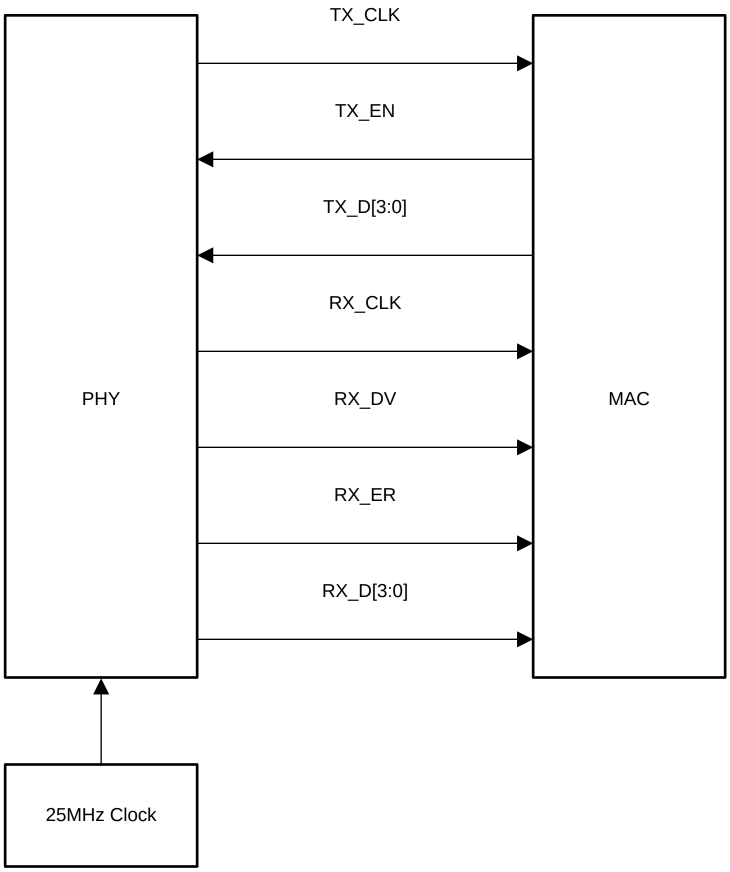


图 23. MII Signaling

9.4.6 Bridge Modes

The DP83869HM supports Bridge modes to translate data between two MAC interface types. Bridge mode is activated through straps or register configuration. The two types of Bridge mode supported by DP83869HM are:

RGMII-to-SGMII mode
SGMII-to-RGMII mode

9.4.6.1 RGMII-to-SGMII Mode

图 24. DP83869HM RGMII-to-SGMII Bridge

In RGMII-to-SGMII mode Ethernet MAC is connected to the RGMII pins of the DP83869HM and PHY is connected to the SGMII pins of the DP83869. In this mode, DP83869HM will configure SGMII in Auto Mode. In Auto mode, the RGMII side will automatically adjust to the link-up speed on the SGMII side. In case where the PHY is does not have a link, the RGMII clock frequency will default to 2.5 MHz.

After auto-negotiation is completed on the PHY side, the link capabilities are communicated to DP83869HM over the SGMII interface. However, this information is conveyed to the Ethernet MAC through RGMII Inband signaling and RX_CLK adjustment. The MAC can also read this information from the DP83869.

In Bridge mode, the DP83869HM SMI will act as slave mode to MAC.

9.4.6.2 *SGMII-to-RGMII Mode*

图 25. DP83869HM SGMII-to-RGMII Bridge

In SGMII-to-RGMII mode, Ethernet MAC is connected to the SGMII pins of the DP83869HM and PHY is connected to the RGMII pins of the DP83869. In this mode, DP83869HM will configure SGMII in Auto. In Auto mode, SGMII will adapt the link speed based on RGMII.

After auto-negotiation is completed on the PHY side, the link capabilities are communicated to DP83869HM over the RGMII interface. However, this information needs to be conveyed to the Ethernet MAC as well. The MAC can read this information from the DP83869HM through the registers.

In Bridge mode, DP83869HM SMI will act as slave mode to MAC. RGMII interface pins will be reversed in this case, TX pins will behave as RX (input data pins) and RX pins will behave as TX (output data pins). This will account for the fact that DP83869HM will act as RGMII MAC for the Ethernet PHY.

In both Bridge modes, PRBS mode of the PHY is not applicable and should not be used.

LEDs, if used, will indicate status on the RGMII side in both Bridge Modes.

9.4.7 Media Convertor Mode

In media convertor mode, DP83869HM will translate data between copper and fiber interface for 1000M and 100M speeds. Media convertor mode can be activated through the straps. The DP83869HM supports Managed Media Convertor mode.

图 26. Media Convertor Mode

In Managed mode, Media Convertor can still be activated via straps but register configuration option are also used. When Media Convertor Mode is enabled then bit [0] of register 0x01EC should be set to 0. Enhanced features like changing LED configuration, Capabilities programming broadcasted in Auto-Neg etc may need configuration and are supported through register programming. Register access to the PHY is retained. This provides additional flexibility to use other features supported by the PHY.

1000BASE-X link needs monitoring in the rare case that link is not established. It is recommended to use the application note *DP83869 1000Base-X Link Detection (SNLA305)* for identifying 1000Base-X link. This monitoring is not needed in 100M media convertor mode.

Copper interface will support auto-negotiation, but the user will have to ensure that the speed negotiated on the copper side matches the speed fixed on the fiber side. In cases of speed mismatch between copper and fiber, interface data transmission will not be successful.

The DP83869HM also supports Link Loss Pass Through in 100M mode. In a network containing two media convertors where the link is dropped on one end of the system, a link loss indication is passed through all the way to the far end. The Link Loss Pass-Through is enabled or disabled through straps. An example is shown in 图 27.

1. A fault occurs on copper link at position 1 at Near End Link Partner.
2. Media Converter will disable Fiber TX link at position 2.
3. The Media Converter in the system will lose link at position 3.
4. The second Media Converter disables copper link and the far end link partner loses the copper link.

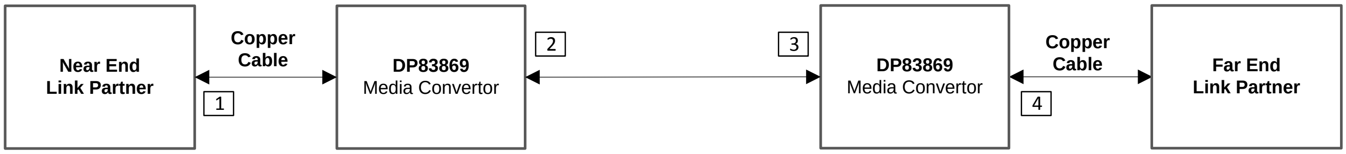


图 27. Link Loss Pass-Through

9.4.8 Register Configuration for Operational Modes

The operational modes of DP83869HM are configured through the OPMODE_0, OPMODE_1, OPMODE_2 straps. When operational modes are changed through register access, additional configurations are necessary apart from 0x01DF. The following sections contain necessary information for changing operational modes through the registers. For modes not listed below, only configuring register 0x01DF is sufficient.

9.4.8.1 RGMII-to-Copper Ethernet Mode

After configuring register 0x01DF, perform the following operations.

- Write 0x1140 to register 0x0000
- Write 0x5048 to register 0x0010
- Write 0x0B00 to register 0x0009

9.4.8.2 RGMII-to-1000Base-X Mode

After configuring register 0x01DF, perform the following operations.

- Write 0x1140 to register 0x0000

9.4.8.3 RGMII-to-SGMII Bridge Mode

After configuring register 0x01DF, perform the following operations.

- Write 0x1140 to register 0x0C00

9.4.8.4 1000M Media Convertor Mode

After configuring register 0x01DF, perform the following operations.

- Write 0x1140 to register 0x0000
- Write 0x5048 to register 0x0010
- Write 0x1140 to register 0x0C00 9

9.4.8.5 100M Media Convertor Mode

After configuring register 0x01DF, perform the following operations.

- Write 0x1140 to register 0x0000
- Write 0x5048 to register 0x0010

9.4.8.6 SGMII-to-Copper Ethernet Mode

After configuring register 0x01DF, perform the following operations.

- Write 0x1140 to register 0x0000
- Write 0x5048 to register 0x0010
- Write 0x0B00 to register 0x0009
- Write 0x1140 to register 0x0C00

9.4.9 Serial Management Interface

The Serial Management Interface (SMI), provides access to the DP83869HM internal register space for status information and configuration. The SMI is compatible with IEEE 802.3-2002 clause 22. The implemented register set consists of the registers required by the IEEE 802.3, plus several others to provide additional visibility and controllability of the DP83869HM device.

The SMI includes the MDC management clock input and the management MDIO data pin. The MDC clock is sourced by the external management entity, also called Station (STA), and can run at a maximum clock rate of 25 MHz. MDC is not expected to be continuous, and can be turned off by the external management entity when the bus is idle.

The MDIO is sourced by the external management entity and by the PHY. The data on the MDIO pin is latched on the rising edge of the MDC clock. The MDIO pin requires a pullup resistor (2.2 kΩ) which, during IDLE and turnaround, pulls MDIO high.

Up to 32 PHYs can share a common SMI bus. To distinguish between the PHYs, a 5-bit address is used. During power-up reset, the DP83869HM latches the PHY_ADD configuration pins to determine its address.

The management entity must not start an SMI transaction in the first cycle after power-up reset. To maintain valid operation, the SMI bus must remain inactive at least one MDC cycle after hard reset is deasserted. In normal MDIO transactions, the register address is taken directly from the management-frame reg_addr field, thus allowing direct access to 32 16-bit registers (including those defined in IEEE 802.3 and vendor specific). The data field is used for both reading and writing. The Start code is indicated by a <01> pattern. This pattern makes sure that the MDIO line transitions from the default idle line state. Turnaround is defined as an idle bit time inserted between the Register Address field and the Data field. To avoid contention during a read transaction, no device may actively drive the MDIO signal during the first bit of turnaround. The addressed DP83869HM drives the MDIO with a zero for the second bit of turnaround and follows this with the required data. 图 28 shows the timing relationship between MDC and the MDIO as driven and received by the Station (STA) and the DP83869HM (PHY) for a typical register read access.

For write transactions, the station-management entity writes data to the addressed DP83869, thus eliminating the requirement for MDIO turnaround. The turnaround time is filled by the management entity by inserting <10>. 图 28 shows the timing relationship for a typical MII register write access. The frame structure and general read and write transactions are shown in 表 8, 图 28, and 图 29.

表 8. Typical MDIO Frame Format

TYPICAL MDIO FRAME FORMAT	<idle><start><op code><device addr><reg addr><turnaround><data<<idle>
Read Operation	<idle><01><10><AAAA><RRRR><Z0><xxxx xxxx xxxx xxxx><idle>
Write Operation	<idle><01<01><AAAA><RRRR><10><xxxx xxxx xxxx xxxx><idle>

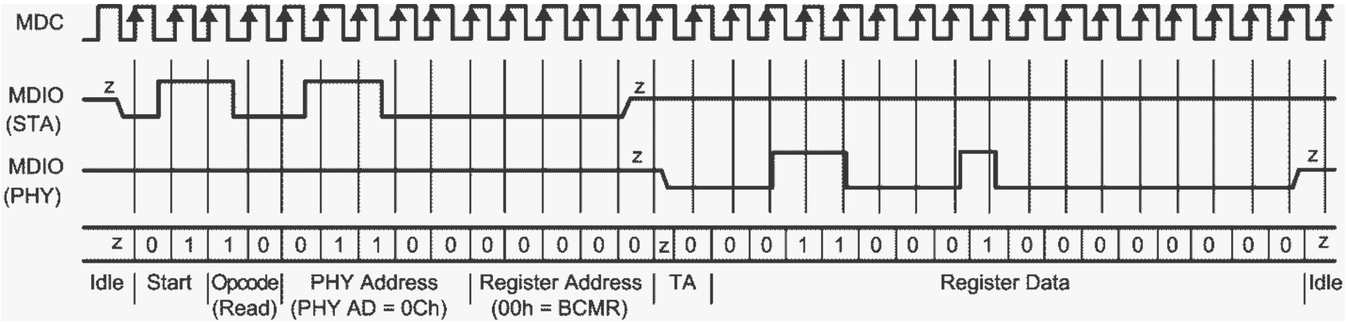


图 28. Typical MDC/MDIO Read Operation

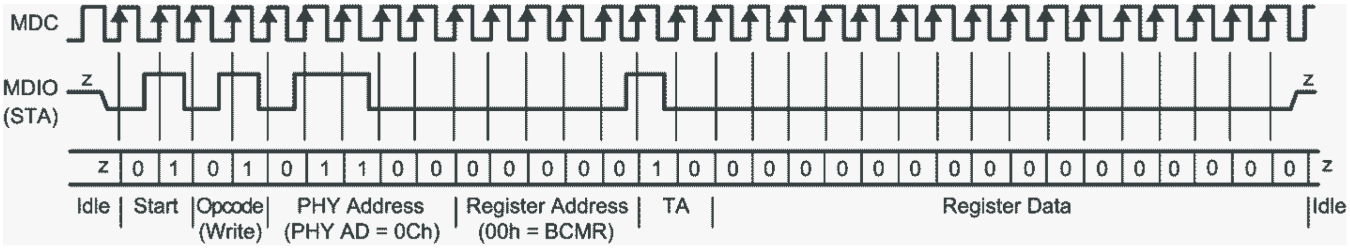


图 29. Typical MDC/MDIO Write Operation

9.4.9.1 Extended Address Space Access

The DP83869HM SMI function supports read or write access to the extended register set using registers REGCR (0x000Dh) and ADDAR (0x000Eh) and the MDIO Manageable Device (MMD) indirect method defined in IEEE 802.3ah Draft for clause 22 for accessing the clause 45 extended register set.

The standard register set, MDIO registers 0 to 31, is accessed using the normal direct-MDIO access or the indirect method, except for register REGCR (0x000Dh) and ADDAR (0x000Eh) which is accessed only using the normal MDIO transaction. The SMI function ignores indirect accesses to these registers.

REGCR (0x000Dh) is the MDIO Manageable MMD access control. In general, register REGCR(4:0) is the device address DEVAD that directs any accesses of ADDAR (0x000Eh) register to the appropriate MMD.

The DP83869HM supports one MMD device address. The vendor-specific device address DEVAD[4:0] = 11111 is used for general MMD register accesses.

All accesses through registers REGCR and ADDAR must use the correct DEVAD. Transactions with other DEVAD are ignored. REGCR[15:14] holds the access function: address (00), data with no post increment (01), data with post increment on read and writes (10) and data with post increment on writes only (11).

- ADDAR is the address and data MMD register. ADDAR is used in conjunction with REGCR to provide the access to the extended register set. If register REGCR[15:1] is 00, then ADDAR holds the address of the extended address space register. Otherwise, ADDAR holds the data as indicated by the contents of its address register. When REGCR[15:14] is set to 00, accesses to register ADDAR modify the extended register set address register. This address register must always be initialized to access any of the registers within the extended register set.
- When REGCR[15:14] is set to 01, accesses to register ADDAR access the register within the extended register set selected by the value in the address register.
- When REGCR[15:14] is set to 10, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for both reads and writes, the value in the address register is incremented.
- When REGCR[15:14] is set to 11, access to register ADDAR access the register within the extended register set selected by the value in the address register. After that access is complete, for write accesses only, the value in the address register is incremented. For read accesses, the value of the address register remains unchanged.

The following sections describe how to perform operations on the extended register set using register REGCR and ADDAR. The descriptions use the device address for general MMD register accesses (DEVAD[4:0] = 11111).

9.4.9.1.1 Write Address Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.

Subsequent writes to register ADDAR (step 2) continue to write the address register.

9.4.9.1.2 Read Address Operation

To read the address register:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Read the register address from register ADDAR.

9.4.9.1.3 Write (No Post Increment) Operation

To write a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) continue to rewrite the register selected by the value in the address register.

Note: steps (1) and (2) can be skipped if the address register was previously configured.

9.4.9.1.4 Read (No Post Increment) Operation

To read a register in the extended register set:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x401F (data, no post increment function field = 01, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads from register ADDAR (step 4) continue reading the register selected by the value in the address register.

Note: steps (1) and (2) can be skipped if the address register was previously configured.

9.4.9.1.5 Write (Post Increment) Operation

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the register address from register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) or the value 0xC01F (data, post increment on writes function field = 11. DEVAD = 31) to register REGCR.
4. Write the content of the desired extended register set register to register ADDAR.

Subsequent writes to register ADDAR (step 4) write the next higher addressed data register selected by the value of the address register. The address register is incremented after each access.

9.4.9.1.6 Read (Post Increment) Operation

To read a register in the extended register set and automatically increment the address register to the next higher value following the write operation:

1. Write the value 0x001F (address function field = 00, DEVAD = 31) to register REGCR.
2. Write the desired register address to register ADDAR.
3. Write the value 0x801F (data, post increment on reads and writes function field = 10, DEVAD = 31) to register REGCR.
4. Read the content of the desired extended register set register to register ADDAR.

Subsequent reads to register ADDAR (step 4) read the next higher addressed data register selected by the value of the address register. The address register is incremented after each access.

9.4.9.1.7 Example of Read Operation Using Indirect Register Access

Read register 0x0170.

1. Write register 0x0D to value 0x001F.
2. Write register 0x0E to value 0x0170
3. Write register 0x0D to value 0x401F.
4. Read register 0x0E.

The expected default value is 0x0C10.

9.4.9.1.8 Example of Write Operation Using Indirect Register Access

Write register 0x0170 to value 0x0C50.

1. Write register 0x0D to value 0x001F.
2. Write register 0x0E to value 0x0170
3. Write register 0x0D to value 0x401F.
4. Write register 0x0E to value 0x0C50.

This write disables the output clock on the CLK_OUT pin.

9.4.10 Auto-Negotiation

All 1000BASE-T PHYs are required to support Auto-Negotiation. The Auto-Negotiation function in 1000BASE-T has three primary purposes:

- Auto-Negotiation of Speed and Duplex Selection
- Auto-Negotiation of Master or Slave Resolution
- Auto-Negotiation of Pause or Asymetrical Pause Resolution

9.4.10.1 Speed and Duplex Selection - Priority Resolution

The Auto-Negotiation function provides a mechanism for exchanging configuration information between the two ends of a link segment. This mechanism is implemented by exchanging Fast Link Pulses (FLP). FLPs are burst pulses that provide the signaling used to communicate the abilities between two devices at each end of a link segment. For further details regarding Auto-Negotiation, refer to Clause 28 of the IEEE 802.3 specification. The DP83869HM supports 1000BASE-T, 100BASE-TX, and 1000BASE-T modes of operation. The process of Auto-Negotiation ensures that the highest performance protocol is selected (that is, priority resolution) based on the advertised abilities of the Link Partner and the local device.

9.4.10.2 Master and Slave Resolution

If 1000BASE-T mode is selected during the priority resolution, the second goal of Auto-Negotiation is to resolve Master or Slave configuration. The Master mode priority is given to the device that supports multiport nodes, such as switches and repeaters. Single node devices such as DTE or NIC card takes lower Master mode priority.

9.4.10.3 Pause and Asymmetrical Pause Resolution

When Full-Duplex operation is selected during priority resolution, the Auto-Negotiation also determines the Flow Control capabilities of the two link partners. Flow control was originally introduced to force a busy station’s Link Partner to stop transmitting data in Full-Duplex operation. Unlike Half-Duplex mode of operation where a link partner could be forced to back off by simply generating collisions, the Full-Duplex operation needed a mechanism to slow down transmission from a link partner in the event that the receiving station’s buffers are becoming full. A new MAC control layer was added to handle the generation and reception of Pause Frames. Each MAC Controller has to advertise whether it is capable of processing Pause Frames. In addition, the MAC Controller advertises if Pause frames can be handled in both directions, that is, receive and transmit. If the MAC Controller only generates Pause frames but does not respond to Pause frames generated by a link partner, it is called Asymmetrical Pause. The advertisement of Pause and Asymmetrical Pause capabilities is enabled by writing 1 to bits 10 and 11 of ANAR (register address 0x0004). The link partner’s Pause capabilities is stored in ANLPAR (register address 0x0005) bits 10 and 11. The MAC Controller has to read from ANLPAR to determine which Pause mode to operate. The PHY layer is not involved in Pause resolution other than simply advertising and reporting of Pause capabilities.

9.4.10.4 Next Page Support

The DP83869HM supports the Auto-Negotiation Next Page protocol as required by IEEE 802.3 clause 28.2.4.1.7. The ANNPTR 0x07 allows for the configuration and transmission of the Next Page. Refer to clause 28 of the IEEE 802.3 standard for detailed information regarding the Auto-Negotiation Next Page function.

9.4.10.5 Parallel Detection

The DP83869HM supports the Parallel Detection function as defined in the IEEE 802.3 specification. Parallel Detection requires the 10/100-Mbps receivers to monitor the receive signal and report link status to the Auto-Negotiation function. Auto-Negotiation uses this information to configure the correct technology in the event that the Link Partner does not support Auto-Negotiation, yet is transmitting link signals that the 10BASE-Te or 100BASE-X PMA recognize as valid link signals.

If the DP83869HM completes Auto-Negotiation as a result of Parallel Detection without Next Page operation, bits 5 and 7 of ANLPAR (register address 0x0005) are set to reflect the mode of operation present in the Link Partner. Note that bits 4:0 of the ANLPAR are also set to 00001 based on a successful parallel detection to indicate a valid 802.3 selector field. Software may determine that the negotiation is completed through Parallel Detection by reading 0 in bit 0 of ANER (register address 0x006) after Auto-Negotiation Complete—bit 5 of BMSR (register address 0x0001)—is set. If the PHY is configured for parallel detect mode and any condition other than a good link occurs, the parallel detect fault—bit 4 of ANER (register address 0x06)—sets.

9.4.10.6 Restart Auto-Negotiation

If a link is established by successful Auto-Negotiation and then lost, the Auto-Negotiation process resumes to determine the configuration for the link. This function ensures that a link can be re-established if the cable becomes disconnected and reconnected. After Auto-Negotiation is completed, it may be restarted at any time by writing 1 to bit 9 of the BMCR (register address 0x0000). A restart Auto-Negotiation request from any entity, such as a management agent, causes DP83869HM to halt data transmission or link pulse activity until the break_link_timer expires. Consequently, the Link Partner goes into link fail mode and the resume Auto-Negotiation. The DP83869HM resumes Auto-Negotiation after the break_link_timer has expired by transmitting FLP (Fast Link Pulse) bursts.

9.4.10.7 Enabling Auto-Negotiation Through Software

If Auto-Negotiation is disabled by MDIO access, and the user desires to restart Auto-Negotiation, this could be accomplished by software access. Bit 12 of BMCR (register address 0x00) should be cleared and then set for Auto-Negotiation operation to take place.

If Auto-Negotiation is disabled by strap option, Auto-Negotiation cannot be re-enabled.

9.4.10.8 Auto-Negotiation Complete Time

Parallel detection and Auto-Negotiation typically take 2-3 seconds to complete. In addition, Auto-Negotiation with next page exchange takes approximately 2-3 seconds to complete, depending on the number of next pages exchanged. Refer to Clause 28 of the IEEE 802.3 standard for a full description of the individual timers related to Auto-Negotiation.

9.4.10.9 Auto-MDIX Resolution

The DP83869HM can determine if a *straight* or *crossover* cable is used to connect to the link partner. It can automatically re-assign channel A and B to establish link with the link partner, (and channel C and D in 1000BASE-T mode). Auto-MDIX resolution precedes the actual Auto-Negotiation process that involves exchange of FLPs to advertise capabilities. Automatic MDI/MDIX is described in IEEE 802.3 Clause 40, section 40.8.2. It is not a required implementation for 10BASE-Te and 100BASE-TX.

Auto-MDIX can be enabled or disabled by strap, using the AMDIX Disable strap, or by register configuration, using bit 6 of the PHYCR register (address 0x0010). When Auto-MDIX is disabled, the PMA is forced to either MDI (*straight*) or MDIX (*crossed*). Manual configuration of MDI or MDIX can also be accomplished by strap, using the Force MDI/X strap, or by register configuration, using bit 5 of the PHYCR register.

For 10/100, Auto-MDIX is independent of Auto-Negotiation. Auto-MDIX works in both Auto-Negotiation mode and manual forced speed mode.

9.5 Programming

9.5.1 Strap Configuration

The DP83869HM uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset. The strap option pin assignments are defined below.

Configuration of the device may be done through the strap pins or through the management register interface. A pullup resistor and/or a pulldown resistor of suggested values may be used to set the voltage ratio of the strap pin input and the supply to select one of the possible selected modes.

The MAC interface pins must support I/O voltages of 3.3 V, 2.5 V, and 1.8 V. As the strap inputs are implemented on these pins, the straps must also support operation at 3.3-V, 2.5-V, and 1.8-V supplies depending on what voltage was selected for I/O. RX_D0 and RX_D1 pins are 4 level strap pins. All other strap pins have two levels.

Programming (接下页)

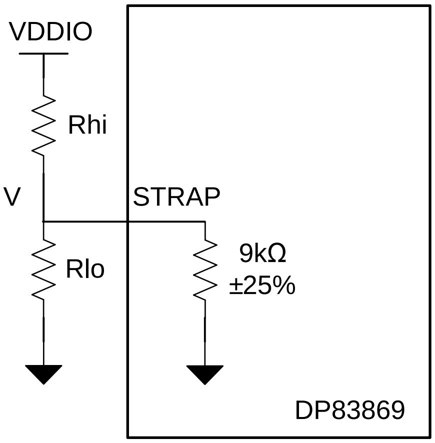


图 30. Strap Circuit

表 9. 4-Level Strap Resistor Ratio

MODE	TARGET VOLTAGE			IDEAL RESISTORS	
	Vmin (V)	**Vtyp (V)**	**Vmax (V)**	**Rhi (kΩ)**	**Rlo (kΩ)**
0	0	0	0.093 × VDDIO	OPEN	OPEN
1	0.136 × VDDIO	0.165 × VDDIO	0.184 × VDDIO	10	2.49
2	0.219 × VDDIO	0.255 × VDDIO	0.280 × VDDIO	5.76	2.49
3	0.6 × VDDIO	0.783 × VDDIO	0.888 × VDDIO	2.49	OPEN

表 10. 2-Level Strap Resistor Ratio

MODE	TARGET VOLTAGE			IDEAL RESISTORS	
	Vmin (V)	**Vtyp (V)**	**Vmax (V)**	**Rhi (kΩ)**	**Rlo (kΩ)**
0	0		0.18 x VDDIO	OPEN	2.49
1	0.5 x VDDIO		0.88 x VDDIO	2.49	OPEN

9.5.1.1 Straps for PHY Address

表 11. PHY Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT			
RX_D0	PHY_ADD[1:0]	33	00		PHY_ADD1	PHY_ADD0
				MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1
RX_D1	PHY_ADD[3:2]	34	00		PHY_ADD3	PHY_ADD2
				MODE 0	0	0
				MODE 1	0	1
				MODE 2	1	0
				MODE 3	1	1

9.5.1.2 *Strap for DP83869HM Functional Mode Selection*

表 12. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMODE_2	OPMODE_1	OPMODE_0	FUNCTIONAL MODES
JTAG_TDO/GPIO_1	OPMODE_0	22	0	0	0	0	RGMII to Copper(1000Base-T/100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE_1	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
RX_D2	OPMODE_2	35	0	1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-T to 100Base-FX
				1	1	0	SGMII to Copper(1000Base-T/100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

9.5.1.3 *Straps for RGMII/SGMII to Copper*

表 13. Copper Ethernet Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT				
LED_0	ANEG_DIS	47	0	**ANEG_DIS**	**ANEGSEL_1**	**ANEGSEL_0**	**FUNCTION**
				0	0	0	Auto-negotiation, 1000/100/10 advertised, Auto MDI-X
				0	0	1	Auto-negotiation, 1000/100 advertised, Auto MDI-X
LED_1	ANEGSEL_0	46	0	0	1	0	Auto-negotiation, 100/10 advertised, Auto-MDI-X
				0	1	1	NA
				1	0	0	NA
LED_2	ANEGSEL_1	45	0	1	0	1	NA
				1	1	0	Forced 100M, full duplex, MDI mode
				1	1	1	Forced 100M, full duplex, MDI-X mode
RX_CTRL	MIRROR_EN	38	0	0			Port Mirroring Disabled
				1			Port Mirroring Enabled

9.5.1.4 *Straps for RGMII to 1000Base-X*

表 14. 1000Base-X Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
LED_0	ANEG_DIS	47	0	0	Fiber Auto-negotiation ON
				1	Fiber Force mode
LED_1	ANEGSEL_0	46	0	0	Signal Detect disable on Pin 24
				1	Configure Pin 24 as Signal Detect Pin

9.5.1.5 Straps for RGMII to 100Base-FX

表 15. 100Base-X Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
LED_1	ANEGSEL_0	46	0	0	Signal Detect disable on Pin 24
				1	Configure Pin 24 as Signal Detect Pin

9.5.1.6 Straps for Bridge Mode (SGMII-RGMII)

表 16. Bridge Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT		
RX_CTRL	MIRROR_EN	38	0	0	RGMII to SGMII (RGMII : MAC I/F, SGMII : Phy I/F)
				1	SGMII to RGMII (SGMII : MAC I/F, RGMII : Phy I/F)

9.5.1.7 Straps for 100M Media Convertor

表 17. 100M Media Convertor Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT			
LED_1	ANEGSEL_0	46	0	**ANEGSEL_1**	**ANEGSEL_0**	
LED_2	ANEGSEL_1	45	0	0	0	Copper : Auto-negotiation (100/10 Advertised), Auto MDIX
				1	1	Copper : Auto Negotiation (100 Advertised), Auto MDIX
RX_CTRL	MIRROR_EN	38	0	0		Copper: Mirror Disable
				1		Copper: Mirror Enable
RX_CLK	LINK_LOSS	32	0	0		Link Loss Pass Thru Enabled
				1		Link Loss Pass Thru Disabled

9.5.1.8 Straps for 1000M Media Convertor

表 18. 1000M Media Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT			
LED_0	ANEG_DIS	47	0	0		Fiber Auto Negotiation
				1		Fiber Force Mode
LED_1	ANEGSEL_0	46	0	ANEGSEL_1	ANEGSEL_0	
LED_2	ANEGSEL_1	45	0	0	0	Copper : Auto-negotiation (1000/100 Advertised), Auto MDIX
				1	1	Copper : Auto Negotiation (1000 Advertised), Auto MDIX

9.5.2 LED Configuration

The DP83869HM supports three configurable Light Emitting Diode (LED) pins: LED_0, LED_1, and LED_2. Several functions can be multiplexed onto the LEDs for different modes of operation. The LED operation mode can be selected using the LEDS_CFG1 register (address 0x0018).

Because the LED output pins are also used as straps, the external components required for strapping and LED usage must be considered to avoid contention. Specifically, when the LED outputs are used to drive LEDs directly, the active state of each output driver is dependent on the logic level sampled by the corresponding AN input upon power up or reset.

If a given strap input is resistively pulled low then the corresponding output is configured as an active high driver. Conversely, if a given strap input is resistively pulled high, then the corresponding output is configured as an active low driver.

Refer to 图 31 for an example of strap connections to external components. In this example, the strapping results in Mode 1 for LED_0 and Mode 2 for LED_1.

The adaptive nature of the LED outputs helps to simplify potential implementation issues of these dual purpose pins.

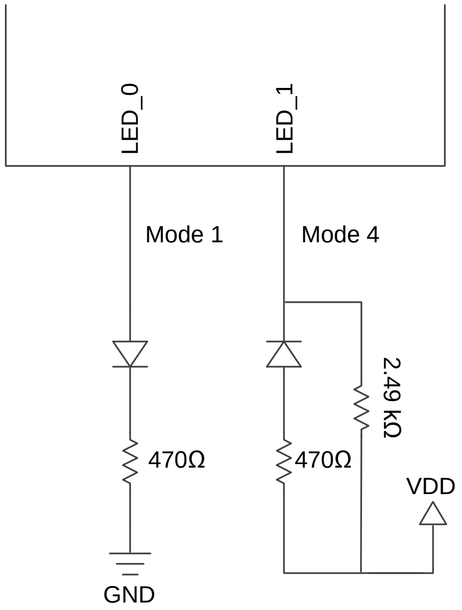


图 31. Example Strap Connections

The following conditions must be accounted when using LEDs:

- In RGMII-to-SGMII bridge mode with force speeds, Link LED function cannot be used.
- In both Bridge modes, LEDs can be configures to indicate TX only or RX only activity. LED will indicate activity with respect to RGMII when the PHY is in Bridge mode.
- In 1000-Mbps media convertor mode, the link LED corresponds to 1000M link on Copper interface. If link speed is changed then Link LED cannot be used.
- In 100-Mbps media convertor mode, the link LED corresponds to 100M link on Copper interface. If link speed is changed then Link LED cannot be used.

9.5.3 Reset Operation

The DP83869HM needs external control over RESET_N pin during power up. If RESET_N pin is connected to host controller, then the PHY should be held in reset for a minimum of 200ms after the last supply powers up as shown in 图 4. If host controller cannot be connected to RESET_N then a 100-Ω resistor and 47-µF capacitor are required to be connected in series between RESET_N pin and ground as shown in 图 32. During normal operation, the device can be reset by a hardware or software reset.

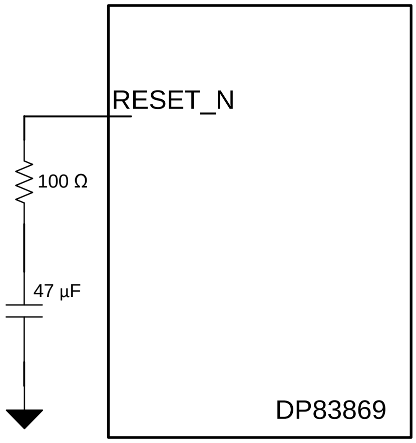


图 32. RESET_N Circuit

9.5.3.1 Hardware Reset

A hardware reset is accomplished by applying a low pulse, with a duration of at least 1 µs, to the RESET_N pin. This resets the device such that all registers are reinitialized to default values and the hardware configuration values are re-latched into the device (similar to the power up or reset operation).

9.5.3.2 IEEE Software Reset

An IEEE registers software reset is accomplished by setting the reset bit (bit 15) of the BMCR register (address 0x0000). This bit resets the IEEE-defined standard registers.

9.5.3.3 Global Software Reset

A global software reset is accomplished by setting bit 15 of register CTRL (address 0x001F) to 1. This bit resets all the internal circuits in the PHY including IEEE-defined registers and all the extended registers. The global software reset resets the device such that all registers are reset to default values and the hardware configuration values are maintained.

9.5.3.4 Global Software Restart

A global software restart is accomplished by setting bit 14 of register CTRL (0x001F) to 1. This action resets all the PHY circuits except the registers in the Register File.

9.6 Register Maps

For Fiber Operations (RGMII-to-1000Base-X and RGMII-to-100Base-FX), Fiber register location 0Cxxh get mapped to 0xxxxh address location to comply with IEEE Specifications.

Register Maps (continued)

9.6.1 DP83869 Registers

Table 19 lists the memory-mapped registers for the DP83869 registers. All register offset addresses not listed in Table 19 should be considered as reserved locations and the register contents should not be modified.

Table 19. DP83869 Registers

Address	Acronym	Register Name	Section
0x0	BMCR	Basic Mode Control Register	Go
0x1	BMSR	Basic Mode Status Register	Go
0x2	PHYIDR1	PHY Identifier Register #1	Go
0x3	PHYIDR2	PHY Identifier Register #2	Go
0x4	ANAR	Auto-Negotiation Advertisement Register	Go
0x5	ALNPAR	Auto-Negotiation Link Partner Ability Register	Go
0x6	ANER	Auto-Negotiate Expansion Register	Go
0x7	ANNPTR	Auto-Negotiation Next Page Transmit Register	Go
0x8	ANLNPTR	Auto-Negotiation Link Partner Next Page Receive Register	Go
0x9	GEN_CFG1	Configuration Register 1	Go
0xA	GEN_STATUS1	Status Register 1	Go
0xD	REGCR	Register Control Register	Go
0xE	ADDAR	Address or Data Register	Go
0xF	1KSCR	1000BASE-T Status Register	Go
0x10	PHY_CONTROL	PHY Control Register	Go
0x11	PHY_STATUS	PHY Status Register	Go
0x12	INTERRUPT_MASK	MII Interrupt Control Register	Go
0x13	INTERRUPT_STATUS	Interrupt Status Register	Go
0x14	GEN_CFG2	Configuration Register 2	Go
0x15	RX_ERR_CNT		Go
0x16	BIST_CONTROL	BIST Control Register	Go
0x17	GEN_STATUS2	Status Register 2	Go
0x18	LEDS_CFG1	LED Configuration Register 1	Go
0x19	LEDS_CFG2	LED Configuration Register 2	Go
0x1A	LEDS_CFG3	LED Configuration Register 3	Go
0x1E	GEN_CFG4	Configuration Register 3	Go
0x1F	GEN_CTRL	Control Register	Go
0x25	ANALOG_TEST_CTRL	Testmode Channel Control Register	Go
0x2C	GEN_CFG_ENH_AMIX		Go
0x2D	GEN_CFG_FLD		Go
0x2E	GEN_CFG_FLD_THR		Go
0x31	GEN_CFG3	Configuration Register 4	Go
0x32	RGMII_CTRL	RGMII Control Register	Go
0x33	RGMII_CTRL2		Go
0x37	SGMII_AUTO_NEG_STATUS	SGMII Autonegotiation Status Register	Go
0x39	PRBS_TX_CHK_CTRL		Go
0x3A	PRBS_TX_CHK_BYTE_CNT		Go
0x43	G_100BT_REG0		Go
0x4F	SERDES_SYNC_STS		Go
0x6E	STRAP_STS	Strap Status Register	Go
0x86	ANA_RGMII_DLL_CTRL	RGMII Delay Control Register	Go

Table 19. DP83869 Registers (continued)

Address	Acronym	Register Name	Section
0x134	RXF_CFG		Go
0x135	RXF_STATUS		Go
0x170	IO_MUX_CFG		Go
0x180	TDR_GEN_CFG1		Go
0x181	TDR_GEN_CFG2		Go
0x182	TDR_SEG_DURATION1		Go
0x183	TDR_SEG_DURATION2		Go
0x184	TDR_GEN_CFG3		Go
0x185	TDR_GEN_CFG4		Go
0x190	TDR_PEAKS_LOC_A_0_1		Go
0x191	TDR_PEAKS_LOC_A_2_3		Go
0x192	TDR_PEAKS_LOC_A_4_B_0		Go
0x193	TDR_PEAKS_LOC_B_1_2		Go
0x194	TDR_PEAKS_LOC_B_3_4		Go
0x195	TDR_PEAKS_LOC_C_0_1		Go
0x196	TDR_PEAKS_LOC_C_2_3		Go
0x197	TDR_PEAKS_LOC_C_4_D_0		Go
0x198	TDR_PEAKS_LOC_D_1_2		Go
0x199	TDR_PEAKS_LOC_D_3_4		Go
0x1A4	TDR_GEN_STATUS		Go
0x1A5	TDR_PEAKS_SIGN_A_B		Go
0x1A6	TDR_PEAKS_SIGN_C_D		Go
0x1DF	OP_MODE_DECODE		Go
0x1E0	GPIO_MUX_CTRL		Go
0xC00	FX_CTRL	Fiber Control Register	Go
0xC01	FX_STS	Fiber Status Register	Go
0xC02	FX_PHYID1	Fiber PHYID Register 1	Go
0xC03	FX_PHYID2	Fiber PHYID Register 2	Go
0xC04	FX_ANADV	Fiber Autonegotiation Advertisement Register	Go
0xC05	FX_LPABL	Fiber Link Partner Ability Register	Go
0xC06	FX_ANEXP	Fiber Autonegotiation Expansion Register	Go
0xC07	FX_LOCNP	Fiber LOC Next Page Register	Go
0xC08	FX_LPNP	Fiber Link Partner Next Page Register	Go
0xC18	FX_INT_EN	Fiber Interrupt Enable Register	Go
0xC19	FX_INT_STS	Fiber Interrupt Status Register	Go

Complex bit access types are encoded to fit into small table cells. Table 20 shows the codes that are used for access types in this section.

Table 20. DP83869 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
RC	C R	to Clear Read
RH	H R	Set or cleared by hardware Read
Write Type		

Table 20. DP83869 Access Type Codes (continued)

Access Type	Code	Description
W	W	Write
W1C	1C W	1 to clear Write
WoP	W	Write
WtoP	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

9.6.1.1 BMCR Register (Address = 0x0) [reset = 0x1140]

BMCR is shown in Figure 33 and described in Table 21.

Return to Summary Table.

IEEE defined register to control PHY functionality.

Figure 33. BMCR Register

15	14	13	12	11	10	9	8
RESET	MII_LOOPBACK	SPEED_SEL_LSB	AUTONEG_EN	PWD_DWN	ISOLATE	RSTRT_AUTONEG	DUPLEX_EN
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1	R-0x0	R/W-0x0	RH/WtoP-0x0	R/W-0x1
7	6	5	4	3	2	1	0
COL_TST	SPEED_SEL_MSB	RESERVED					
R/W-0x0	R-0x1	R-0x0					

Table 21. BMCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESET	R/W	0x0	This bit controls the MII reset function. This bit is self cleared after reset is completed. 0x0 = Normal Operation 0x1 = Reset.
14	MII_LOOPBACK	R/W	0x0	This bit controls the MII Loopback. When enabled, this will send data back to the MAC 0x0 = Disable 0x1 = Enable
13	SPEED_SEL_LSB	R/W	0x0	Speed selection bits LSB[13] and MSB[6] are used to control the data rate of the ethernet link when auto-negotiation is disabled. 0x0 = 10Mbps 0x1 = 100Mbps 0x2 = 1000Mbps 0x3 = Reserved
12	AUTONEG_EN	R/W	0x1	Controls autonegotiation feature 0x0 = Autonegotiation off 0x1 = Autonegotiation on
11	PWD_DWN	R	0x0	Controls IEEE power down feature 0x0 = Normal Mode 0x1 = IEEE power down mode

Table 21. BMCR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10	ISOLATE	R/W	0x0	Isolate MAC interface pins. 0x0 = Normal mode 0x1 = MAC Isolate mode enabled
9	RSTRT_AUTONEG	RH/WtoP	0x0	Restart auto-negotiation 0x0 = Normal mode 0x1 = Restart autonegotiation
8	DUPLEX_EN	R/W	0x1	Controls Half and Full duplex mode of the ethernet link 0x0 = Half Duplex mode 0x1 = Full Duplex mode
7	COL_TST	R/W	0x0	Controls Collision Signal Test 0x0 = Disable Collision Signal Test 0x1 = Enable Collision Signal Test
6	SPEED_SEL_MSB	R	0x1	Controls data rate of ethernet link when autonegotiation is disabled. See bit 13 description for morw information.
5-0	RESERVED	R	0x0	Reserved

9.6.1.2 *BMSR Register (Address = 0x1) [reset = 0x7949]*

BMSR is shown in Figure 34 and described in Table 22.

Return to Summary Table.

IEEE defined register to show status of PHY

Figure 34. BMSR Register

15	14	13	12	11	10	9	8
RESERVED	100M_FDUP	100M_HDUP	10M_FDUP	10M_HDUP	RESERVED	RESERVED	EXT_STS
R-0x0	R-0x1	R-0x1	R-0x1	R-0x1	R-0x0	R-0x0	R-0x1

7	6	5	4	3	2	1	0
RESERVED	MF_PREAMBLE_SUP	AUTONEG_COMP	REMOTE_FAULT	AUTONEG_ABL	LINK_STS1	JABBER_DTCT	EXT_CAPBLTY
R-0x0	R-0x1	R-0x0	RC-0x0	R-0x1	R-0x0	RC-0x0	R-0x1

Table 22. BMSR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	100M_FDUP	R	0x1	100Base-TX full duplex 0x0 = PHY not able to perform full duplex 100Base-X 0x1 = PHY able to perform full duplex 100Base-X
13	100M_HDUP	R	0x1	100Base-TX halfduplex 0x0 = PHY not able to perform half duplex 100Base-X 0x1 = PHY able to perform half duplex 100Base-X
12	10M_FDUP	R	0x1	10Base-Te full duplex 0x0 = PHY not able to operate at 10Mbps in full duplex 0x1 = PHY able to operate at 10Mbps in full duplex

Table 22. BMSR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	10M_HDUP	R	0x1	10Base-Te half duplex 0x0 = PHY not able to operate at 10Mbps in half duplex 0x1 = PHY able to operate at 10Mbps in half duplex
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	EXT_STS	R	0x1	Extended status for 1000Base T abilities in register 15 0x1 = Extended status information in register 0x0F
7	RESERVED	R	0x0	Reserved
6	MF_PREAMBLE_SUP	R	0x1	Ability to accept management frames with preamble suppressed. 0x0 = PHY will not accept management frames with preamble suppressed 0x1 = PHY will accept management frames with preamble suppressed
5	AUTONEG_COMP	R	0x0	Status of Autonegotiation 0x0 = Auto Negotiation process not completed 0x1 = Auto Negotiation process completed
4	REMOTE_FAULT	RC	0x0	Remote fault detection 0x0 = No remote fault condition detected 0x1 = Remote fault condition detected
3	AUTONEG_ABL	R	0x1	Autonegotiation ability 0x0 = PHY is not able to perform Auto-Negotiation 0x1 = PHY is able to perform Auto-Negotiation
2	LINK_STS1	R	0x0	Link Status This is latch low and needs to be read twice for valid link up 0x0 = Link down 0x1 = Link up
1	JABBER_DTCT	RC	0x0	Jabber detected 0x0 = No jabber detected 0x1 = Jabber detected
0	EXT_CAPBLTY	R	0x1	Extended register capabilities 0x0 = Basic register set capabilities 0x1 = Extended register set capabilities

9.6.1.3 PHYIDR1 Register (Address = 0x2) [reset = 0x2000]

PHYIDR1 is shown in Figure 35 and described in Table 23.

Return to Summary Table.

The PHY Identifier Registers #1 and #2 together form a unique identifier for the DP83869. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if esired. The PHY Identifier is intended to support network management. Texas Instruments' IEEE assigned OUI is 080028h.

Figure 35. PHYIDR1 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUI_MSB															
R-0x2000															

Table 23. PHYIDR1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	OUI_MSB	R	0x2000	OUI Most Significant Bits: Bits 3 to 18 of the OUI (080028h,) are stored in bits 15 to 0 of this register respectively. Bit numbering for OUI goes from 1 (MSB) to 24(LSB). The most significant two bits of the OUI are ignored (the IEEE standard refers to these as bits 1 and 2).

9.6.1.4 PHYIDR2 Register (Address = 0x3) [reset = 0xA0F1]

PHYIDR2 is shown in Figure 36 and described in Table 24.

Return to Summary Table.

Figure 36. PHYIDR2 Register

15	14	13	12	11	10	9	8
OUI_LSB						MODEL_NUM	
R-0x28						R-0xF	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MODEL_NUM				REVISION_NUM			
R-0xF				R-0x1			

Table 24. PHYIDR2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	OUI_LSB	R	0x28	OUI Least Significant Bits: Bits 19 to 24 of the OUI (080028h) are mapped from bits 15 to 10 of this register respectively.
9-4	MODEL_NUM	R	0xF	Model number: The six bits of vendor model number are mapped from bits 9 to 4 (most significant bit to bit 9).
3-0	REVISION_NUM	R	0x1	Revision number: Four bits of the vendor model revision number are mapped from bits 3 to 0 (most significant bit to bit 3). This field will be incremented for all major device changes.

9.6.1.5 ANAR Register (Address = 0x4) [reset = 0x1]

ANAR is shown in Figure 37 and described in Table 25.

Return to Summary Table.

This register contains the advertised abilities of this device as they will be transmitted to its link partner during Auto-Negotiation. Any writes to this register prior to completion of Auto-Negotiation (as indicated in the Basic Mode Status Register (address 01h) Auto-Negotiation Complete bit, BMSR[5]) should be followed by a renegotiation. This will ensure that the new values are properly used in the Auto-Negotiation.

Figure 37. ANAR Register

15	14	13	12	11	10	9	8
NEXT_PAGE_1_ADV	RESERVED	REMOTE_FAULT_ADV	ANAR_BIT12	ASYMMETRIC_PAUSE_ADV	PAUSE_ADV	G_100BT_4_ADV	G_100BTX_FD_ADV
R/W-0x0	R-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G_100BTX_HD_ADV	G_10BT_FD_ADV	G_10BT_HD_ADV	SELECTOR_FIELD_ADV				
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1				

Table 25. ANAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NEXT_PAGE_1_ADV	R/W	0x0	Next Page Advertisement 0x0 = Do not advertise desire to send additional SW next pages 0x1 = Advertise desire to send additional SW next pages
14	RESERVED	R	0x0	Reserved
13	REMOTE_FAULT_ADV	R/W	0x0	Remote Fault Advertisement 0x0 = Do not advertise remote fault event detection 0x1 = Advertise remote fault event detection
12	ANAR_BIT12	R/W	0x0	
11	ASYMMETRIC_PAUSE_ADV	R/W	0x0	1b = Advertise asymmetric pause ability 0b = Do not advertise asymmetric pause ability
10	PAUSE_ADV	R/W	0x0	0x0 = Do not advertise pause ability 0x1 = Advertise pause ability
9	G_100BT_4_ADV	R/W	0x0	100BT-4 is not supported
8	G_100BTX_FD_ADV	R/W	0x0	100Base-TX Full Duplex. Default depends on strap, non strap default '1'. 0x0 = Do not advertise 100Base-TX Full Duplex ability 0x1 = Advertise 100Base-TX Full Duplex ability
7	G_100BTX_HD_ADV	R/W	0x0	100Base-TX Half Duplex. Default depends on strap, non strap default '1'. 0x0 = Do not advertise 100Base-TX Half Duplex ability 0x1 = Advertise 100Base-TX Half Duplex ability
6	G_10BT_FD_ADV	R/W	0x0	Default depends on strap, non strap default '1' 0x0 = Do not advertise 10Base-T Full Duplex ability 0x1 = Advertise 10Base-T Full Duplex ability
5	G_10BT_HD_ADV	R/W	0x0	Default depends on strap, non strap default '1' 0x0 = Do not advertise 10Base-T Half Duplex ability 0x1 = Advertise 10Base-T Half Duplex ability
4-0	SELECTOR_FIELD_ADV	R/W	0x1	Technology selector field (802.3 == 00001)

9.6.1.6 ALNPAR Register (Address = 0x5) [reset = 0x0]

ALNPAR is shown in Figure 38 and described in Table 26.

Return to Summary Table.

This register contains the advertised abilities of the Link Partner as received during Auto-Negotiation. The content changes after the successful Auto-Negotiation if Next pages are supported.

Figure 38. ALNPAR Register

15	14	13	12	11	10	9	8
NEXT_PAGE_1_LP	ACKNOWLEDGE_1_LP	REMOTE_FAULT_LP	RESERVED	ASYMMETRIC_PAUSE_LP	PAUSE_LP	G_100BT4_LP	G_100BTX_FD_LP
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
G_100BTX_HD_LP	G_10BT_FD_LP	G_10BT_HD_LP	SELECTOR_FIELD_LP				
R-0x0	R-0x0	R-0x0	R-0x0				

Table 26. ALNPAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NEXT_PAGE_1_LP	R	0x0	0x0 = Link Partner does not advertise desire to send additional SW next pages 0x1 = Link Partner advertises desire to send additional SW next pages
14	ACKNOWLEDGE_1_LP	R	0x0	0x0 = Link Partner does not acknowledge reception of link partner's link code word 0x1 = Link Partner acknowledges reception of link partner's link code word
13	REMOTE_FAULT_LP	R	0x0	0x0 = Link Partner does not advertise remote fault event detection 0x1 = Link Partner advertises remote fault event detection
12	RESERVED	R	0x0	Reserved
11	ASYMMETRIC_PAUSE_LP	R	0x0	0x0 = Link Partner does not advertise asymmetric pause ability 0x1 = Link Partner advertises asymmetric pause ability
10	PAUSE_LP	R	0x0	0x0 = Link Partner does not advertise pause ability 0x1 = Link Partner advertises pause ability
9	G_100BT4_LP	R	0x0	0x0 = Link Partner does not advertise 100Base-T4 ability 0x1 = Link Partner advertises 100Base-T4 ability
8	G_100BTX_FD_LP	R	0x0	0x0 = Link Partner does not advertise 100Base-TX Full Duplex ability 0x1 = Link Partner advertises 100Base-TX Full Duplex ability
7	G_100BTX_HD_LP	R	0x0	0x0 = Link Partner does not advertise 100Base-TX Half Duplex ability 0x1 = Link Partner advertises 100Base-TX Half Duplex ability
6	G_10BT_FD_LP	R	0x0	0x0 = Link Partner does not advertise 10Base-T Full Duplex ability 0x1 = Link Partner advertises 10Base-T Full Duplex ability
5	G_10BT_HD_LP	R	0x0	0x0 = Link Partner does not advertise 10Base-T Half Duplex ability 0x1 = Link Partner advertises 10Base-T Half Duplex ability
4-0	SELECTOR_FIELD_LP	R	0x0	Technology selector field

9.6.1.7 ANER Register (Address = 0x6) [reset = 0x64]

ANER is shown in Figure 39 and described in Table 27.

Return to Summary Table.

This register contains additional Local Device and Link Partner status information.

Figure 39. ANER Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0

RESERVED	RX_NEXT_PAGE_LOC_ABLE	RX_NEXT_PAGE_STOR_LOC	PRLL_TDCT_FAULE	LP_NP_ABLE	LOCAL_NP_ABLE	PAGE_RECEIVED_1	LP_AUTONEG_ABLE
R-0x0	R-0x1	R-0x1	RC-0x0	R-0x0	R-0x1	RC-0x0	R-0x0

Table 27. ANER Register Field Descriptions

Bit	Field	Type	Reset	Description
15-7	RESERVED	R	0x0	Reserved
6	RX_NEXT_PAGE_LOC_ABLE	R	0x1	0x0 = Received Next Page storage location is not specified by bit 6.5 0x1 = Received Next Page storage location is specified by bit 6.5
5	RX_NEXT_PAGE_STOR_LOC	R	0x1	0x0 = Link Partner Next Pages are stored in register 5 0x1 = Link Partner Next Pages are stored in register 8
4	PRLL_TDCT_FAULE	RC	0x0	THIS STATUS IS LH (Latched-High) 0x0 = A fault has not been detected during the parallel detection process 0x1 = A fault has been detected during the parallel detection process
3	LP_NP_ABLE	R	0x0	0x0 = Link partner is not able to exchange next pages 0x1 = Link partner is able to exchange next pages
2	LOCAL_NP_ABLE	R	0x1	0x0 = Local device is not able to exchange next pages 0x1 = Local device is able to exchange next pages
1	PAGE_RECEIVED_1	RC	0x0	THIS STATUS IS LH (Latched-High) 0x0 = A new page has not been received 0x1 = A new page has been received
0	LP_AUTONEG_ABLE	R	0x0	0x0 = Link partner is not Auto-Negotiation able 0x1 = Link partner is Auto-Negotiation able

9.6.1.8 ANNPTR Register (Address = 0x7) [reset = 0x2001]

ANNPTR is shown in Figure 40 and described in Table 28.

Return to Summary Table.

This register contains the next page information sent by this device to its Link Partner during Auto-Negotiation.

Figure 40. ANNPTR Register

15	14	13	12	11	10	9	8
NEXT_PAGE_2_ADV	RESERVED	MESSAGE_PAGE	ACKNOWLEDGE2	TOGGLE	MESSAGE_UNFORMATTED		
R/W-0x0	R-0x0	R/W-0x1	R/W-0x0	R-0x0	R/W-0x1		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MESSAGE_UNFORMATTED							
R/W-0x1							

Table 28. ANNPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NEXT_PAGE_2_ADV	R/W	0x0	0x0 = Do not advertise desire to send additional next pages 0x1 = Advertise desire to send additional next pages

Table 28. ANNPTR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	RESERVED	R	0x0	Reserved
13	MESSAGE_PAGE	R/W	0x1	0x0 = Current page is an unformatted page 0x1 = Current page is a message page
12	ACKNOWLEDGE2	R/W	0x0	0x0 = Do not set the ACK2 bit 0x1 = Set the ACK2 bit
11	TOGGLE	R	0x0	Toggles every page. Initial value is !4.11
10-0	MESSAGE_UNFORMATTED	R/W	0x1	Contents of the message/unformatted page

9.6.1.9 ANLNPTR Register (Address = 0x8) [reset = 0x2001]

ANLNPTR is shown in Figure 41 and described in Table 29.

Return to Summary Table.

This register contains the next page information sent by the Link Partner during Auto-Negotiation.

Figure 41. ANLNPTR Register

15	14	13	12	11	10	9	8
NEXT_PAGE_2_LP	ACKNOWLEDGE_2_LP	MESSAGE_PAGE_LP	ACKNOWLEDGE2_LP	TOGGLE_LP	MESSAGE_UNFORMATTED_LP		
R-0x0	R-0x0	R-0x1	R-0x0	R-0x0	R-0x1		

7	6	5	4	3	2	1	0
MESSAGE_UNFORMATTED_LP							
R-0x1							

Table 29. ANLNPTR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NEXT_PAGE_2_LP	R	0x0	0x0 = Link partner does not advertise desire to send additional next pages 0x1 = Link partner advertises desire to send additional next pages
14	ACKNOWLEDGE_2_LP	R	0x0	0x0 = Link partner does not acknowledge reception of link code work 0x1 = Link partner acknowledges reception of link code word
13	MESSAGE_PAGE_LP	R	0x1	0x0 = Received page is an unformatted page 0x1 = Received page is a message page
12	ACKNOWLEDGE2_LP	R	0x0	0x0 = Link partner does not set the ACK2 bit 0x1 = Link partner sets the ACK2 bit
11	TOGGLE_LP	R	0x0	Toggles every page. Initial value is !5.11
10-0	MESSAGE_UNFORMATTED_LP	R	0x1	Contents of the message/unformatted page

9.6.1.10 GEN_CFG1 Register (Address = 0x9) [reset = 0x300]

GEN_CFG1 is shown in Figure 42 and described in Table 30.

Return to Summary Table.

Figure 42. GEN_CFG1 Register

15	14	13	12	11	10	9	8
TEST_MODE			MASTER_SLAVE_MAN_CFG_EN	MASTER_SLAVE_MAN_CFG_VAL	PORT_TYPE	G_1000BT_FD_ADV	G_1000BT_HD_ADV
R/W-0x0			R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1	R/W-0x1

7	6	5	4	3	2	1	0
TDR_AUTO_RUN	RESERVED						
R/W-0x0	R-0x0						

Table 30. GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	TEST_MODE	R/W	0x0	0x0 = Normal Mode 0x1 = Test Mode 1 - Transmit Waveform Test 0x2 = Test Mode 2 - Transmit Jitter Test (Master Mode) 0x3 = Test Mode 3 - Transmit Jitter Test (Slave Mode) 0x4 = Test Mode 4 - Transmit Distortion Test 0x5 = Test Mode 5 - Scrambled MLT3 Idles 0x6 = Test Mode 6 - Repetitive 0001 sequence 0x7 = Test Mode 7 - Repetitive {Pulse, 63 zeros}
12	MASTER_SLAVE_MAN_CFG_EN	R/W	0x0	1 = Enable manual Master/Slave configuration 0 = Do not enable manual Master/Slave configuration
11	MASTER_SLAVE_MAN_CFG_VAL	R/W	0x0	1 = Manual configure as Master 0 = Manual configure as Slave
10	PORT_TYPE	R/W	0x0	1 = Multi-port device 0 = Single-port device
9	G_1000BT_FD_ADV	R/W	0x1	Default depends on strap 0x0 = Do not advertise 1000Base-T Full Duplex ability 0x1 = Advertise 1000Base-T Full Duplex ability
8	G_1000BT_HD_ADV	R/W	0x1	Default depends on strap 0x0 = Do not advertise 1000Base-T Half Duplex ability 0x1 = Advertise 1000Base-T Half Duplex ability
7	TDR_AUTO_RUN	R/W	0x0	TDR Auto Run at link down: 0x0 = Disable automatic execution of TDR 0x1 = Enable execution of TDR procedure after link down event
6-0	RESERVED	R	0x0	Reserved

9.6.1.11 GEN_STATUS1 Register (Address = 0xA) [reset = 0x0]

GEN_STATUS1 is shown in Figure 43 and described in Table 31.

Return to Summary Table.

Figure 43. GEN_STATUS1 Register

15	14	13	12	11	10	9	8
MS_CONFIG_FAULT	MS_CONFIG_RES	LOC_RCVR_STATUS_1	REM_RCVR_STATUS	LP_1000BT_FD_ABILITY	LP_1000BT_HD_ABILITY	RESERVED	
RC-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	

7	6	5	4	3	2	1	0
IDLE_ERR_COUNT							
R-0x0							

Table 31. GEN_STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	MS_CONFIG_FAULT	RC	0x0	1 = Master/Slave configuration fault detected 0 = No Master/Slave configuration fault detected THIS STATUS IS LH (Latched-High)
14	MS_CONFIG_RES	R	0x0	1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
13	LOC_RCVR_STATUS_1	R	0x0	1 = Local receiver is OK 0 = Local receiver is not OK
12	REM_RCVR_STATUS	R	0x0	1 = Remote receiver is OK 0 = Remote receiver is not OK
11	LP_1000BT_FD_ABILITY	R	0x0	1 = Link partner supports 1000Base-T Full Duplex ability 0 = Link partner does not support 1000Base-T Full Duplex ability
10	LP_1000BT_HD_ABILITY	R	0x0	1 = Link partner supports 1000Base-T Half Duplex ability 0 = Link partner does not support 1000Base-T Half Duplex ability
9-8	RESERVED	R	0x0	Reserved
7-0	IDLE_ERR_COUNT	R	0x0	1000Base-T Idle Error Counter

9.6.1.12 REGCR Register (Address = 0xD) [reset = 0x0]

REGCR is shown in Figure 44 and described in Table 32.

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This register is the MDIO Manageable MMD access control. In general, register REGCR (4:0) is the device address DEVAD that directs any accesses of the ADDAR (0x000E) register to the appropriate MMD. REGCR also contains selection bits for auto increment of the data register. This register contains the device address to be written to access the extended registers. Write 0x1F into bits 4:0 of this register. REGCR also contains selection bits (15:14) for the address auto-increment mode of ADDAR.

Figure 44. REGCR Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">G_FUNCTION</td><td colspan="6">RESERVED</td></tr>
<tr><td colspan="2">R/W-0x0</td><td colspan="6">R-0x0</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">RESERVED</td><td colspan="5">DEVAD</td></tr>
<tr><td colspan="3">R-0x0</td><td colspan="5">R/W-0x0</td></tr>
</table>

Table 32. REGCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	G_FUNCTION	R/W	0x0	00 = Address 01 = Data, no post increment 10 = Data, post increment on read and write 11 = Data, post increment on write only
13-5	RESERVED	R	0x0	Reserved
4-0	DEVAD	R/W	0x0	Device Address

9.6.1.13 ADDAR Register (Address = 0xE) [reset = 0x0]

ADDAR is shown in Figure 45 and described in Table 33.

Return to Summary Table.

This register is the address/data MMD register. ADDAR is used in conjunction with REGCR register (0x000D) to provide the access by indirect read/write mechanism to the extended register set.

Figure 45. ADDAR Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADDR_DATA															
R/W-0x0															

Table 33. ADDAR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADDR_DATA	R/W	0x0	If register 13.15:14 = 00, holds the MMD DEVAD's address register, otherwise holds the MMD DEVAD's data register

9.6.1.14 1KSCR Register (Address = 0xF) [reset = 0xF000]

1KSCR is shown in Figure 46 and described in Table 34.

Return to Summary Table.

Figure 46. 1KSCR Register

15	14	13	12	11	10	9	8
G_1000BX_FD	G_1000BX_HD	G_1000BT_FD	G_1000BT_HD	RESERVED			
R-0x1	R-0x1	R-0x1	R-0x1	R-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED							
R-0x0							

Table 34. 1KSCR Register Field Descriptions

Bit	Field	Type	Reset	Description
15	G_1000BX_FD	R	0x1	1 = PHY supports 1000Base-X Full Duplex capability 0 = PHY does not support 1000Base-X Full Duplex capability
14	G_1000BX_HD	R	0x1	1 = PHY supports 1000Base-X Half Duplex capability 0 = PHY does not support 1000Base-X Half Duplex capability
13	G_1000BT_FD	R	0x1	1 = PHY supports 1000Base-T Full Duplex capability 0 = PHY does not support 1000Base-T Full Duplex capability
12	G_1000BT_HD	R	0x1	1 = PHY supports 1000Base-T Half Duplex capability 0 = PHY does not support 1000Base-T Half Duplex capability
11-0	RESERVED	R	0x0	Reserved

9.6.1.15 PHY_CONTROL Register (Address = 0x10) [reset = 0x5048]

PHY_CONTROL is shown in Figure 47 and described in Table 35.

Return to Summary Table.

Figure 47. PHY_CONTROL Register

15	14	13	12	11	10	9	8
TX_FIFO_DEPTH		RX_FIFO_DEPTH		RESERVED	FORCE_LINK_GOOD	POWER_SAVE_MODE	
R/W-0x1		R/W-0x1		R/W-0x0	R/W-0x0	R/W-0x0	
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	MDI_CROSSOVER_MODE		DISABLE_CLK_125	RESERVED	RESERVED	LINE_DRIVER_INV_EN	DISABLE_JABBER
R/W-0x0	R/W-0x2		R/W-0x0	R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x0

Table 35. PHY_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	TX_FIFO_DEPTH	R/W	0x1	FIFO is enabled only in the following modes: 1000BaseT + GMII, 10BaseT/100BaseTX/1000BaseT + SGMII 0x0 = 3 bytes/nibbles (1000Mbps/Other Speeds) 0x1 = 4 bytes/nibbles (1000Mbps/Other Speeds) 0x2 = 6 bytes/nibbles (1000Mbps/Other Speeds) 0x3 = 8 bytes/nibbles (1000Mbps/Other Speeds)
13-12	RX_FIFO_DEPTH	R/W	0x1	FIFO is enabled only when SGMII is used 0x0 = 3 bytes/nibbles (1000Mbps/Other Speeds) 0x1 = 4 bytes/nibbles (1000Mbps/Other Speeds) 0x2 = 6 bytes/nibbles (1000Mbps/Other Speeds) 0x3 = 8 bytes/nibbles (1000Mbps/Other Speeds)
11	RESERVED	R/W	0x0	Reserved
10	FORCE_LINK_GOOD	R/W	0x0	0x0 = Do Normal operation 0x1 = Force Link OK if speed is 1G
9-8	POWER_SAVE_MODE	R/W	0x0	0x0 = Normal mode 0x1 = Reserved 0x2 = Active Sleep mode 0x3 = Passive Sleep mode
7	RESERVED	R/W	0x0	Reserved
6-5	MDI_CROSSOVER_MODE	R/W	0x2	Default depends on strap 0x0 = Manual MDI configuration 0x1 = Manual MDI-X configuration 0xA = Enable automatic crossover 0xB = Enable automatic crossover
4	DISABLE_CLK_125	R/W	0x0	0x0 = Enable CLK125 0x1 = Disable CLK125
3	RESERVED	R/W	0x1	Reserved
2	RESERVED	R/W	0x0	Reserved
1	LINE_DRIVER_INV_EN	R/W	0x0	This bit is not applicable in Mirror mode 0x0 = Do not Invert LD transmission 0x1 = Invert LD transmission
0	DISABLE_JABBER	R/W	0x0	0x0 = Enable Jabber function 0x1 = Disable Jabber function

9.6.1.16 *PHY_STATUS Register (Address = 0x11) [reset = 0x0]*

PHY_STATUS is shown in Figure 48 and described in Table 36.

Return to Summary Table.

Figure 48. PHY_STATUS Register

15	14	13	12	11	10	9	8
SPEED_SEL		DUPLEX_MODE_ENV	PAGE_RECEIVED_2	SPEED_DUPLEX_RESOLVED	LINK_STATUS_2	MDI_X_MODE_CD_1	MDI_X_MODE_AB_1
R-0x0		R-0x0	RC-0x0	R-0x0	R-0x0	R-0x0	R-0x0

7	6	5	4	3	2	1	0
SPEED_OPT_STATUS	SLEEP_MODE	WIRE_CROSS				DATA_POLARITY	JABBER_DTCT_2
R-0x0	R-0x0	R-0x0				R-0x0	R-0x0

Table 36. PHY_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	SPEED_SEL	R	0x0	00 = 10Mbps 01 = 100Mbps 10 = 1000Mbps 11 = Reserved
13	DUPLEX_MODE_ENV	R	0x0	1 = Full duplex 0 = Half duplex
12	PAGE_RECEIVED_2	RC	0x0	1 = Page received 0 = Page not received THIS BIT IS LH (Latched-High)
11	SPEED_DUPLEX_RESOLVED	R	0x0	1 = Auto-Negotiation completed or disabled 0 = Auto-Negotiation enabled and not completed
10	LINK_STATUS_2	R	0x0	1 = Link is up 0 = Link is down
9	MDI_X_MODE_CD_1	R	0x0	1 = MDI-X 0 = MDI
8	MDI_X_MODE_AB_1	R	0x0	1 = MDI-X 0 = MDI
7	SPEED_OPT_STATUS	R	0x0	1 = Auto-Negotiation is currently being performed with Speed Optimization masking 1000BaseT abilities (Valid only during Auto-Negotiation) 0 = Auto-Negotiation is currently being performed without Speed Optimization
6	SLEEP_MODE	R	0x0	1 = Sleep 0 = Active
5-2	WIRE_CROSS	R	0x0	Indicates channels [D,C,B,A] polarity in 1000BT link 1 = Channel polarity is reversed 0 = Channel polarity is normal
1	DATA_POLARITY	R	0x0	1 = 10BT is in normal polarity 0 = 10BT is in reversed polarity
0	JABBER_DTCT_2	R	0x0	1 = Jabber 0 = No Jabber

9.6.1.17 INTERRUPT_MASK Register (Address = 0x12) [reset = 0x0]

INTERRUPT_MASK is shown in Figure 49 and described in Table 37.

Return to Summary Table.

This register implements the Interrupt PHY Specific Control register. The individual interrupt events must be enabled by setting bits in the MII Interrupt Control Register (MICR). If the corresponding enable bit in the register is set, an interrupt is generated if the event occurs.

Figure 49. INTERRUPT_MASK Register

15	14	13	12	11	10	9	8
AUTONEG_ERR_INT_EN	SPEED_CHNG_INT_EN	DUPLEX_MODE_CHNG_INT_EN	PAGE_RECEIVED_INT_EN	AUTONEG_COMP_INT_EN	LINK_STATUS_CHNG_INT_EN	EEE_ERR_INT_EN	FALSE_CARRIER_INT_EN
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ADC_FIFO_OVF_UNF_INT_EN	MDI_CROSSOVER_CHNG_INT_EN	SPEED_OPT_EVENT_INT_EN	SLEEP_MODE_CHNG_INT_EN	WOL_INT_EN	XGMII_ERR_INT_EN	POLARITY_CHNG_INT_EN	JABBER_INT_EN
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 37. INTERRUPT_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15	AUTONEG_ERR_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
14	SPEED_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt

Table 37. INTERRUPT_MASK Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	DUPLEX_MODE_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
12	PAGE_RECEIVED_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
11	AUTONEG_COMP_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
10	LINK_STATUS_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
9	EEE_ERR_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
8	FALSE_CARRIER_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
7	ADC_FIFO_OVF_UNF_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
6	MDI_CROSSOVER_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
5	SPEED_OPT_EVENT_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
4	SLEEP_MODE_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
3	WOL_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
2	XGMII_ERR_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
1	POLARITY_CHNG_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt
0	JABBER_INT_EN	R/W	0x0	1 = Enable interrupt 0 = Disable interrupt

9.6.1.18 INTERRUPT_STATUS Register (Address = 0x13) [reset = 0x0]

INTERRUPT_STATUS is shown in Figure 50 and described in Table 38.

Return to Summary Table.

This register contains event status for the interrupt function. If an event has occurred since the last read of this register, the corresponding status bit will be set. The status indications in this register will be set even if the interrupt is not enabled.

Figure 50. INTERRUPT_STATUS Register

15	14	13	12	11	10	9	8
AUTONEG_ERR	SPEED_CHNG	DUPLEX_MODE_CHNG	PAGE_RECEIVED	AUTONEG_COMP	LINK_STATUS_CHNG	EEE_ERR_STATUS	FALSE_CARRIER
RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	R-0x0	RC-0x0
7	6	5	4	3	2	1	0
ADC_FIFO_OVF_UNF	MDI_CROSSOVER_CHNG	SPEED_OPT_EVENT	SLEEP_MODE_CHNG	WOL_STATUS	XGMII_ERR_STATUS	POLARITY_CHNG	JABBER
RC-0x0	RC-0x0	RC-0x0	RC-0x0	R-0x0	R-0x0	R-0x0	RC-0x0

Table 38. INTERRUPT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	AUTONEG_ERR	RC	0x0	1 = Auto-Negotiation error has occurred 0 = Auto-Negotiation error has not occurred THIS BIT IS LH (Latched-High)
14	SPEED_CHNG	RC	0x0	1 = Link speed has changed 0 = Link speed has not changed THIS BIT IS LH (Latched-High)
13	DUPLEX_MODE_CHNG	RC	0x0	1 = Duplex mode has changed 0 = Duplex mode has not changed THIS BIT IS LH (Latched-High)

Table 38. INTERRUPT_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12	PAGE_RECEIVED	RC	0x0	1 = Page has been received 0 = Page has not been received THIS BIT IS LH (Latched-High)
11	AUTONEG_COMP	RC	0x0	1 = Auto-Negotiation has completed 0 = Auto-Negotiation has not completed THIS BIT IS LH (Latched-High)
10	LINK_STATUS_CHNG	RC	0x0	1 = Link status has changed 0 = Link status has not changed THIS BIT IS LH (Latched-High)
9	EEE_ERR_STATUS	R	0x0	1 = EEE error has been detected
8	FALSE_CARRIER	RC	0x0	1 = Enable interrupt 0 = Disable interrupt THIS BIT IS LH (Latched-High)
7	ADC_FIFO_OVF_UNF	RC	0x0	1 = Overflow / underflow has been detected in one of ADC's FIFOs THIS BIT IS LH (Latched-High)
6	MDI_CROSSOVER_CHNG	RC	0x0	1 = MDI crossover has changed 0 = MDI crossover has not changed THIS BIT IS LH (Latched-High)
5	SPEED_OPT_EVENT	RC	0x0	1 = MDI crossover has changed 0 = MDI crossover has not changed THIS BIT IS LH (Latched-High)
4	SLEEP_MODE_CHNG	RC	0x0	1 = Sleep mode has changed 0 = Sleep mode has not changed THIS BIT IS LH (Latched-High)
3	WOL_STATUS	R	0x0	1 = WoL (or pattern) packet has been received
2	XGMII_ERR_STATUS	R	0x0	1 = Overflow / underflow has been detected in one of GMII / RGMII / SGMII buffers NOTE: this indication have issue, recommend to not put on DS, unless proven otherwise on the lab, CDDS #475
1	POLARITY_CHNG	R	0x0	1 = Data polarity has changed 0 = Data polarity has not changed THIS BIT IS LH (Latchde-High)
0	JABBER	RC	0x0	1 = Jabber detected 0 = Jabber not detected THIS BIT IS LH (Latched-High)

9.6.1.19 GEN_CFG2 Register (Address = 0x14) [reset = 0x29C7]

GEN_CFG2 is shown in Figure 51 and described in Table 39.

Return to Summary Table.

Figure 51. GEN_CFG2 Register

15	14	13	12	11	10	9	8
PD_DETECT_EN	SGMII_TX_ERR_DIS	INTERRUPT_POLARITY	SGMII_SOFT_RESET	SPEED_OPT_ATTEMPT_CNT		SPEED_OPT_EN	SPEED_OPT_ENHANCED_EN
RH/WtoP-0x0	R/W-0x0	R/W-0x1	RH/WtoP-0x0	R/W-0x2		R/W-0x0	R/W-0x1

7	6	5	4	3	2	1	0
SGMII_AUTONEG_EN	SPEED_OPT_10M_EN	MII_CLK_CFG		COL_FD_EN	LEGACY_CODING_TXMODE_EN	MASTER_SEMI_CROSS_EN	SLAVE_SEMI_CROSS_EN
R/W-0x1	R/W-0x1	R/W-0x0		R/W-0x0	R/W-0x1	R/W-0x1	R/W-0x1

Table 39. GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PD_DETECT_EN	RH/WtoP	0x0	0x0 = Disable PD detection 0x1 = Enable PD (Powered Device) detection
14	SGMII_TX_ERR_DIS	R/W	0x0	0x0 = Enable SGMII TX Error indication 0x1 = Disable SGMII TX Error indication

Table 39. GEN_CFG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13	INTERRUPT_POLARITY	R/W	0x1	0x0 = Interrupt pin is active high 0x1 = Interrupt pin is active low
12	SGMII_SOFT_RESET	RH/WtoP	0x0	Setting this bit will generate a soft reset pulse of SGMII. This register is WSC (write-self-clear).
11-10	SPEED_OPT_ATTEMPT_CNT	R/W	0x2	Selects the number of 1G link establishment attempt failures prior to performing Speed Optimization: 0x0 = 1 attempt 0x1 = 2 attempts 0x2 = 4 attempts 0x3 = 8 attempts
9	SPEED_OPT_EN	R/W	0x0	0x0 = Disable Speed Optimization 0x1 = Enable Speed Optimization
8	SPEED_OPT_ENHANCED_EN	R/W	0x1	In enhanced mode, speed is optimized if energy is not detected in channels C and D 0x0 = Disable Speed Optimization enhanced mode 0x1 = Enable Speed Optimization enhanced mode
7	SGMII_AUTONEG_EN	R/W	0x1	0x0 = Disable SGMII Auto-Negotiation 0x1 = Enable SGMII Auto-Negotaition
6	SPEED_OPT_10M_EN	R/W	0x1	0x0 = Disable speed optimization to 10M 0x1 = Enable speed optimization to 10M (If link establishments of 1G and 100M fail)
5-4	MII_CLK_CFG	R/W	0x0	Selects frequency of GMII_TX_CLK in 1G mode: 0x0 = 2.5Mhz 0x1 = 25Mhz 0x2 = Disabled 0x3 = Disabled
3	COL_FD_EN	R/W	0x0	0x0 = Disable COL indication in full duplex mode 0x1 = Enable COL indication in full duplex mode
2	LEGACY_CODING_TXMODE_EN	R/W	0x1	0x0 = Disable automatic selection of Legacy scrambler mode in 1G, Master mode 0x1 = Enable automatic selection of Legacy scrambler mode in 1G, Master mode
1	MASTER_SEMI_CROSS_EN	R/W	0x1	0x0 = Disable semi-cross mode in 1G Master mode 0x1 = Enable semi-cross mode in 1G Master mode
0	SLAVE_SEMI_CROSS_EN	R/W	0x1	0x0 = Disable semi-cross mode in 1G Slave mode 0x1 = Enable semi-cross mode in 1G Slave mode

9.6.1.20 RX_ERR_CNT Register (Address = 0x15) [reset = 0x0]

RX_ERR_CNT is shown in Figure 52 and described in Table 40.

Return to Summary Table.

Figure 52. RX_ERR_CNT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_ERROR_COUNT															
R/W1C-0x0															

Table 40. RX_ERR_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	RX_ERROR_COUNT	R/W1C	0x0	Receive Error Counter

9.6.1.21 BIST_CONTROL Register (Address = 0x16) [reset = 0x0]

BIST_CONTROL is shown in Figure 53 and described in Table 41.

Return to Summary Table.

This register is used for Build-In Self Test (BIST) configuration. The BIST functionality provides Pseudo Random Bit Stream (PRBS) mechanism including packet generation generator and checker. Selection of the exact loopback point in the signal chain is also done in this register.

Figure 53. BIST_CONTROL Register

15	14	13	12	11	10	9	8
PACKET_GEN_EN_3:0				RESERVED		RESERVED	RESERVED
R/W-0x0				R-0x0		R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
REV_LOOP_RX_DATA_CTRL	MII_LOOP_TX_DATA_CTRL	LOOP_TX_DATA_MIX				LOOPBACK_MODE	
R/W-0x0	R/W-0x0	R/W-0x0				R/W-0x0	

Table 41. BIST_CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	PACKET_GEN_EN_3:0	R/W	0x0	These bits along controls PRBS generator.Other values are not applicable. 0x0 = Disable PRBS 0xF = Enable Continuous PRBS
11-10	RESERVED	R	0x0	Reserved
9	RESERVED	R/W	0x0	Reserved
8	RESERVED	R/W	0x0	Reserved
7	REV_LOOP_RX_DATA_CTRL	R/W	0x0	Reverse Loopback Receive Data Control: This bit may only be set in Reverse Loopback mode 0x0 = Suppress RX packets to MAC in reverse loop 0x1 = Send RX packets to MAC in reverse loop
6	MII_LOOP_TX_DATA_CTRL	R/W	0x0	MII Loopback Transmit Data Control: This bit may only be set in MII Loopback mode 0x0 = Suppress data to MDI in MII loop 0x1 = Transmit data to MDI in MII loop
5-2	LOOP_TX_DATA_MIX	R/W	0x0	Loopback Mode Select: PCS loopback must be disabled (Bits[1:0] = 00) 0x0 = No Loopback 0x1 = Digital Loopback 0x2 = Analog Loopback 0x4 = External Loopback 0x8 = Reverse Loopback

Table 41. BIST_CONTROL Register Field Descriptions (continued)

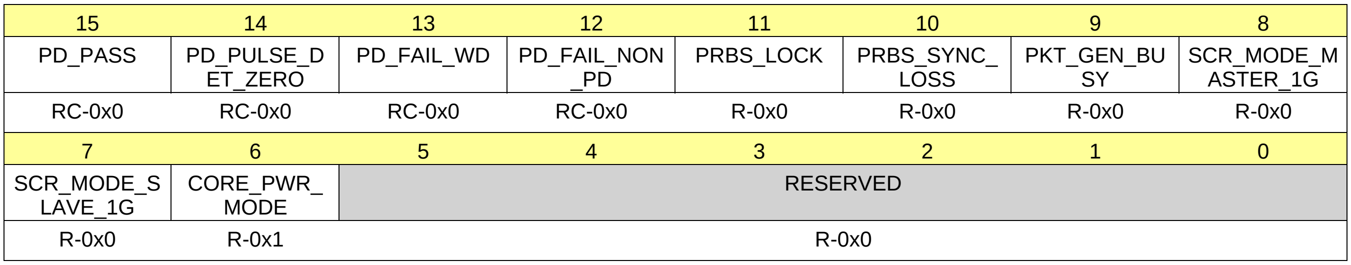
Bit	Field	Type	Reset	Description
1-0	LOOPBACK_MODE	R/W	0x0	PCS Loopback Select When configured in 1000Base-T x1b = Loop before 1000Base-T signal processing. When configured in 100Base-TX 0x0 = See bits [5:2] 01b = Loop before scrambler 10b = Loop after scrambler, before MLT3 encoder 11b = Loop after MLT3 encoder

9.6.1.22 GEN_STATUS2 Register (Address = 0x17) [reset = 0x40]

GEN_STATUS2 is shown in Figure 54 and described in Table 42.

Return to Summary Table.

Figure 54. GEN_STATUS2 Register



15	14	13	12	11	10	9	8
PD_PASS	PD_PULSE_DET_ZERO	PD_FAIL_WD	PD_FAIL_NON_PD	PRBS_LOCK	PRBS_SYNC_LOSS	PKT_GEN_BUSY	SCR_MODE_MASTER_1G
RC-0x0	RC-0x0	RC-0x0	RC-0x0	R-0x0	R-0x0	R-0x0	R-0x0
7	6	5	4	3	2	1	0
SCR_MODE_SLAVE_1G	CORE_PWR_MODE	RESERVED					
R-0x0	R-0x1	R-0x0					

Table 42. GEN_STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PD_PASS	RC	0x0	1b = PD (Powered Device) has been successfully detected 0b = PD has not been detected
14	PD_PULSE_DET_ZERO	RC	0x0	1b = PD detection mechanism has received no signal 0b = PD detection mechanism has received signal
13	PD_FAIL_WD	RC	0x0	1b = PD detection mechanism watchdog has expired 0b = PD detection mechanism watchdog has not expired
12	PD_FAIL_NON_PD	RC	0x0	1b = PD detection mechanism has detected a non-powered device 0b = PD detection mechanism has not detected a non-powered device
11	PRBS_LOCK	R	0x0	1b = PRBS checker is locked sync) on received byte stream 0b = PRBS checker is not locked
10	PRBS_SYNC_LOSS	R	0x0	1b = PRBS checker has lost sync 0b = PRBS checker has not lost sync LH - clear on read register
9	PKT_GEN_BUSY	R	0x0	1b = Packet generator is in process 0b = Packet generator is not in process
8	SCR_MODE_MASTER_1G	R	0x0	1b = 1G PCS (master) is in legacy encoding mode 0b = 1G PCS (master) is in normal encoding mode
7	SCR_MODE_SLAVE_1G	R	0x0	1b = 1G PCS (slave) is in legacy encoding mode 0b = 1G PCS (slave) is in normal encoding mode
6	CORE_PWR_MODE	R	0x1	1b = Core is in normal power mode 0b = Core is powered down or in sleep mode
5-0	RESERVED	R	0x0	Reserved

9.6.1.23 LEDS_CFG1 Register (Address = 0x18) [reset = 0x6150]

LEDS_CFG1 is shown in Figure 55 and described in Table 43.

Return to Summary Table.

Figure 55. LEDS_CFG1 Register

15	14	13	12	11	10	9	8
LED_GPIO_SEL				LED_2_SEL			
R/W-0x6				R/W-0x1			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LED_1_SEL				LED_0_SEL			
R/W-0x5				R/W-0x0			

Table 43. LEDS_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	LED_GPIO_SEL	R/W	0x6	Source of GPIO LED, same as bits 3:0
11-8	LED_2_SEL	R/W	0x1	Source of LED_2 (LED 2) , same as bits 3:0
7-4	LED_1_SEL	R/W	0x5	Source of LED_1 (LED 1) , same as bits 3:0
3-0	LED_0_SEL	R/W	0x0	Source of LED_0 (LED 0) 0x0 = link OK 0x1 = RX/TX activity 0x2 = TX activity 0x3 = RX activity 0x4 = collision detected 0x5 = 1000BT link is up 0x6 = 100 BTX link is up 0x7 = 10BT link is up 0x8 = 10/100BT link is up 0x9 = 100/1000BT link is up 0xA = full duplex 0xB = link OK + blink on TX/RX activity 0xC = NA 0xD = RX_ER or TX_ER 0xE = RX_ER

9.6.1.24 LEDS_CFG2 Register (Address = 0x19) [reset = 0x4444]

LEDS_CFG2 is shown in Figure 56 and described in Table 44.

Return to Summary Table.

Figure 56. LEDS_CFG2 Register

15	14	13	12	11	10	9	8
RESERVED	LED_GPIO_POLARITY	LED_GPIO_DRV_VAL	LED_GPIO_DRV_EN	RESERVED	LED_2_POLARITY	LED_2_DRV_VAL	LED_2_DRV_EN
R-0x0	R/W-0x1	R/W-0x0	R/W-0x0	R-0x0	R/W-0x1	R/W-0x0	R/W-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	LED_1_POLARITY	LED_1_DRV_VAL	LED_1_DRV_EN	RESERVED	LED_0_POLARITY	LED_0_DRV_VAL	LED_0_DRV_EN
R-0x0	R/W-0x1	R/W-0x0	R/W-0x0	R-0x0	R/W-0x1	R/W-0x0	R/W-0x0

Table 44. LEDS_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	LED_GPIO_POLARITY	R/W	0x1	GPIO LED polarity: Default depends on strap, non strap default Active High 0x0 = Active low 0x1 = Active high
13	LED_GPIO_DRV_VAL	R/W	0x0	If bit #12 is set, this is the value of GPIO LED
12	LED_GPIO_DRV_EN	R/W	0x0	Force value to LED_GPIO as per bit #13 0x0 = LED_GPIO is in normal operation mode 0x1 = Force the value of LED_GPIO
11	RESERVED	R	0x0	Reserved
10	LED_2_POLARITY	R/W	0x1	LED_2 polarity. Default depends on strap, non strap default Active High 0x0 = Active low 0x1 = Active high
9	LED_2_DRV_VAL	R/W	0x0	If bit #8 is set, this is the value of LED_2
8	LED_2_DRV_EN	R/W	0x0	Force value to LED_GPIO as per bit #9 0x0 = LED_2 is in normal operation mode 0x1 = Drive the value of LED_2
7	RESERVED	R	0x0	Reserved
6	LED_1_POLARITY	R/W	0x1	LED_1 polarity: Default depends on strap, non strap default Active High 0x0 = Active low 0x1 = Active high
5	LED_1_DRV_VAL	R/W	0x0	If bit #4 is set, this is the value of LED_1
4	LED_1_DRV_EN	R/W	0x0	Force value to LED_GPIO as per bit #5 0x0 = LED_1 is in normal operation mode 0x1 = Drive the value of LED_1
3	RESERVED	R	0x0	Reserved
2	LED_0_POLARITY	R/W	0x1	LED_0 polarity: Default depends on strap, non strap default Active High 0x0 = Active low 0x1 = Active high
1	LED_0_DRV_VAL	R/W	0x0	If bit #1 is set, this is the value of LED_0
0	LED_0_DRV_EN	R/W	0x0	Force value to LED_GPIO as per bit #1 0x0 = LED_0 is in normal operation mode 0x1 = Drive the value of LED_0

9.6.1.25 LEDS_CFG3 Register (Address = 0x1A) [reset = 0x2]

LEDS_CFG3 is shown in Figure 57 and described in Table 45.

Return to Summary Table.

Figure 57. LEDS_CFG3 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED					LEDS_BYPASS_STRETCHING	LEDS_BLINK_RATE	
R-0x0					R/W-0x0	R/W-0x2	

Table 45. LEDS_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R	0x0	Reserved
2	LEDS_BYPASS_STRETCHING	R/W	0x0	0b = Noraml Operation 1b = Bypass LEDs stretching
1-0	LEDS_BLINK_RATE	R/W	0x2	00b = 20Hz (50mSec) 01b = 10Hz (100mSec) 10b = 5Hz (200mSec) 11b = 2Hz (500mSec)

9.6.1.26 GEN_CFG4 Register (Address = 0x1E) [reset = 0x12]

GEN_CFG4 is shown in Figure 58 and described in Table 46.

Return to Summary Table.

Figure 58. GEN_CFG4 Register

15	14	13	12	11	10	9	8
RESERVED	CFG_FAST_ANEG_EN	CFG_FAST_ANEG_SEL_VAL		CFG_ANEG_ADV_FD_EN	RESTART_STATUS_BITS_EN	CFG_ROBUST_AMDIX_EN	CFG_FAST_AMDIX_EN
R/W-0x0	R/W-0x0	R/W-0x0		R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
INT_OE	FORCE_INTERRUPT	RESERVED	RESERVED	FORCE_1G_AUTONEG_EN	TDR_FAIL	TDR_DONE	TDR_START
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1	R/W-0x0	R-0x0	R-0x1	RH/WtoP-0x0

Table 46. GEN_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R/W	0x0	Reserved
14	CFG_FAST_ANEG_EN	R/W	0x0	Enable Fast ANEG mode
13-12	CFG_FAST_ANEG_SEL_VAL	R/W	0x0	when Fast ANEG mode enabled, value will select short timer duration 0x0 will be the shortest timers config and 0x2 the longest
11	CFG_ANEG_ADV_FD_EN	R/W	0x0	this but enables to declare FD also in parallel detect link, the IEEE defien on parallel detect to always declare HD, this bit allows also to declare FD in this scenario
10	RESTART_STATUS_BITS_EN	R/W	0x0	reset enable 1b = clear all the phy status bits (part of register 0x11) 0b = do not clear the status bit
9	CFG_ROBUST_AMDIX_EN	R/W	0x0	Enable Robust Auto MDI/MDIX resolution
8	CFG_FAST_AMDIX_EN	R/W	0x0	Enabe Fast Auto MDI-X mode
7	INT_OE	R/W	0x0	Interrupt Output Enable: 1b = INTN/PWDNN Pad is an Interrupt Output 0b = INTN/PWDNN Pad in an Power Down Input
6	FORCE_INTERRUPT	R/W	0x0	1b = Assert interrupt pin 0b = Normal interrupt mode
5	RESERVED	R/W	0x0	Reserved

Table 46. GEN_CFG4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	RESERVED	R/W	0x1	Reserved
3	FORCE_1G_AUTONEG_EN	R/W	0x0	1b = Invoke Auto-Negotiation with only 1G advertised when manual speed in register 0 is 1G 0b = Do not invoke Auto-Negotiation when manual speed in register 0 is 1G
2	TDR_FAIL	R	0x0	
1	TDR_DONE	R	0x1	
0	TDR_START	RH/WtoP	0x0	1b = Start TDR 0b = TDR Completed

9.6.1.27 GEN_CTRL Register (Address = 0x1F) [reset = 0x0]

GEN_CTRL is shown in Figure 59 and described in Table 47.

Return to Summary Table.

Figure 59. GEN_CTRL Register

15	14	13	12	11	10	9	8
SW_RESET	SW_RESTART	RESERVED	RESERVED				
RH/WtoP-0x0	RH/WtoP-0x0	R/W-0x0	R/W-0x0				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RESERVED						
R/W-0x0	R/W-0x0						

Table 47. GEN_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SW_RESET	RH/WtoP	0x0	Software Reset This will reset the PHY and return registers to their default values. Registers controlled via strap pins will return back to their last strapped values. 0x0 = Normal mode 0x1 = Reset PHY
14	SW_RESTART	RH/WtoP	0x0	Soft Restart Restarts the PHY without affecting registers. 0x0 = Normal Operation 0x1 = Software Reset
13	RESERVED	R/W	0x0	Reserved
12-7	RESERVED	R/W	0x0	Reserved
6-0	RESERVED	R/W	0x0	Reserved

9.6.1.28 ANALOG_TEST_CTRL Register (Address = 0x25) [reset = 0x480]

ANALOG_TEST_CTRL is shown in Figure 60 and described in Table 48.

Return to Summary Table.

Figure 60. ANALOG_TEST_CTRL Register

15	14	13	12	11	10	9	8
RESERVED				TM7_PULSE_SEL		EXTND_TM7_100BT_MSB	EXTND_TM7_100BT_EN
R-0x0				R/W-0x1		R/W-0x0	R/W-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STIM_CH_SEL			ANALOG_TEST				
R/W-0x4			R/W-0x0				

Table 48. ANALOG_TEST_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11-10	TM7_PULSE_SEL	R/W	0x1	Selects pulse amplitude and polarity for Test Mode 7 (See register 0x9): 00b = +2 01b = -2 10b = +1 11b = -1
9	EXTND_TM7_100BT_MSB	R/W	0x0	MSB of configurable length for 100BT extended TM7 For 100BT Test Mode: repetitive sequence of "1" with configurable number of "0". Bits { 9,[3:0] } define the number of "0" to follow the "1", from 1 to 31. 0,0001 - 1,1111 : single "0" to 31 zeros. 0,0000 - clear the shiftreg.
8	EXTND_TM7_100BT_EN	R/W	0x0	Enable extended TM7 for 100M. NOTE1: bit 4 must be "0" for 100BT TestMode. NOTE2: 100BT testmode must be Clear before appling new Value. e.g, one need to write 0x0 before configuring new value. NOTE3: use FORCE100 for 100BT testing, via Reg0x0.
7-5	STIM_CH_SEL	R/W	0x4	Selects the channel(s) that outputs the test mode: If bit #7 is set, test mode is driven to all channels. If bit #7 is cleared, test mode is driven according to bits 6:5 - 00b = Channel A 01b = Channel B 10b = Channel C 11b = Channel D
4-0	ANALOG_TEST	R/W	0x0	Bit [4] enables 10BaseT test modes. Bits [3:0] select the 10BaseT test pattern, as follows: To operate extended TM7 for 100BT, bits 3:0 shall be configured as well - more details in bit #9 0000b = Single NLP 0001b = Single Pulse 1 0010b = Single Pulse 0 0011b = Repetitive 1 0100b = Repetitive 0 0101b = Preamble (repetitive "10") 0110b = Single 1 followed by TP_IDLE 0111b = Single 0 followed by TP_IDLE 1000b = Repetitive "1001" sequence 1001b = Random 10Base-T data 1010b = TP_IDLE_00 1011b = TP_IDLE_01 1100b = TP_IDLE_10 1101b = TP_IDLE_11 0110b = Proprietary T.M for amplitude, RFT, DCD and template for FT on tester (1000) ---> need to write register 0 0x2000

9.6.1.29 GEN_CFG_ENH_AMIX Register (Address = 0x2C) [reset = 0x141F]

GEN_CFG_ENH_AMIX is shown in Figure 61 and described in Table 49.

Return to Summary Table.

Figure 61. GEN_CFG_ENH_AMIX Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="5">CFG_FLD_WINDW_CNT</td><td>CFG_FAST_AMDIX_VAL</td></tr>
<tr><td colspan="2">R-0x0</td><td colspan="5">R/W-0xA</td><td>R/W-0x1</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">CFG_FAST_AMDIX_VAL</td><td colspan="4">CFG_ROBUST_AMDIX_VAL</td></tr>
<tr><td colspan="4">R/W-0x1</td><td colspan="4">R/W-0xF</td></tr>
</table>

Table 49. GEN_CFG_ENH_AMIX Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-9	CFG_FLD_WINDW_CNT	R/W	0xA	counter to define the wondow in which we lok for fast link down criteria, default 10usec
8-4	CFG_FAST_AMDIX_VAL	R/W	0x1	timer of the mdi/x switch cuonterin force 100m fast amdix mode, very fast as it need only to allow far end to detect energy ~4ms in default
3-0	CFG_ROBUST_AMDIX_VAL	R/W	0xF	the value of the timer that switch mdi/x in robust mode, this shoul be long timer to allow far end to still do parallel detect witht he IEEE ANEG timers... default ~0.5s

9.6.1.30 GEN_CFG_FLD Register (Address = 0x2D) [reset = 0x0]

GEN_CFG_FLD is shown in Figure 62 and described in Table 50.

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Figure 62. GEN_CFG_FLD Register

15	14	13	12	11	10	9	8
CFG_FORCE_DROP_LINK_EN	FLD_BYPASS_MAX_WAIT_TIMER	SLICER_OUT_STUCK	FLD_STATUS				
R/W-0x0	R/W-0x0	R-0x0	R-0x0				
7	6	5	4	3	2	1	0
RESERVED			CFG_FAST_LINK_DOWN_MODES				
R-0x0			R/W-0x0				

Table 50. GEN_CFG_FLD Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CFG_FORCE_DROP_LINK_EN	R/W	0x0	Drop link (stop transmitting) when no signal is received
14	FLD_BYPASS_MAX_WAIT_TIMER	R/W	0x0	If set, MAX_WAIT_TIMER is skipped (and therefore link is dropped faster)
13	SLICER_OUT_STUCK	R	0x0	indicate slicer)out_stuck status
12-8	FLD_STATUS	R	0x0	Fast link down status LH - clear on read register
7-5	RESERVED	R	0x0	Reserved
4-0	CFG_FAST_LINK_DOWN_MODES	R/W	0x0	5 bits for different fast link down option (can all work simultaniously): bit [0] - energy lost bit [1] - mse bit [2] - mlt3 errors bit [3] - rx_err bit [4] - descrambler sync loss

9.6.1.31 GEN_CFG_FLD_THR Register (Address = 0x2E) [reset = 0x221]

GEN_CFG_FLD_THR is shown in Figure 63 and described in Table 51.

Return to Summary Table.

Figure 63. GEN_CFG_FLD_THR Register

15	14	13	12	11	10	9	8
RESERVED					ENERGY_WINDOW_LEN_FLD		
R-0x0					R/W-0x2		
7	6	5	4	3	2	1	0
RESERVED	ENERGY_ON_FLD_THR			RESERVED	ENERGY_LOST_FLD_THR		
R-0x0	R/W-0x2			R-0x0	R/W-0x1		

Table 51. GEN_CFG_FLD_THR Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	RESERVED	R	0x0	Reserved
10-8	ENERGY_WINDOW_LEN_FLD	R/W	0x2	window length in FLD energy lost mode for energy detection accumulator
7	RESERVED	R	0x0	Reserved
6-4	ENERGY_ON_FLD_THR	R/W	0x2	energy lost threshold for FLD energy lost mode. energy_detected indication will be asserted when energy detector accumulator exceeds this threshold.
3	RESERVED	R	0x0	Reserved

Table 51. GEN_CFG_FLD_THR Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	ENERGY_LOST_FLD_THR	R/W	0x1	energy lost threshold for FLD energy lost mode energy_lost indication will be asserted if energy detector accumulator falls below this threshold.

9.6.1.32 GEN_CFG3 Register (Address = 0x31) [reset = 0x10B0]

GEN_CFG3 is shown in Figure 64 and described in Table 52.

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Figure 64. GEN_CFG3 Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED			RESERVED
R-0x0	R/W-0x0	R/W-0x0	R/W-0x1	R-0x0			R/W-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	SGMII_AUTONEG_TIMER		RESERVED	RESERVED	RESERVED	RESERVED	PORT_MIRRORING_MODE
R/W-0x1	R/W-0x1		R/W-0x1	R/W-0x0	R/W-0x0	R-0x0	R/W-0x0

Table 52. GEN_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R/W	0x0	Reserved
13	RESERVED	R/W	0x0	Reserved
12	RESERVED	R/W	0x1	Reserved
11-9	RESERVED	R	0x0	Reserved
8	RESERVED	R/W	0x0	Reserved
7	RESERVED	R/W	0x1	Reserved
6-5	SGMII_AUTONEG_TIMER	R/W	0x1	Selects duration of SGMII Auto-Negotiation timer: 00: 1.6ms 01: 2µs 10: 800µs 11: 11ms
4	RESERVED	R/W	0x1	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R	0x0	Reserved
0	PORT_MIRRORING_MODE	R/W	0x0	Port mirroring mode: 0 - Disabled 1 - Enabled

9.6.1.33 RGMII_CTRL Register (Address = 0x32) [reset = 0xD0]

RGMII_CTRL is shown in Figure 65 and described in Table 53.

Return to Summary Table.

Figure 65. RGMII_CTRL Register

15	14	13	12	11	10	9	8
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
R-0x0	R-0x0	R-0x0	R-0x0	R/W-0x0	R-0x0	R/W-0x0	R/W-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	RGMII_RX_HALF_FULL_THR		RGMII_TX_HALF_FULL_THR		SUPPRESS_TX_ERR_EN	RGMII_TX_CLK_DELAY	RGMII_RX_CLK_DELAY

R/W-0x1	R/W-0x2	R/W-0x2	R/W-0x0	R/W-0x0	R/W-0x0

Table 53. RGMII_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14	RESERVED	R	0x0	Reserved
13	RESERVED	R	0x0	Reserved
12	RESERVED	R	0x0	Reserved
11	RESERVED	R/W	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R/W	0x0	Reserved
8	RESERVED	R/W	0x0	Reserved
7	RESERVED	R/W	0x1	Reserved
6-5	RGMII_RX_HALF_FULL_THR	R/W	0x2	RGMII RX sync FIFO half full threshold 2 lsbs [1:0], msb [2] in reg 0x33 In the RX our default is recovered mode (can change in reg 0x0060 #4 below) In recovered mode we can reduce the threshold in from 2 to 1, this will save 8 nsec in 1G, and 40/400 in 100/10M
4-3	RGMII_TX_HALF_FULL_THR	R/W	0x2	RGMII TX sync FIFO half full threshold 2 lsbs [1:0], - the msb is on reg 0x33 - [2]
2	SUPPRESS_TX_ERR_EN	R/W	0x0	
1	RGMII_TX_CLK_DELAY	R/W	0x0	RGMII Transmit Clock Delay 0x0 = RGMII transmit clock is shifted with respect to transmit data. 0x1 = RGMII transmit clock is aligned with respect to transmit data.
0	RGMII_RX_CLK_DELAY	R/W	0x0	RGMII Receive Clock Delay 0x0 = RGMII receive clock is shifted with respect to receive data. 0x1 = RGMII transmit clock is aligned with respect to receive data.

9.6.1.34 RGMII_CTRL2 Register (Address = 0x33) [reset = 0x0]

RGMII_CTRL2 is shown in Figure 66 and described in Table 54.

Return to Summary Table.

Figure 66. RGMII_CTRL2 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED			RGMII_AF_BYPASS_EN	RGMII_AF_BYPASS_DLY_EN	LOW_LATENCY_10_100_EN	RESERVED	RESERVED
R-0x0			R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 54. RGMII_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-5	RESERVED	R	0x0	Reserved
4	RGMII_AF_BYPASS_EN	R/W	0x0	RGMII Async FIFO Bypass Enable: 1 = Enable RGMII Async FIFO Bypass. 0 = Normal operation.
3	RGMII_AF_BYPASS_DLY_EN	R/W	0x0	RGMII Async FIFO Bypass Delay Enable: 1 = Delay RX_CLK when operating in 10/100 with RGMII. 0 = Normal operation
2	LOW_LATENCY_10_100_EN	R/W	0x0	Low Latency 10/100 Enable: 1 = Enable low latency in 10/100 operation. 0 = Normal operation.
1	RESERVED	R/W	0x0	Reserved
0	RESERVED	R/W	0x0	Reserved

9.6.1.35 SGMII_AUTO_NEG_STATUS Register (Address = 0x37) [reset = 0x0]

SGMII_AUTO_NEG_STATUS is shown in Figure 67 and described in Table 55.

Return to Summary Table.

Figure 67. SGMII_AUTO_NEG_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED						SGMII_PAGE_RX	SGMII_AUTONEG_COMPLETE
R-0x0						R-0x0	R-0x0

Table 55. SGMII_AUTO_NEG_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-2	RESERVED	R	0x0	Reserved
1	SGMII_PAGE_RX	R	0x0	1b = indicate that a new auto-neg page was received
0	SGMII_AUTONEG_COMPLETE	R	0x0	1b = Auto-Negotiation process completed 0b = Auto-Negotiation process not completed

9.6.1.36 PRBS_TX_CHK_CTRL Register (Address = 0x39) [reset = 0x0]

PRBS_TX_CHK_CTRL is shown in Figure 68 and described in Table 56.

Return to Summary Table.

Figure 68. PRBS_TX_CHK_CTRL Register

15	14	13	12	11	10	9	8
RESERVED	PRBS_TX_CHK_ERR_CNT						
R-0x0	R-0x0						
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRBS_TX_CHK_ERR_CNT	RESERVED	PRBS_TX_CHK_SYNC_LOSS	PRBS_TX_CHK_LOCK_STS	RESERVED	PRBS_TX_CHK_BYTE_CNT_OVF	PRBS_TX_CHK_CNT_MODE	PRBS_TX_CHK_EN
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R/W-0x0	R/W-0x0

Table 56. PRBS_TX_CHK_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14-7	PRBS_TX_CHK_ERR_CNT	R	0x0	Holds number of errored bytes that received by the PRBS TX checker. When TX PRBS Count Mode (see bit [1]) set to 0, count stops on 0xFF. Notes: Writing bit 7 generates a lock signal for the PRBS TX counters. Writing bit 8 generates a lock and clear signal for the PRBS TX counters
6	RESERVED	R	0x0	Reserved
5	PRBS_TX_CHK_SYNC_LOSS	R	0x0	1b = PRBS TX checker has lost sync 0b = PRBS TX checker has not lost sync This bit is LH
4	PRBS_TX_CHK_LOCK_STS	R	0x0	1b = PRBS TX checker is locked on received byte stream 0b = PRBS TX checker is not locked
3	RESERVED	R	0x0	Reserved
2	PRBS_TX_CHK_BYTE_CNT_OVF	R	0x0	If set, bytes counter reached overflow
1	PRBS_TX_CHK_CNT_MODE	R/W	0x0	PRBS Checker Mode 1b = Continuous mode 0b = Single Mode.
0	PRBS_TX_CHK_EN	R/W	0x0	If set, PRBS TX checker is enabled (PRBS TX checker is used in external reverse loop)

9.6.1.37 PRBS_TX_CHK_BYTE_CNT Register (Address = 0x3A) [reset = 0x0]

PRBS_TX_CHK_BYTE_CNT is shown in Figure 69 and described in Table 57.

Return to Summary Table.

Figure 69. PRBS_TX_CHK_BYTE_CNT Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRBS_TX_CHK_BYTE_CNT															
R-0x0															

Table 57. PRBS_TX_CHK_BYTE_CNT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PRBS_TX_CHK_BYTE_CNT	R	0x0	Holds number of total bytes that received by the PRBS TX checker. Value in this register is locked when write is done to register PRBS_TX_CHK_CTRL bit[7]or bit[8]. When PRBS Count Mode set to zero, count stops on 0xFFFF (see register 0x0016)

9.6.1.38 G_100BT_REG0 Register (Address = 0x43) [reset = 0x7A0]

G_100BT_REG0 is shown in Figure 70 and described in Table 58.

Return to Summary Table.

Figure 70. G_100BT_REG0 Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED	RESERVED		
R-0x0				R/W-0x0	R/W-0xF		

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FAST_RX_DV
R/W-0xF	R/W-0x0	R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 58. G_100BT_REG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11	RESERVED	R/W	0x0	Reserved
10-7	RESERVED	R/W	0xF	Reserved
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x1	Reserved
4	RESERVED	R/W	0x0	Reserved
3	RESERVED	R/W	0x0	Reserved
2	RESERVED	R/W	0x0	Reserved
1	RESERVED	R/W	0x0	Reserved
0	FAST_RX_DV	R/W	0x0	Enable Fast RX_DV for low latency in 100Mbps mode. 0x0 = Fast rx dv disable 0x1 = Fast rx dv enable

9.6.1.39 SERDES_SYNC_STS Register (Address = 0x4F) [reset = 0x0]

SERDES_SYNC_STS is shown in Figure 71 and described in Table 59.

Return to Summary Table.

Figure 71. SERDES_SYNC_STS Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td>RESERVED</td><td>RESERVED</td><td>RESERVED</td><td>SYNC_STATUS</td></tr>
<tr><td colspan="4">R/W-0x0</td><td>R/W-0x0</td><td>R-0x0</td><td>R-0x0</td><td>R-0x0</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="4">R-0x0</td><td colspan="4">R-0x0</td></tr>
</table>

Table 59. SERDES_SYNC_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11	RESERVED	R/W	0x0	Reserved
10	RESERVED	R	0x0	Reserved
9	RESERVED	R	0x0	Reserved
8	SYNC_STATUS	R	0x0	Synchronization Status 0x0 = No Sync 0x1 = Sync Established
7-4	RESERVED	R	0x0	Reserved
3-0	RESERVED	R	0x0	Reserved

9.6.1.40 STRAP_STS Register (Address = 0x6E) [reset = 0x0]

STRAP_STS is shown in Figure 72 and described in Table 60.

Return to Summary Table.

Figure 72. STRAP_STS Register

15	14	13	12	11	10	9	8
RESERVED		STRAP_LINK_LOSS_PASS_THRU	STRAP_MIRROR_EN	STRAP_OPMODE			STRAP_PHY_ADD
R-0x0		R-0x0	R-0x0	R-0x0			R-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STRAP_PHY_ADD				STRAP_ANEGSEL		STRAP_ANEG_EN	STRAP_RGMII_MII_SEL
R-0x0				R-0x0		R-0x0	R-0x0

Table 60. STRAP_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13	STRAP_LINK_LOSS_PASS_THRU	R	0x0	Link Loss Pass Through Enable Strap 0x0 = Enable 0x1 = Disable
12	STRAP_MIRROR_EN	R	0x0	Mirror Mode Enable StraP. Refer to strap configuration section as this strap also decides MAC interface in Bridge Mode applications. 0x0 = Disable 0x1 = Enable
11-9	STRAP_OPMODE	R	0x0	OPMODE Strap 0x0 = RGMII To Copper 0x1 = RGMII to 1000Base-X 0x2 = RGMII to 100Base-FX 0x3 = RGMII-SGMII Bridge 0x4 = 1000Base-T to 1000Base-X 0x5 = 100Base-T to 100Base-FX 0x6 = SGMII to Copper 0x7 = JTAG for Boundary Scan
8-4	STRAP_PHY_ADD	R	0x0	PHY Address Strap
3-2	STRAP_ANEGSEL	R	0x0	Auto Negotiation Mode Select Strap. Refer to Strap Configuration Section
1	STRAP_ANEG_EN	R	0x0	Auto Negotiation Enable Strap 0x0 = Enable 0x1 = Disable
0	STRAP_RGMII_MII_SEL	R	0x0	RGMII to MII Enable Strap 0x0 = RGMII mode 0x1 = MII Mode

9.6.1.41 ANA_RGMII_DLL_CTRL Register (Address = 0x86) [reset = 0x77]

ANA_RGMII_DLL_CTRL is shown in Figure 73 and described in Table 61.

Return to Summary Table.

Figure 73. ANA_RGMII_DLL_CTRL Register

15	14	13	12	11	10	9	8
RESERVED						DLL_EN_FORCE_VAL	DLL_EN_FORCE_CTRL
R-0x0						R/W-0x0	R/W-0x0

7	6	5	4	3	2	1	0
DLL_TX_DELAY_CTRL_SL				DLL_RX_DELAY_CTRL_SL			
R/W-0x7				R/W-0x7			

Table 61. ANA_RGMII_DLL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	DLL_EN_FORCE_VAL	R/W	0x0	If dll_en_force_en is set, this is the value of DLL_EN
8	DLL_EN_FORCE_CTRL	R/W	0x0	Force DLL_EN value
7-4	DLL_TX_DELAY_CTRL_SL	R/W	0x7	Steps of 250ps, affects the CLK_90 output. - same behavior as bit [3:0]
3-0	DLL_RX_DELAY_CTRL_SL	R/W	0x7	Steps of 250ps, affects the CLK_90 output. b[3],b[2],b[1],b[0], shift, mode 0, 1, 1, 1, 2.0ns, Shift (*) - default 0, 1, 0, 1, 1.5ns, Shift 0, 0, 1, 1, 1.0ns, Shift 0, 0, 0, 1, 0.5ns, Shift 1, 1, 1, 1, 0ns, Align (**) 1, 1, 0, 1, 3.5ns, Shift 1, 0, 1, 1, 3.0ns, Shift 1, 0, 0, 1, 2.5ns, Shift please note - the actual delay is also effected by the shift mode in reg 0x32

9.6.1.42 RXF_CFG Register (Address = 0x134) [reset = 0x1000]

RXF_CFG is shown in Figure 74 and described in Table 62.

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Figure 74. RXF_CFG Register

15	14	13	12	11	10	9	8
RESERVED		RESERVED	RESERVED	WOL_OUT_CLEAN	WOL_OUT_STRETCH		WOL_OUT_MODE
R/W-0x0		R/W-0x0	R/W-0x1	RH/WoP-0x0	R/W-0x0		R/W-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ENHANCED_MAC_SUPPORT	RESERVED	RESERVED	WAKE_ON_UCAST	RESERVED	WAKE_ON_BCAST	WAKE_ON_PATTERN	WAKE_ON_MAGIC
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 62. RXF_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0x0	Reserved
13	RESERVED	R/W	0x0	Reserved
12	RESERVED	R/W	0x1	Reserved
11	WOL_OUT_CLEAN	RH/WoP	0x0	If WOL out is in level mode in bit 8, writing to this bit will clear it.
10-9	WOL_OUT_STRETCH	R/W	0x0	If WOL out is in pulse mode in bit 8, this is the pulse length: 0x0 = 8 clock cycles 0x1 = 16 clock cycles 0x2 = 32 clock cycles 0x3 = 64 clock cycles
8	WOL_OUT_MODE	R/W	0x0	Mode of the wake up that goes to GPIO pin: 0x0 = Pulse Mode. 0x1 = Level Mode
7	ENHANCED_MAC_SUPPORT	R/W	0x0	Enables enhanced RX features. This bit should be set when using wakeup abilities, CRC check or RX 1588 indication
6	RESERVED	R/W	0x0	Reserved
5	RESERVED	R/W	0x0	Reserved

Table 62. RXF_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	WAKE_ON_UCAST	R/W	0x0	If set, issue an interrupt upon reception of unicast packets
3	RESERVED	R/W	0x0	Reserved
2	WAKE_ON_BCAST	R/W	0x0	If set, issue an interrupt upon reception of broadcast packets
1	WAKE_ON_PATTERN	R/W	0x0	If set, issue an interrupt upon reception of a packet with configured pattern
0	WAKE_ON_MAGIC	R/W	0x0	If set, issue an interrupt upon reception of magic packet

9.6.1.43 RXF_STATUS Register (Address = 0x135) [reset = 0x0]

RXF_STATUS is shown in Figure 75 and described in Table 63.

Return to Summary Table.

Figure 75. RXF_STATUS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SFD_ERR	BAD_CRC	RESERVED	UCAST_RCVD	RESERVED	BCAST_RCVD	PATTERN_RCVD	MAGIC_RCVD
RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0

Table 63. RXF_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESERVED	R	0x0	Reserved
7	SFD_ERR	RC	0x0	SFD Error Detected
6	BAD_CRC	RC	0x0	Bad CRC Packet Received
5	RESERVED	RC	0x0	Reserved
4	UCAST_RCVD	RC	0x0	Unicast Packet Received
3	RESERVED	RC	0x0	Reserved
2	BCAST_RCVD	RC	0x0	Broadcast Packet Received
1	PATTERN_RCVD	RC	0x0	Pattern Match Packet Received
0	MAGIC_RCVD	RC	0x0	Magic Packet Received

9.6.1.44 IO_MUX_CFG Register (Address = 0x170) [reset = X]

IO_MUX_CFG is shown in Figure 76 and described in Table 64.

Return to Summary Table.

Figure 76. IO_MUX_CFG Register

15	14	13	12	11	10	9	8
RESERVED			CLK_O_SEL				
R-0x0			R/W-0xC				
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	CLK_O_DISABLE	RESERVED	MAC_IMPEDANCE_CTRL				
R-0x0	R/W-X	R/W-0x0	R/W-0x10				

Table 64. IO_MUX_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0x0	Reserved
12-8	CLK_O_SEL	R/W	0xC	Select clock output source 0x0 = Channel A receive clock 0x1 = Channel B receive clock 0x2 = Channel C receive clock 0x3 = Channel D receive clock 0x4 = Channel A receive clock divided by 5 0x5 = Channel B receive clock divided by 5 0x6 = Channel C receive clock divided by 5 0x7 = Channel D receive clock divided by 5 0x8 = Channel A transmit clock 0x9 = Channel B transmit clock 0xA = Channel C transmit clock 0xB = Channel D transmit clock 0xC = Reference clock (synchronous to XI input clock)
7	RESERVED	R	0x0	Reserved
6	CLK_O_DISABLE	R/W	X	Clock Out Disable 0x0 = Clock Out Enable 0x1 = Clock Out Disable
5	RESERVED	R/W	0x0	Reserved
4-0	MAC_IMPEDANCE_CTRL	R/W	0x10	Impedance Control for MAC I/Os: Output impedance approximate range from 35-70 Ω in 32 steps. Lowest being 11111 and highest being 00000. Range and Step size will vary with process. Default is set to 50 Ω by trim but the default register value can vary by process. Non default values of MAC I/O impedance can be used based on trace impedance. Mismatch between device and trace impedance can cause voltage overshoot and undershoot.

9.6.1.45 TDR_GEN_CFG1 Register (Address = 0x180) [reset = 0x752]

TDR_GEN_CFG1 is shown in Figure 77 and described in Table 65.

Return to Summary Table.

Figure 77. TDR_GEN_CFG1 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="3">RESERVED</td><td>TDR_CH_CD_BYPASS</td><td>TDR_CROSS_MODE_DIS</td><td>TDR_NLP_CHECK</td><td colspan="2">TDR_AVG_NUM</td></tr>
<tr><td colspan="3">R/W-0x0</td><td>R/W-0x0</td><td>R/W-0x0</td><td>R/W-0x1</td><td colspan="2">R/W-0x6</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>TDR_AVG_NUM</td><td colspan="3">TDR_SEG_NUM</td><td colspan="4">TDR_CYCLE_TIME</td></tr>
<tr><td>R/W-0x6</td><td colspan="3">R/W-0x5</td><td colspan="4">R/W-0x2</td></tr>
</table>

Table 65. TDR_GEN_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R/W	0x0	Reserved
12	TDR_CH_CD_BYPASS	R/W	0x0	Bypass channel C and D in TDR tests

Table 65. TDR_GEN_CFG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	TDR_CROSS_MODE_DIS	R/W	0x0	If set, disable cross mode option - never check the cross (Listen only to the same channel you transmit)
10	TDR_NLP_CHECK	R/W	0x1	If set, check for NLPs during silence
9-7	TDR_AVG_NUM	R/W	0x6	Number Of TDR Cycles to Average: 000b = 1 TDR cycle 001b = 2 TDR cycles 010b = 4 TDR cycles 011b = 8 TDR cycles 100b = 16 TDR cycles 101b = 32 TDR cycles 110b = 64 TDR cycles (default) 111b = Reserved
6-4	TDR_SEG_NUM	R/W	0x5	Number of TDR segments to check
3-0	TDR_CYCLE_TIME	R/W	0x2	Number of micro-seconds in each TDR cycle

9.6.1.46 TDR_GEN_CFG2 Register (Address = 0x181) [reset = 0xC850]

TDR_GEN_CFG2 is shown in Figure 78 and described in Table 66.

Return to Summary Table.

Figure 78. TDR_GEN_CFG2 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">TDR_SILENCE_TH</td></tr>
<tr><td colspan="8">R/W-0xC8</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">TDR_POST_SILENCE_TIME</td><td colspan="2">TDR_PRE_SILENCE_TIME</td><td colspan="4">RESERVED</td></tr>
<tr><td colspan="2">R/W-0x1</td><td colspan="2">R/W-0x1</td><td colspan="4">R-0x0</td></tr>
</table>

Table 66. TDR_GEN_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_SILENCE_TH	R/W	0xC8	Energy detection threshold
7-6	TDR_POST_SILENCE_TIME	R/W	0x1	timer for tdr to look for energy after TDR transaction, if energy detected this is fail tdr
5-4	TDR_PRE_SILENCE_TIME	R/W	0x1	timer for tdr to look for energy before starting , if energy detected this is fail tdr
3-0	RESERVED	R	0x0	Reserved

9.6.1.47 TDR_SEG_DURATION1 Register (Address = 0x182) [reset = 0x5326]

TDR_SEG_DURATION1 is shown in Figure 79 and described in Table 67.

Return to Summary Table.

Figure 79. TDR_SEG_DURATION1 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td>RESERVED</td><td colspan="5">TDR_SEG_DURATION_SEG3</td><td colspan="2">TDR_SEG_DURATION_SEG2</td></tr>
<tr><td>R-0x0</td><td colspan="5">R/W-0x14</td><td colspan="2">R/W-0x19</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="3">TDR_SEG_DURATION_SEG2</td><td colspan="5">TDR_SEG_DURATION_SEG1</td></tr>
<tr><td colspan="3">R/W-0x19</td><td colspan="5">R/W-0x6</td></tr>
</table>

Table 67. TDR_SEG_DURATION1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RESERVED	R	0x0	Reserved
14-10	TDR_SEG_DURATION_SEG3	R/W	0x14	Number of 125MHz clock cycles to run for segment #3
9-5	TDR_SEG_DURATION_SEG2	R/W	0x19	Number of 125MHz clock cycles to run for segment #2
4-0	TDR_SEG_DURATION_SEG1	R/W	0x6	Number of 125MHz clock cycles to run for segment #1

9.6.1.48 TDR_SEG_DURATION2 Register (Address = 0x183) [reset = 0xA01E]

TDR_SEG_DURATION2 is shown in Figure 80 and described in Table 68.

Return to Summary Table.

Figure 80. TDR_SEG_DURATION2 Register

15	14	13	12	11	10	9	8
TDR_SEG_DURATION_SEG5							
R/W-0xA0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED		TDR_SEG_DURATION_SEG4					
R-0x0		R/W-0x1E					

Table 68. TDR_SEG_DURATION2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_SEG_DURATION_SEG5	R/W	0xA0	Number of 125MHz clock cycles to run for segment #5
7-6	RESERVED	R	0x0	Reserved
5-0	TDR_SEG_DURATION_SEG4	R/W	0x1E	Number of 125MHz clock cycles to run for segment #4

9.6.1.49 TDR_GEN_CFG3 Register (Address = 0x184) [reset = 0xE976]

TDR_GEN_CFG3 is shown in Figure 81 and described in Table 69.

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Figure 81. TDR_GEN_CFG3 Register

15	14	13	12	11	10	9	8
TDR_FWD_SHADOW_SEG4				TDR_FWD_SHADOW_SEG3			
R/W-0xE				R/W-0x9			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	TDR_FWD_SHADOW_SEG2			RESERVED	TDR_FWD_SHADOW_SEG1		
R-0x0	R/W-0x7			R-0x0	R/W-0x6		

Table 69. TDR_GEN_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	TDR_FWD_SHADOW_SEG4	R/W	0xE	Indicates how much time to wait after max level before declaring we found a peak in segment #4
11-8	TDR_FWD_SHADOW_SEG3	R/W	0x9	Indicates how much time to wait after max level before declaring we found a peak in segment #3
7	RESERVED	R	0x0	Reserved

Table 69. TDR_GEN_CFG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	TDR_FWD_SHADOW_SEG2	R/W	0x7	Indicates how much time to wait after max level before declaring we found a peak in segment #2
3	RESERVED	R	0x0	Reserved
2-0	TDR_FWD_SHADOW_SEG1	R/W	0x6	Indicates how much time to wait after max level before declaring we found a peak in segment #1

9.6.1.50 TDR_GEN_CFG4 Register (Address = 0x185) [reset = 0x19CF]

TDR_GEN_CFG4 is shown in Figure 82 and described in Table 70.

Return to Summary Table.

Figure 82. TDR_GEN_CFG4 Register

15	14	13	12	11	10	9	8
RESERVED		TDR_SDW_AVG_LOC			RESERVED		TDR_TX_TYPE_SEG5
R-0x0		R/W-0x3			R-0x0		R/W-0x1
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDR_TX_TYPE_SEG4	TDR_TX_TYPE_SEG3	TDR_TX_TYPE_SEG2	TDR_TX_TYPE_SEG1	TDR_FWD_SHADOW_SEG5			
R/W-0x1	R/W-0x1	R/W-0x0	R/W-0x0	R/W-0xF			

Table 70. TDR_GEN_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-11	TDR_SDW_AVG_LOC	R/W	0x3	how much to look between segments to search average peak
10-9	RESERVED	R	0x0	Reserved
8	TDR_TX_TYPE_SEG5	R/W	0x1	the tx type (10/100) for this segment
7	TDR_TX_TYPE_SEG4	R/W	0x1	the tx type (10/100) for this segment
6	TDR_TX_TYPE_SEG3	R/W	0x1	the tx type (10/100) for this segment
5	TDR_TX_TYPE_SEG2	R/W	0x0	the tx type (10/100) for this segment
4	TDR_TX_TYPE_SEG1	R/W	0x0	the tx type (10/100) for this segment
3-0	TDR_FWD_SHADOW_SEG5	R/W	0xF	Indicates how much time to wait after max level before declaring we found a peak in segment #5

9.6.1.51 TDR_PEAKS_LOC_A_0_1 Register (Address = 0x190) [reset = 0x0]

TDR_PEAKS_LOC_A_0_1 is shown in Figure 83 and described in Table 71.

Return to Summary Table.

Figure 83. TDR_PEAKS_LOC_A_0_1 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_A_1							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDR_PEAKS_LOC_A_0							
R-0x0							

Table 71. TDR_PEAKS_LOC_A_0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_A_1	R	0x0	Found peak location 1 in channel A
7-0	TDR_PEAKS_LOC_A_0	R	0x0	Found peak location 0 in channel A

9.6.1.52 TDR_PEAKS_LOC_A_2_3 Register (Address = 0x191) [reset = 0x0]

TDR_PEAKS_LOC_A_2_3 is shown in Figure 84 and described in Table 72.

Return to Summary Table.

Figure 84. TDR_PEAKS_LOC_A_2_3 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_A_3							
R-0x0							
7	6	5	4	3	2	1	0
TDR_PEAKS_LOC_A_2							
R-0x0							

Table 72. TDR_PEAKS_LOC_A_2_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_A_3	R	0x0	Found peak location 3 in channel A
7-0	TDR_PEAKS_LOC_A_2	R	0x0	Found peak location 2 in channel A

9.6.1.53 TDR_PEAKS_LOC_A_4_B_0 Register (Address = 0x192) [reset = 0x0]

TDR_PEAKS_LOC_A_4_B_0 is shown in Figure 85 and described in Table 73.

Return to Summary Table.

Figure 85. TDR_PEAKS_LOC_A_4_B_0 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_B_0							
R-0x0							
7	6	5	4	3	2	1	0
TDR_PEAKS_LOC_A_4							
R-0x0							

Table 73. TDR_PEAKS_LOC_A_4_B_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_B_0	R	0x0	Found peak location 0 in channel B
7-0	TDR_PEAKS_LOC_A_4	R	0x0	Found peak location 4 in channel A

9.6.1.54 TDR_PEAKS_LOC_B_1_2 Register (Address = 0x193) [reset = 0x0]

TDR_PEAKS_LOC_B_1_2 is shown in Figure 86 and described in Table 74.

Return to Summary Table.

Figure 86. TDR_PEAKS_LOC_B_1_2 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_B_2							
R-0x0							

7	6	5	4	3	2	1	0
TDR_PEAKS_LOC_B_1							
R-0x0							

Table 74. TDR_PEAKS_LOC_B_1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_B_2	R	0x0	Found peak location 2 in channel B
7-0	TDR_PEAKS_LOC_B_1	R	0x0	Found peak location 1 in channel B

9.6.1.55 TDR_PEAKS_LOC_B_3_4 Register (Address = 0x194) [reset = 0x0]

TDR_PEAKS_LOC_B_3_4 is shown in Figure 87 and described in Table 75.

Return to Summary Table.

Figure 87. TDR_PEAKS_LOC_B_3_4 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_B_4							
R-0x0							
7	6	5	4	3	2	1	0
TDR_PEAKS_LOC_B_3							
R-0x0							

Table 75. TDR_PEAKS_LOC_B_3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_B_4	R	0x0	Found peak location 4 in channel B
7-0	TDR_PEAKS_LOC_B_3	R	0x0	Found peak location 3 in channel B

9.6.1.56 TDR_PEAKS_LOC_C_0_1 Register (Address = 0x195) [reset = 0x0]

TDR_PEAKS_LOC_C_0_1 is shown in Figure 88 and described in Table 76.

Return to Summary Table.

Figure 88. TDR_PEAKS_LOC_C_0_1 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_C_1							
R-0x0							
7	6	5	4	3	2	1	0
TDR_PEAKS_LOC_C_0							
R-0x0							

Table 76. TDR_PEAKS_LOC_C_0_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_C_1	R	0x0	Found peak location 1 in channel C
7-0	TDR_PEAKS_LOC_C_0	R	0x0	Found peak location 0 in channel C

9.6.1.57 TDR_PEAKS_LOC_C_2_3 Register (Address = 0x196) [reset = 0x0]

TDR_PEAKS_LOC_C_2_3 is shown in Figure 89 and described in Table 77.

Return to Summary Table.

Figure 89. TDR_PEAKS_LOC_C_2_3 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_C_3							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDR_PEAKS_LOC_C_2							
R-0x0							

Table 77. TDR_PEAKS_LOC_C_2_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_C_3	R	0x0	Found peak location 3 in channel C
7-0	TDR_PEAKS_LOC_C_2	R	0x0	Found peak location 2 in channel C

9.6.1.58 TDR_PEAKS_LOC_C_4_D_0 Register (Address = 0x197) [reset = 0x0]

TDR_PEAKS_LOC_C_4_D_0 is shown in Figure 90 and described in Table 78.

Return to Summary Table.

Figure 90. TDR_PEAKS_LOC_C_4_D_0 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_D_0							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDR_PEAKS_LOC_C_4							
R-0x0							

Table 78. TDR_PEAKS_LOC_C_4_D_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_D_0	R	0x0	Found peak location 0 in channel D
7-0	TDR_PEAKS_LOC_C_4	R	0x0	Found peak location 4 in channel C

9.6.1.59 TDR_PEAKS_LOC_D_1_2 Register (Address = 0x198) [reset = 0x0]

TDR_PEAKS_LOC_D_1_2 is shown in Figure 91 and described in Table 79.

Return to Summary Table.

Figure 91. TDR_PEAKS_LOC_D_1_2 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_D_2							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDR_PEAKS_LOC_D_1							
R-0x0							

Table 79. TDR_PEAKS_LOC_D_1_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_D_2	R	0x0	Found peak location 2 in channel D
7-0	TDR_PEAKS_LOC_D_1	R	0x0	Found peak location 1 in channel D

9.6.1.60 TDR_PEAKS_LOC_D_3_4 Register (Address = 0x199) [reset = 0x0]

TDR_PEAKS_LOC_D_3_4 is shown in Figure 92 and described in Table 80.

Return to Summary Table.

Figure 92. TDR_PEAKS_LOC_D_3_4 Register

15	14	13	12	11	10	9	8
TDR_PEAKS_LOC_D_4							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDR_PEAKS_LOC_D_3							
R-0x0							

Table 80. TDR_PEAKS_LOC_D_3_4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	TDR_PEAKS_LOC_D_4	R	0x0	Found peak location 4 in channel D
7-0	TDR_PEAKS_LOC_D_3	R	0x0	Found peak location 3 in channel D

9.6.1.61 TDR_GEN_STATUS Register (Address = 0x1A4) [reset = 0x0]

TDR_GEN_STATUS is shown in Figure 93 and described in Table 81.

Return to Summary Table.

Figure 93. TDR_GEN_STATUS Register

15	14	13	12	11	10	9	8
RESERVED				TDR_P_LOC_CROSS_MODE_D	TDR_P_LOC_CROSS_MODE_C	TDR_P_LOC_CROSS_MODE_B	TDR_P_LOC_CROSS_MODE_A
R-0x0				R-0x0	R-0x0	R-0x0	R-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDR_P_LOC_OVERFLOW_D	TDR_P_LOC_OVERFLOW_C	TDR_P_LOC_OVERFLOW_B	TDR_P_LOC_OVERFLOW_A	TDR_SEG1_HIGH_CROSS_D	TDR_SEG1_HIGH_CROSS_C	TDR_SEG1_HIGH_CROSS_B	TDR_SEG1_HIGH_CROSS_A
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 81. TDR_GEN_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R	0x0	Reserved
11	TDR_P_LOC_CROSS_MODE_D	R	0x0	Peak found at cross mode in channel D
10	TDR_P_LOC_CROSS_MODE_C	R	0x0	Peak found at cross mode in channel C
9	TDR_P_LOC_CROSS_MODE_B	R	0x0	Peak found at cross mode in channel B
8	TDR_P_LOC_CROSS_MODE_A	R	0x0	Peak found at cross mode in channel A
7	TDR_P_LOC_OVERFLOW_D	R	0x0	Total number of peaks in current segment reached max value of 5 in channel D
6	TDR_P_LOC_OVERFLOW_C	R	0x0	Total number of peaks in current segment reached max value of 5 in channel C
5	TDR_P_LOC_OVERFLOW_B	R	0x0	Total number of peaks in current segment reached max value of 5 in channel B
4	TDR_P_LOC_OVERFLOW_A	R	0x0	Total number of peaks in current segment reached max value of 5 in channel A

Table 81. TDR_GEN_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	TDR_SEG1_HIGH_CROSS_D	R	0x0	Peak crossed high threshold of segment #1 in channel D
2	TDR_SEG1_HIGH_CROSS_C	R	0x0	peak crossed high threshold of segment #1 in channel C
1	TDR_SEG1_HIGH_CROSS_B	R	0x0	peak crossed high threshold of segment #1 in channel B
0	TDR_SEG1_HIGH_CROSS_A	R	0x0	peak crossed high threshold of segment #1 in channel A

9.6.1.62 TDR_PEAKS_SIGN_A_B Register (Address = 0x1A5) [reset = 0x0]

TDR_PEAKS_SIGN_A_B is shown in Figure 94 and described in Table 82.

Return to Summary Table.

Figure 94. TDR_PEAKS_SIGN_A_B Register

15	14	13	12	11	10	9	8
RESERVED						TDR_PEAKS_SIGN_B_4	TDR_PEAKS_SIGN_B_3
R-0x0						R-0x0	R-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TDR_PEAKS_SIGN_B_2	TDR_PEAKS_SIGN_B_1	TDR_PEAKS_SIGN_B_0	TDR_PEAKS_SIGN_A_4	TDR_PEAKS_SIGN_A_3	TDR_PEAKS_SIGN_A_2	TDR_PEAKS_SIGN_A_1	TDR_PEAKS_SIGN_A_0
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 82. TDR_PEAKS_SIGN_A_B Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	TDR_PEAKS_SIGN_B_4	R	0x0	found peaks sign 4 in channel B
8	TDR_PEAKS_SIGN_B_3	R	0x0	found peaks sign 3 in channel B
7	TDR_PEAKS_SIGN_B_2	R	0x0	found peaks sign 2 in channel B
6	TDR_PEAKS_SIGN_B_1	R	0x0	found peaks sign 1 in channel B
5	TDR_PEAKS_SIGN_B_0	R	0x0	found peaks sign 0 in channel B
4	TDR_PEAKS_SIGN_A_4	R	0x0	found peaks sign 4 in channel A
3	TDR_PEAKS_SIGN_A_3	R	0x0	found peaks sign 3 in channel A
2	TDR_PEAKS_SIGN_A_2	R	0x0	found peaks sign 2 in channel A
1	TDR_PEAKS_SIGN_A_1	R	0x0	found peaks sign 1 in channel A
0	TDR_PEAKS_SIGN_A_0	R	0x0	found peaks sign 0 in channel A

9.6.1.63 TDR_PEAKS_SIGN_C_D Register (Address = 0x1A6) [reset = 0x0]

TDR_PEAKS_SIGN_C_D is shown in Figure 95 and described in Table 83.

Return to Summary Table.

Figure 95. TDR_PEAKS_SIGN_C_D Register

15	14	13	12	11	10	9	8
RESERVED						TDR_PEAKS_SIGN_D_4	TDR_PEAKS_SIGN_D_3
R-0x0						R-0x0	R-0x0

7	6	5	4	3	2	1	0
TDR_PEAKS_SIGN_D_2	TDR_PEAKS_SIGN_D_1	TDR_PEAKS_SIGN_D_0	TDR_PEAKS_SIGN_C_4	TDR_PEAKS_SIGN_C_3	TDR_PEAKS_SIGN_C_2	TDR_PEAKS_SIGN_C_1	TDR_PEAKS_SIGN_C_0
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 83. TDR_PEAKS_SIGN_C_D Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	TDR_PEAKS_SIGN_D_4	R	0x0	found peaks sign 4 in channel D
8	TDR_PEAKS_SIGN_D_3	R	0x0	found peaks sign 3 in channel D
7	TDR_PEAKS_SIGN_D_2	R	0x0	found peaks sign 2 in channel D
6	TDR_PEAKS_SIGN_D_1	R	0x0	found peaks sign 1 in channel D
5	TDR_PEAKS_SIGN_D_0	R	0x0	found peaks sign 0 in channel D
4	TDR_PEAKS_SIGN_C_4	R	0x0	found peaks sign 4 in channel C
3	TDR_PEAKS_SIGN_C_3	R	0x0	found peaks sign 3 in channel C
2	TDR_PEAKS_SIGN_C_2	R	0x0	found peaks sign 2 in channel C
1	TDR_PEAKS_SIGN_C_1	R	0x0	found peaks sign 1 in channel C
0	TDR_PEAKS_SIGN_C_0	R	0x0	found peaks sign 0 in channel C

9.6.1.64 OP_MODE_DECODE Register (Address = 0x1DF) [reset = 0x40]

OP_MODE_DECODE is shown in Figure 96 and described in Table 84.

Return to Summary Table.

Figure 96. OP_MODE_DECODE Register

15	14	13	12	11	10	9	8
RESERVED							RESERVED
R-0x0							R-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESERVED	BRIDGE_MODE_RGMII_MAC	RGMII_MII_SEL	RESERVED	RESERVED	CFG_OPMODE		
R-0x0	R/W-0x1	R/W-0x0	R-0x0	R-0x0	R/W-0x0		

Table 84. OP_MODE_DECODE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-9	RESERVED	R	0x0	Reserved
8-7	RESERVED	R	0x0	Reserved
6	BRIDGE_MODE_RGMII_MAC	R/W	0x1	0x0 = RGMII to SGMII Bridge 0x1 = SGMII to RGMII Bridge
5	RGMII_MII_SEL	R/W	0x0	0x0 = RGMII 0x1 = MII
4	RESERVED	R	0x0	Reserved
3	RESERVED	R	0x0	Reserved

Table 84. OP_MODE_DECODE Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	CFG_OPMODE	R/W	0x0	Operation Mode 0x0 = RGMII to Copper 0x1 = RGMII to 1000Base-X 0x2 = RGMII to 100Base-FX 0x3 = RGMII to SGMII 0x4 = 1000Base-T to 1000Base-X 0x5 = 100Base-T to 100Base-FX 0x6 = SGMII to Copper 0x7 = Reserved

9.6.1.65 GPIO_MUX_CTRL Register (Address = 0x1E0) [reset = 0x417A]

GPIO_MUX_CTRL is shown in Figure 97 and described in Table 85.

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Figure 97. GPIO_MUX_CTRL Register

15	14	13	12	11	10	9	8
RESERVED				RESERVED			
R/W-0x4				R/W-0x1			
7	6	5	4	3	2	1	0
JTAG_TDO_GPIO_1_CTRL				LED_2_GPIO_0_CTRL			
R/W-0x7				R/W-0xA			

Table 85. GPIO_MUX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x4	Reserved
11-8	RESERVED	R/W	0x1	Reserved
7-4	JTAG_TDO_GPIO_1_CTRL	R/W	0x7	See bits [3:0] for GPIO control options. If either type of SFD is enabled, this pin will be automatically configured to TX_SFD.
3-0	LED_2_GPIO_0_CTRL	R/W	0xA	Following options are available for GPIO control. If either type of SFD is enabled, this pin will be automatically configured to RX_SFD. 0x0 = CLK_OUT 0x1 = RESERVED 0x2 = INT 0x3 = Link status 0x4 = RESERVED 0x5 = Transmit SFD 0x6 = Receive SFD 0x7 = WOL 0x8 = Energy detect(1000Base-T and 100Base-TX only) 0x9 = PRBS errors 0xA = LED_2 0xB = LED_GPIO(3) 0xC = CRS 0xD = COL 0xE = constant '0' 0xF = constant '1'

9.6.1.66 FX_CTRL Register (Address = 0xC00) [reset = 0x1140]

FX_CTRL is shown in Figure 98 and described in Table 86.

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Registers after 0xC00 are common for Fiber, SGMII IP blocks for RGMII-to-SGMII, SGMII-to-RGMII, and Media Convertor.

Figure 98. FX_CTRL Register

15	14	13	12	11	10	9	8
CTRL0_RESET	CTRL0_LOOPBACK	CTRL0_SPEED_SEL_LSB	CTRL0_ANEG_EN	CTRL0_PWRDN	CTRL0_ISOLATE	CTRL0_RESTART_AN	CTRL0_DUPLEX_MODE
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1

7	6	5	4	3	2	1	0
CTRL0_COL_TEST	CTRL0_SPEED_SEL_MSB	RESERVED					
R/W-0x0	R/W-0x1	R/W-0x0					

Table 86. FX_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CTRL0_RESET	R/W	0x0	Controls reset in Fiber mode. This bit is automatically cleared after reset is completed. 0x0 = Normal Operation 0x1 = Reset.
14	CTRL0_LOOPBACK	R/W	0x0	100BASE-X, 1000BASE-FX and RGMII-SGMII, SGMII-RGMII MAC loopback. 0x0 = Disable MAC loopback 0x1 = Enable MAC Loopback
13	CTRL0_SPEED_SEL_LSB	R/W	0x0	Speed selection bits LSB[13] and MSB[6] are used to control the data rate of the ethernet link when in Fiber Ethernet mode. These bits are also affected by straps. 0x0 = 10Mbps 0x1 = 100Mbps 0x2 = 1000Mbps 0x3 = Reserved
12	CTRL0_ANEG_EN	R/W	0x1	Enable 1000BASE-X, R2S, S2R Bridge mode Auto-negotiation. Controlled by strap. 0x0 = Disable 0x1 = Enable
11	CTRL0_PWRDN	R/W	0x0	Power Down SGMII for R2S, S2R, 1000BX, 100FX. Digital is in reset. 0x0 = Normal operation 0x1 = Power Down
10	CTRL0_ISOLATE	R/W	0x0	Isolate MAC interface. Used in 1000BX, 100FX and RGMII-SGMII mode. N/A in SGMII-RGMII mode. 0x0 = Normal operation 0x1 = Isolate
9	CTRL0_RESTART_AN	R/W	0x0	Writing 1 to this control bit restarts Autoneg in SGMII and 1000B-X mode. It is self-cleared by hardware. 0x0 = Normal operation 0x1 = Restart 1000BASE-X/SGMII Auto-Negotiation Process

Table 86. FX_CTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8	CTRL0_DUPLEX_MODE	R/W	0x1	Forced Duplex mode. Applicable only in MII-100FX mode. 0x0 = Half duplex mode 0x1 = Full duplex mode
7	CTRL0_COL_TEST	R/W	0x0	Used to test collision functionality. Settings this bit asserts collision on just asserting tx_en
6	CTRL0_SPEED_SEL_MSB	R/W	0x1	Forced Speed for SGMII only when Autoneg is disabled. Controlled by straps. See bit 13 of this register.
5-0	RESERVED	R/W	0x0	Reserved

9.6.1.67 FX_STS Register (Address = 0xC01) [reset = 0x6149]

FX_STS is shown in Figure 99 and described in Table 87.

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Figure 99. FX_STS Register

15	14	13	12	11	10	9	8
STTS_100B_T4	STTS_100B_X_FD	STTS_100B_X_HD	STTS_10B_FD	STTS_10B_HD	STTS_100B_T2_FD	STTS_100B_T2_HD	STTS_EXTENDED_STATUS
R-0x0	R-0x1	R-0x1	R-0x0	R-0x0	R-0x0	R-0x0	R-0x1
7	6	5	4	3	2	1	0
RESERVED	STTS_MF_PREAMBLE_SUPRSN	STTS_ANEG_COMPLETE	STTS_REMOTE_FAULT	STTS_ANEG_ABILITY	STTS_LINK_STATUS	STTS_JABBER_DET	STTS_EXTENDED_CAPABILITY
R-0x0	R-0x1	R-0x0	R-0x0	R-0x1	R-0x0	R-0x0	R-0x1

Table 87. FX_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	STTS_100B_T4	R	0x0	Return Always 0. Device doesn 't support 100BASE-T4 mode
14	STTS_100B_X_FD	R	0x1	Return Always 1. Device supports 100BASE-FX Full-Duplex
13	STTS_100B_X_HD	R	0x1	Return Always 1. Device supports 100BASE-FX Half-Duplex
12	STTS_10B_FD	R	0x0	Return Always 0. Device doesn 't support 10Mbps fiber mode
11	STTS_10B_HD	R	0x0	Return Always 0. Device doesn 't support 10Mbps fiber mode
10	STTS_100B_T2_FD	R	0x0	Return Always 0. Device doesn 't support 100BASE-T2 mode
9	STTS_100B_T2_HD	R	0x0	Return Always 0. Device doesn 't support 100BASE-T2 mode
8	STTS_EXTENDED_STATUS	R	0x1	Return Always 1. Extended status information in register15
7	RESERVED	R	0x0	Reserved
6	STTS_MF_PREAMBLE_SUPRSN	R	0x1	Return Always 1. Phy accepts management frames with preamble suppressed.
5	STTS_ANEG_COMPLETE	R	0x0	1: Auto negotiation process complete 0:Auto negotiation process not complete
4	STTS_REMOTE_FAULT	R	0x0	1: Remote fault condition detected 0:Remote fault condition not detected
3	STTS_ANEG_ABILITY	R	0x1	Return Always 1. Device capable of performing Auto-Negotiation

Table 87. FX_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	STTS_LINK_STATUS	R	0x0	1: link-up 0: link down Indicates 100FX link-up in 100FX and 100FX MC Mode. Indicates 1000X link-up in 1000X and 1000X MC mode. In RGMII-SGMII mode, it indicates SGMII link-up and LP link up if Autoneg is enabled else(if autoneg disabled) it indicates SGMII link-up. In SGMII-RGMII mode, it indicates LP link-up
1	STTS_JABBER_DET	R	0x0	Return 0.
0	STTS_EXTENDED_CAPABILITY	R	0x1	Return Always 1. Device supports Extended register capabilities

9.6.1.68 FX_PHYID1 Register (Address = 0xC02) [reset = 0x2000]

FX_PHYID1 is shown in Figure 100 and described in Table 88.

Return to Summary Table.

Figure 100. FX_PHYID1 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="2">RESERVED</td><td colspan="6">OUI_6_19_FIBER</td></tr>
<tr><td colspan="2">R-0x0</td><td colspan="6">R-0x2000</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">OUI_6_19_FIBER</td></tr>
<tr><td colspan="8">R-0x2000</td></tr>
</table>

Table 88. FX_PHYID1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R	0x0	Reserved
13-0	OUI_6_19_FIBER	R	0x2000	Organizationally Unique Identifier Bits 19:6

9.6.1.69 FX_PHYID2 Register (Address = 0xC03) [reset = 0xA0F1]

FX_PHYID2 is shown in Figure 101 and described in Table 89.

Return to Summary Table.

Figure 101. FX_PHYID2 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="6">OUI_0_5_FIBER</td><td colspan="2">MODEL_NUM_FIBER</td></tr>
<tr><td colspan="6">R-0x28</td><td colspan="2">R-0xF</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">MODEL_NUM_FIBER</td><td colspan="4">REVISION_NUM_FIBER</td></tr>
<tr><td colspan="4">R-0xF</td><td colspan="4">R-0x1</td></tr>
</table>

Table 89. FX_PHYID2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	OUI_0_5_FIBER	R	0x28	Organizationally Unique Identifier Bits 5:0
9-4	MODEL_NUM_FIBER	R	0xF	model number
3-0	REVISION_NUM_FIBER	R	0x1	revision number

9.6.1.70 FX_ANADV Register (Address = 0xC04) [reset = 0x20]

FX_ANADV is shown in Figure 102 and described in Table 90.

Return to Summary Table.

Figure 102. FX_ANADV Register

15	14	13	12	11	10	9	8
BP_NEXT_PAGE	BP_ACK	BP_REMOTE_FAULT		RESERVED			BP_ASYMMETRIC_PAUSE
R/W-0x0	R-0x0	R/W-0x0		R-0x0			R/W-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BP_PAUSE	BP_HALF_DUPLEX	BP_FULL_DUPLEX	BP_RSVD1				
R/W-0x0	R/W-0x0	R/W-0x1	R-0x0				

Table 90. FX_ANADV Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BP_NEXT_PAGE	R/W	0x0	Set this bit if next page needs to be advertised. 1 = Advertise 0 = Not advertised
14	BP_ACK	R	0x0	Always return 0
13-12	BP_REMOTE_FAULT	R/W	0x0	00 = LINK_OK 01=OFFLINE 10=LINK_FAILURE 11=AUTO_ERROR
11-9	RESERVED	R	0x0	Reserved
8	BP_ASYMMETRIC_PAUSE	R/W	0x0	1 = Asymmetric Pause 0 = No asymmetric Pause
7	BP_PAUSE	R/W	0x0	1 = MAC PAUSE 0 = No MAC PAUSE
6	BP_HALF_DUPLEX	R/W	0x0	1 = Advertise 0 = Not advertised
5	BP_FULL_DUPLEX	R/W	0x1	1 = Advertise 0 = Not advertised
4-0	BP_RSVD1	R	0x0	Reserved. Set to 00000

9.6.1.71 FX_LPABL Register (Address = 0xC05) [reset = 0x0]

FX_LPABL is shown in Figure 103 and described in Table 91.

Return to Summary Table.

Figure 103. FX_LPABL Register

15	14	13	12	11	10	9	8
LP_ABILITY_NEXT_PAGE	LP_ABILITY_ACK	LP_ABILITY_REMOTE_FAULT		RESERVED			LP_ABILITY_ASYMMETRIC_PAUSE
R-0x0	R-0x0	R-0x0		R-0x0			R-0x0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LP_ABILITY_PAUSE	LP_ABILITY_HALF_DUPLEX	LP_ABILITY_FULL_DUPLEX	RESERVED				
R-0x0	R-0x0	R-0x0	R-0x0				

Table 91. FX_LPABL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LP_ABILITY_NEXT_PAGE	R	0x0	0x0 = LP is not capable of next page 0x1 = LP is capable of next page

Table 91. FX_LPABL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14	LP_ABILITY_ACK	R	0x0	0x0 = LP has not acknowledged that it has received link code word 0x1 = LP acknowledges that it has received link code word
13-12	LP_ABILITY_REMOTE_FAULT	R	0x0	Received Remote fault from LP. 0x0 = LINK_OK 0x1 = OFFLINE 0x2 = LINK_FAILURE 0x3 = AUTO_ERROR
11-9	RESERVED	R	0x0	Reserved
8	LP_ABILITY_ASYMMETRIC_PAUSE	R	0x0	0x0 = LP does not request asymmetric pause 0x1 = LP requests of asymmetric pause
7	LP_ABILITY_PAUSE	R	0x0	0x0 = LP is not capable of pause operation 0x1 = LP is capable of pause operation
6	LP_ABILITY_HALF_DUPLEX	R	0x0	0x0 = LP is not 1000BASE-X Half-duplex capable 0x1 = LP is 1000BASE-X Half-duplex capable
5	LP_ABILITY_FULL_DUPLEX	R	0x0	0x0 = LP is not 1000BASE-X Full-duplex capable 0x1 = LP is 1000BASE-X Full-duplex capable
4-0	RESERVED	R	0x0	Reserved

9.6.1.72 FX_ANEXP Register (Address = 0xC06) [reset = 0x0]

FX_ANEXP is shown in Figure 104 and described in Table 92.

Return to Summary Table.

Figure 104. FX_ANEXP Register

15	14	13	12	11	10	9	8
RESERVED							
R-0x0							
7	6	5	4	3	2	1	0
RESERVED				AN_EXP_LP_NEXT_PAGE_ABLE	AN_EXP_LOCAL_NEXT_PAGE_ABLE	AN_EXP_PAGE_RECEIVED	AN_EXP_LP_AUTO_NEG_ABLE
R-0x0				R-0x0	R-0x0	R-0x0	R-0x0

Table 92. FX_ANEXP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0x0	Reserved
3	AN_EXP_LP_NEXT_PAGE_ABLE	R	0x0	1: Link partner is Next page able 0: Link partner is not next page able Bit is set to 1 when device receives base page with NP bit (bit 15) set to 1. It is cleared when Autoneg state goes to AN_ENABLE. It is expected that NP bit will be set to 0 in SGMII mode as SGMII doesn 't supports next page.
2	AN_EXP_LOCAL_NEXT_PAGE_ABLE	R	0x0	1 : Local device is next page able 0 : Local device is not next page able This bit is set to 1 in fiber 1000BASE-X mode. it is set to 0 in SGMII mode.

Table 92. FX_ANEXP Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	AN_EXP_PAGE_RECEIVED	R	0x0	1 : A new page(base page or next page) has been received 0 : No new page has been received Status is latched when new page is received by the device. It is cleared when SW reads this register.
0	AN_EXP_LP_AUTO_NEG_ABLE	R	0x0	1: Link partner is auto negotiation able 0: Link partner is not auto negotiation able Bit is set to 1 when device receives base page. It is cleared when Autoneg state goes to AN_ENABLE.

9.6.1.73 FX_LOCNP Register (Address = 0xC07) [reset = 0x2001]

FX_LOCNP is shown in Figure 105 and described in Table 93.

Return to Summary Table.

Figure 105. FX_LOCNP Register

15	14	13	12	11	10	9	8
NP_TX_NEXT_PAGE	RESERVED	NP_TX_MESSAGE_PAGE_MODE	NP_TX_ACK_2	NP_TX_TOGGLE	NP_TX_MESSAGE_FIELD		
R/W-0x0	R-0x0	R/W-0x1	R/W-0x0	R-0x0	R/W-0x1		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NP_TX_MESSAGE_FIELD							
R/W-0x1							

Table 93. FX_LOCNP Register Field Descriptions

Bit	Field	Type	Reset	Description
15	NP_TX_NEXT_PAGE	R/W	0x0	0: if last page 1: if there is more pages to transmit
14	RESERVED	R	0x0	Reserved
13	NP_TX_MESSAGE_PAGE_MODE	R/W	0x1	0: unformatted page 1: message page
12	NP_TX_ACK_2	R/W	0x0	device has the ability to comply with the message 0: cannot comply with message. 1: comply with message.
11	NP_TX_TOGGLE	R	0x0	0: previous value of the transmitted link codeword equalled logic one. 1: previous value of the transmitted link codeword equalled logic zero
10-0	NP_TX_MESSAGE_FIELD	R/W	0x1	Message code field as defined in IEEE Annex 28C

9.6.1.74 FX_LPNP Register (Address = 0xC08) [reset = 0x0]

FX_LPNP is shown in Figure 106 and described in Table 94.

Return to Summary Table.

Figure 106. FX_LPNP Register

15	14	13	12	11	10	9	8
LP_NP_NEXT_PAGE	LP_NP_ACK	LP_NP_MESSAGE_PAGE_MODE	LP_NP_ACK_2	LP_NP_TOGGLE	LP_NP_MESSAGE_FIELD		
R-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x0		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
LP_NP_MESSAGE_FIELD							
R-0x0							

Table 94. FX_LPNP Register Field Descriptions

Bit	Field	Type	Reset	Description
15	LP_NP_NEXT_PAGE	R	0x0	LP last page 0: if last page 1: if there is more pages to transmit
14	LP_NP_ACK	R	0x0	Reserved
13	LP_NP_MESSAGE_PAGE_MODE	R	0x0	LP message page mode 0: unformatted page 1: message page
12	LP_NP_ACK_2	R	0x0	LP has the ability to comply with the message 0: cannot comply with message. 1: comply with message.
11	LP_NP_TOGGLE	R	0x0	LP Toggle bit 0: previous value of the transmitted link codeword equalled logic one. 1: previous value of the transmitted link codeword equalled logic zero
10-0	LP_NP_MESSAGE_FIELD	R	0x0	LP Message code field as defined in IEEE Annex 28C

9.6.1.75 FX_INT_EN Register (Address = 0xC18) [reset = 0x3FF]

FX_INT_EN is shown in Figure 107 and described in Table 95.

Return to Summary Table.

Figure 107. FX_INT_EN Register

15	14	13	12	11	10	9	8
RESERVED						FEF_FAULT_EN	TX_FIFO_FULL_EN
R-0x0						R/W-0x1	R/W-0x1

7	6	5	4	3	2	1	0
TX_FIFO_EMPTY_EN	RX_FIFO_FULL_EN	RX_FIFO_EMPTY_EN	LINK_STS_CHANGE_EN	LP_FAULT_RX_EN	PRI_RES_FAIL_EN	LP_NP_RX_EN	LP_BP_RX_EN
R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1

Table 95. FX_INT_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	FEF_FAULT_EN	R/W	0x1	FEF fault received interrupt enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt
8	TX_FIFO_FULL_EN	R/W	0x1	Fiber and SGMII Tx FIFO full interrupt enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt
7	TX_FIFO_EMPTY_EN	R/W	0x1	Fiber and SGMII Tx FIFO empty interrupt enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt
6	RX_FIFO_FULL_EN	R/W	0x1	Fiber and SGMII Rx FIFO full interrupt enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt
5	RX_FIFO_EMPTY_EN	R/W	0x1	Fiber and SGMII Rx FIFO empty interrupt enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt

Table 95. FX_INT_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	LINK_STS_CHANGE_EN	R/W	0x1	Link Status Change Interrupt Enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt
3	LP_FAULT_RX_EN	R/W	0x1	Link Partner Remote Fault Interrupt Enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt
2	PRI_RES_FAIL_EN	R/W	0x1	Priority Resolution Fail Interrupt Enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt
1	LP_NP_RX_EN	R/W	0x1	Link Partner Next Page Received Interrupt Enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt
0	LP_BP_RX_EN	R/W	0x1	Link Partner Base Page Received Interrupt Enable 0x0 = Disable Interrupt 0x1 = Enable Interrupt

9.6.1.76 FX_INT_STS Register (Address = 0xC19) [reset = 0x0]

FX_INT_STS is shown in Figure 108 and described in Table 96.

Return to Summary Table.

Figure 108. FX_INT_STS Register

15	14	13	12	11	10	9	8
RESERVED						FEF_FAULT	TX_FIFO_FULL
R-0x0						RC-0x0	RC-0x0

7	6	5	4	3	2	1	0
TX_FIFO_EMPTY	RX_FIFO_FULL	RX_FIFO_EMPTY	LINK_STS_CHANGE	LP_FAULT_RX	PRI_RES_FAIL	LP_NP_RX	LP_BP_RX
RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0	RC-0x0

Table 96. FX_INT_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	FEF_FAULT	RC	0x0	FEF fault received interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read
8	TX_FIFO_FULL	RC	0x0	Fiber Tx FIFO full interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read
7	TX_FIFO_EMPTY	RC	0x0	Fiber Tx FIFO empty interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read
6	RX_FIFO_FULL	RC	0x0	Fiber Rx FIFO full interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read

Table 96. FX_INT_STS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	RX_FIFO_EMPTY	RC	0x0	Fiber Rx FIFO empty interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read
4	LINK_STS_CHANGE	RC	0x0	Link Status Change Interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read
3	LP_FAULT_RX	RC	0x0	Link Partner Remote Fault Interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read
2	PRI_RES_FAIL	RC	0x0	Priority Resolution Fail Interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read
1	LP_NP_RX	RC	0x0	Link Partner Next Page Received Interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read
0	LP_BP_RX	RC	0x0	Link Partner Base Page Received Interrupt 0x0 = No Interrupt pending 0x1 = Interrupt pending, cleared on read

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The DP83869HM is a 10/100/1000 Copper and Fiber Ethernet PHY. It supports connections to an Ethernet MAC through SGMII or RGMII. MII is also supported but only for 100M and 10M speeds. For MII to be operate correctly, 1000M advertisement should be disabled. SGMII is not available in Fiber Ethernet mode and Media Convertor mode because the SGMII pins are multipurpose pins which carry Fiber Ethernet signals. Connections to the Ethernet media are made through the IEEE 802.3 defined Media Dependent Interface.

When using the device for Ethernet application, it is necessary to meet certain requirements for normal operation of the device. The following typical application and design requirements can be used for selecting appropriate component values for the DP83869.

10.2 Typical Applications

10.2.1 Copper Ethernet Typical Application

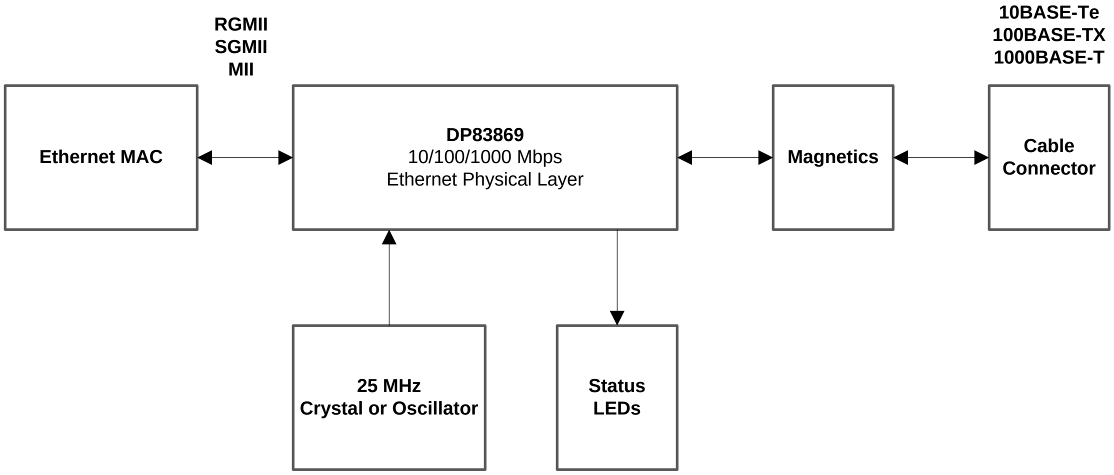


图 109. Typical Copper Ethernet Application

10.2.1.1 Design Requirements

The design requirements for the DP83869HM are:

- VDDA2P5 = 2.5 V
- VDD1P1 = 1.1 V
- VDDIO = 3.3 V, 2.5 V, or 1.8 V
- VDDA1P8_x = 1.8 V (optional)
- Clock Input = 25 MHz

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Clock Input

Input reference clock requirements are same in all functional modes.

Typical Applications (接下页)

10.2.1.2.1.1 Crystal Recommendations

A 25-MHz, parallel, 15-pF to 40-pF load crystal resonator should be used if a crystal source is desired. 图 110 shows a typical connection for a crystal resonator circuit. The load capacitor values vary with the crystal vendors. Check with the vendor for the recommended loads.

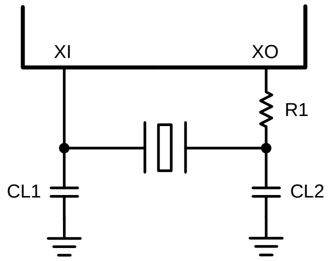


图 110. Crystal Oscillator Circuit

As a starting point for evaluating the oscillator performance, the value of CL1 and CL2 should each be equal to 2x the specified load capacitance from the crystal vendor’s data sheet. For example, if the specified load capacitance of the crystal is 10 pF, set CL1 = CL2 = 20 pF. CL1, CL2 value may need to be adjusted based on the parasitic capacitance. Depending on the crystal drive level, R1 may or may not be needed.

Specification for 25-MHz crystal are listed in 表 97.

表 97. 25-MHz Crystal Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability				±50	ppm
Load Capacitance		15		40	pF
ESR				50	ohm

10.2.1.2.1.2 External Clock Source Recommendation

If an external clock oscillator is used, then it should be directly connected to XI. XO should be left floating.

The CMOS 25-MHz oscillator specifications are listed in 表 98.

表 98. 25-MHz Oscillator Specifications

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm
Rise / Fall Time	20% - 80%			5	ns
Symmetry	Duty Cycle	40%		60%	

10.2.1.2.2 Magnetics Requirements

In applications where copper Ethernet interface is used, magnetic isolation is required. Magnetics can be discrete or integrated in the Ethernet cable connector. The DP83869HM will operate with discrete and integrate magnetics if they meet the electrical specifications listed in 表 99.

表 99. Magnetics Electrical Specification

PARAMETER	TEST CONDITIONS	TYP	UNIT
Turns Ratio	±2% Tolerance	1:1	-
Insertion Loss	1-100 MHz	-1	dB
Return Loss	1-30 MHz	-16	dB
	30-60 MHz	-12	dB
	60-80 MHz	-10	dB
Differential to Common Mode Rejection	1-50 MHz	-30	dB
	60-150 MHz	-20	dB
Crosstalk	30 MHz	-35	dB
	60 MHz	-30	dB
Open Circuit Inductance	8-mA DC Bias	350	µH
Isolation	HPOT	1500	Vrms

10.2.1.2.2.1 Magnetics Connection

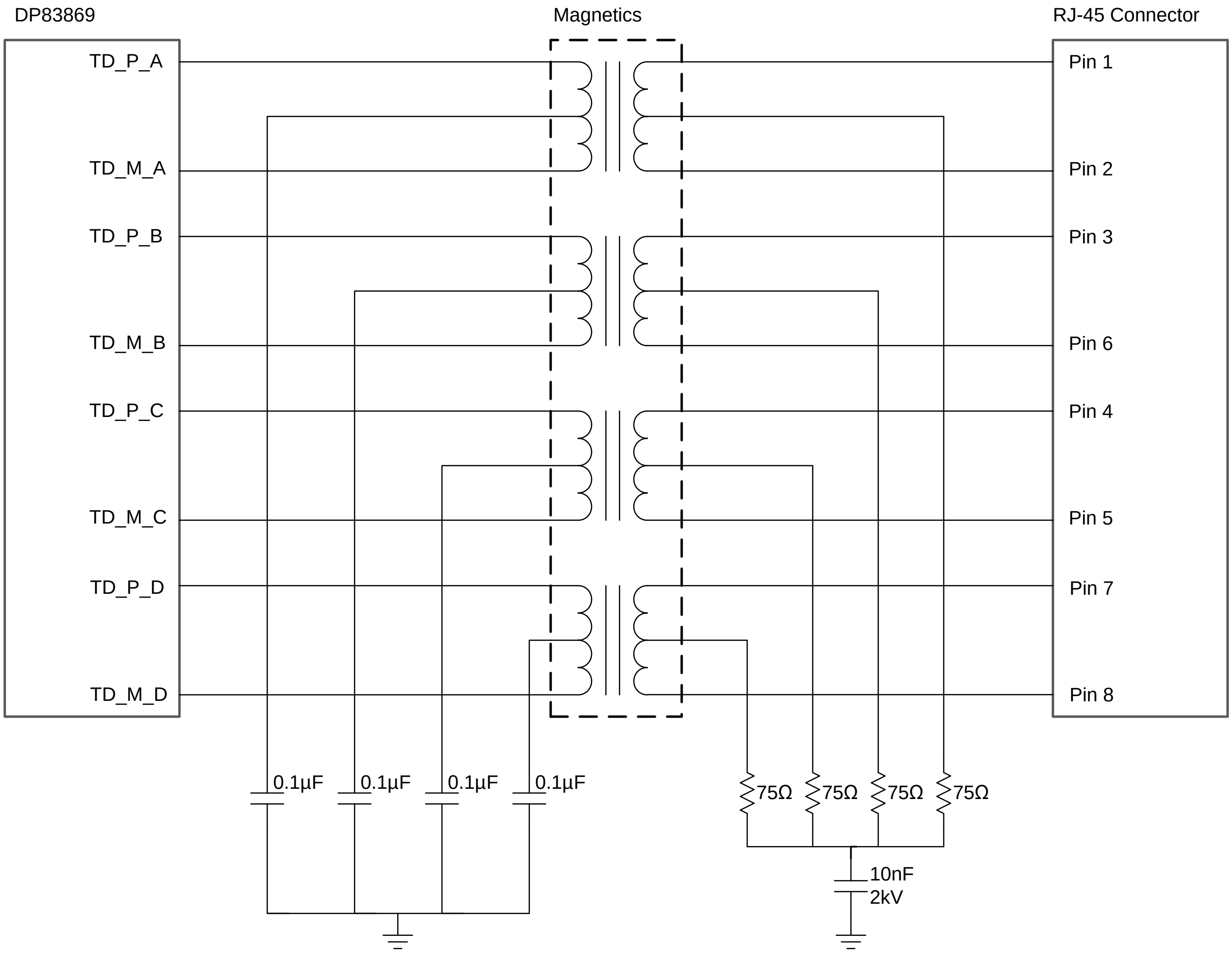


图 111. PHY to RJ45 and Magnetics

10.2.1.3 Application Curves

For expected MDI signal, see 表 100.

表 100. Table of Graphs

NAME	FIGURE
1000Base-T Signal	图 12
100Base-TX Signal	图 13
10Base-Te Link Pulse	图 14
Auto-Negotiation FLP	图 15

10.2.2 Fiber Ethernet Typical Ethernet

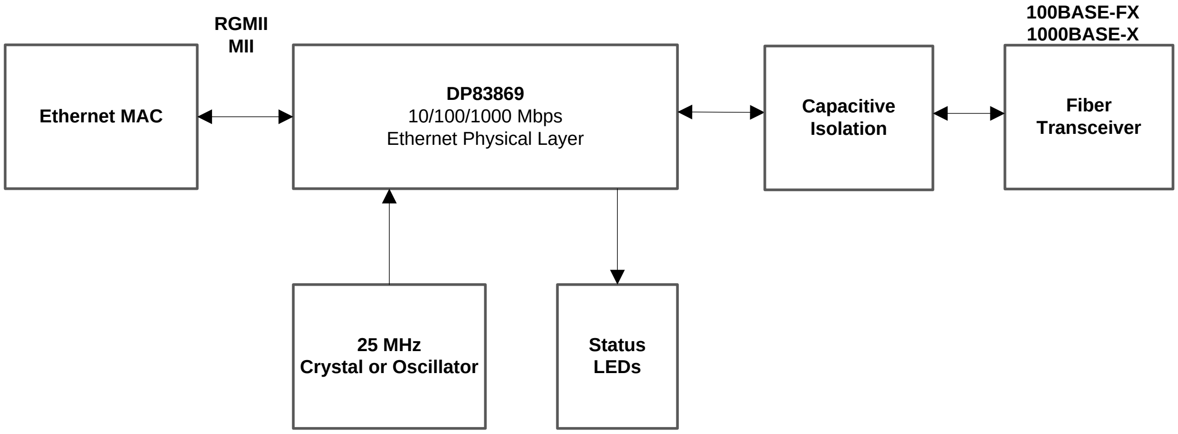


图 112. Typical Fiber Ethernet Application

10.2.2.1 Design Requirements

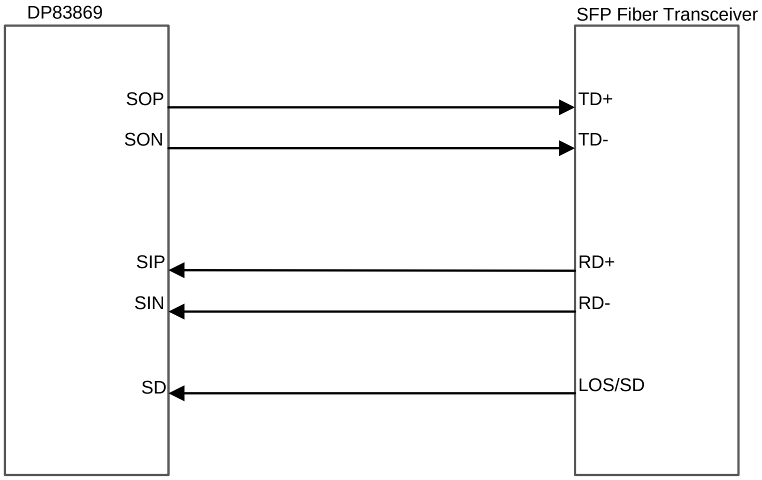
The design requirements for the DP83869HM are:

- VDDA2P5 = 2.5 V
- VDD1P1 = 1.1 V
- VDDIO = 3.3 V, 2.5 V, or 1.8 V
- VDDA1P8_x = 1.8 V (optional)
- Clock Input = 25 MHz

10.2.2.2 Detailed Design Procedure

See *Detailed Design Procedure* for more information.

10.2.2.2.1 Transceiver Connections



SFP Fiber Transceiver usually have integrated AC coupling capacitors. Adding external capacitors may not be needed.

图 113. PHY to Fiber Transceiver Connections

10.2.2.3 Application Curves

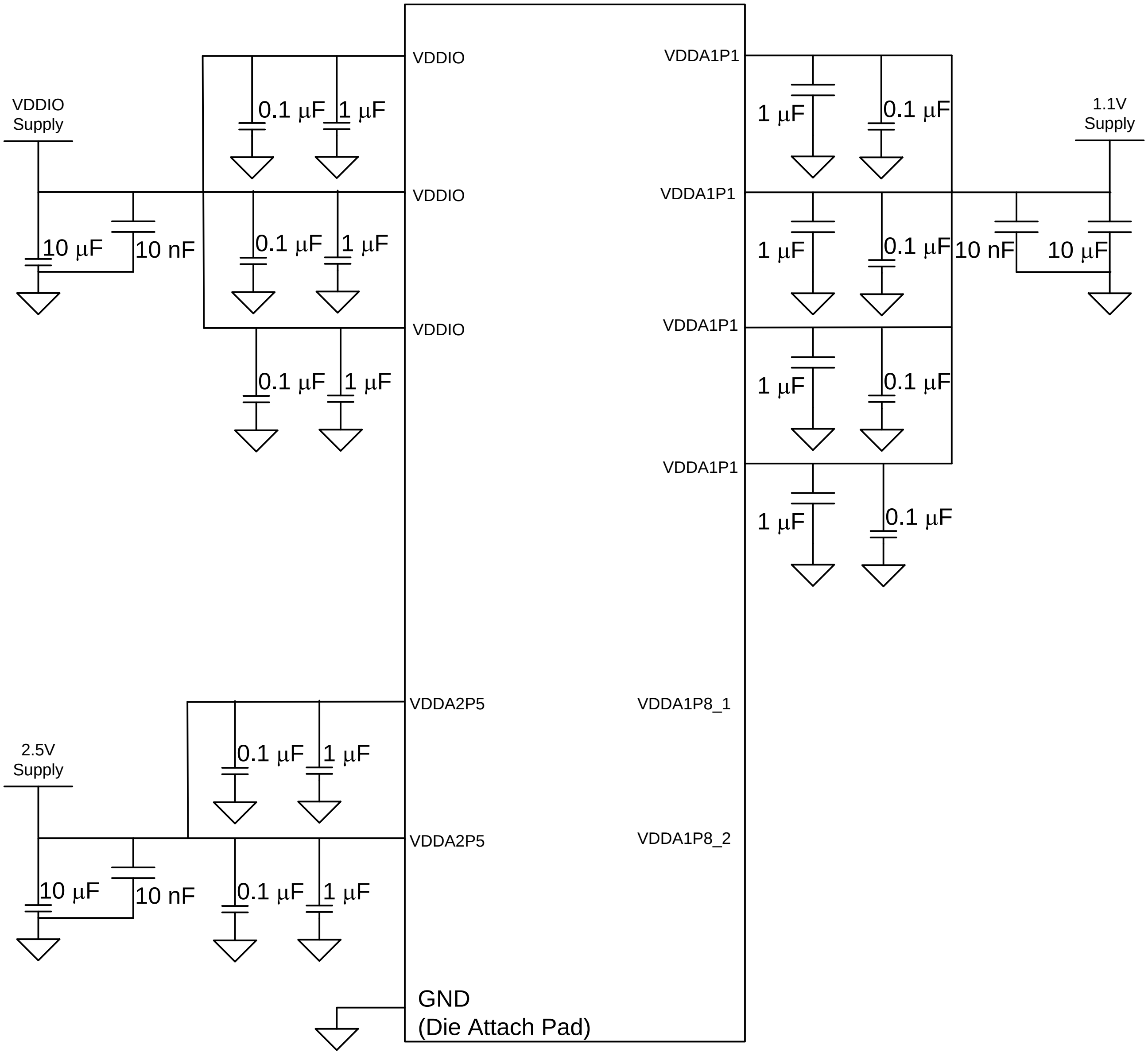
For expected MDI signal, see 表 100 in the *Application Curves* section.

11 Power Supply Recommendations

The DP83869HM is capable of operating with as few as two or three supplies. The I/O power supply can also be operated independently of the main device power supplies to provide flexibility for the MAC interface. There are two possible supply configuration that can be used: Two Supply and Three Supply. In Two Supply Configuration, no power rail is connected to VDDA1P8_x pins (pin 13, 48). When unused, pin 13 and 48 should be left floating with no components attached to them.

11.1 Two Supply Configuration

The connection diagrams for the two-supply is shown below.



For two supply configuration, both VDDA1P8 pins must be left unconnected.

Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins.

VDDIO may be 3.3 V or 2.5 V or 1.8 V.

No Components should be connected to VDDA1P8 pins in Two-Supply Configuration.

图 114. Two-Supply Configuration

Two Supply Configuration (接下页)

For two supply configuration, the recommendation is to power all supplies together. If that is not possible then the following power sequencing needs to be used.

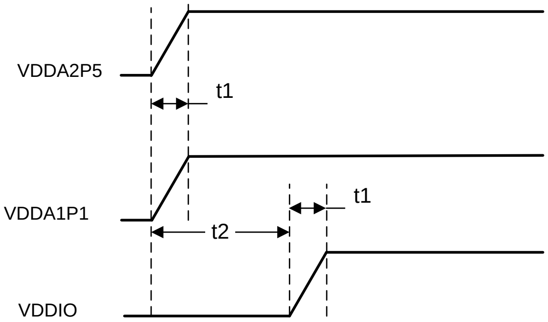


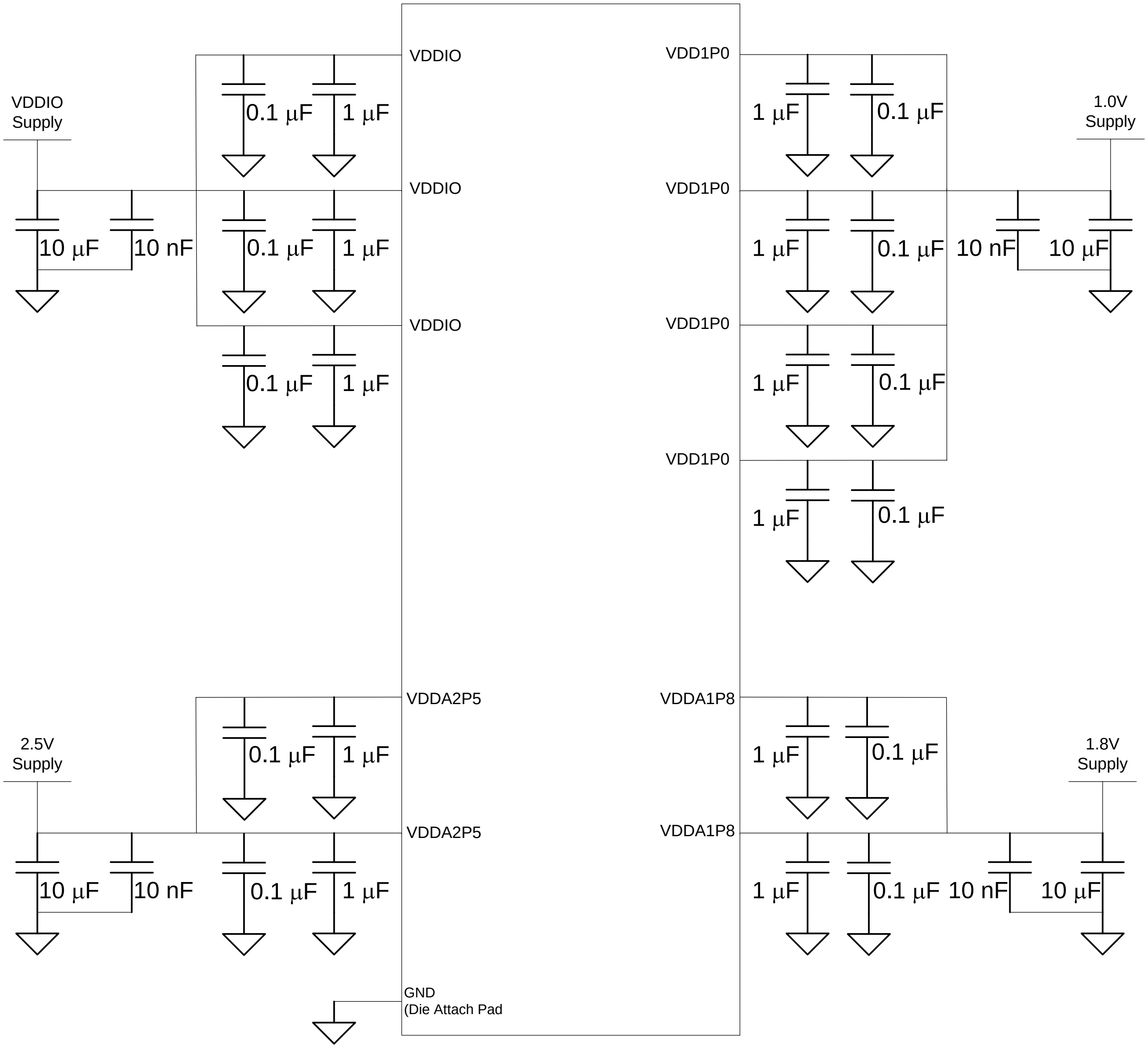
图 115. Two Supply Sequence Diagram

表 101. Two Supply Sequence

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t1	Supply ramp time	Applicable to all supplies	0.5		100	ms
t2	Time instance at which VDDIO starts up	Measured with respect to start of VDDA2P5 and VDDA1P1			50	ms

11.2 Three Supply Configuration

The connection diagrams for the three supply is shown below.



Place 1-µF and 0.1-µF decoupling capacitors as close as possible to component VDD pins.

Note: VDDIO may be 3.3 V or 2.5 V or 1.8 V.

图 116. Three-Supply Configuration

For three supply configuration, the recommendation is to power all supplies together. If that is not possible then the following power sequencing needs to be used.

Three Supply Configuration (接下页)

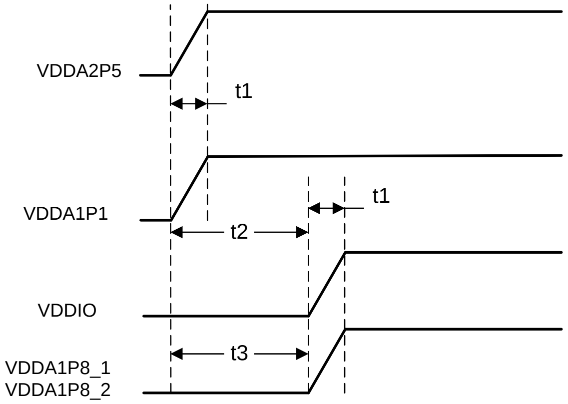


图 117. Three Supply Sequence Diagram

表 102. Three Supply Sequence

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t1	Supply ramp time	Applicable to all supplies	0.5		100	ms
t2	Time instance at which VDDIO starts up	Measured with respect to start of VDDA2P5 and VDDA1P1	0		50	ms
t3	Time instance at which VDDA1P8_x starts up	Measured with respect to start of VDDA2P5 and VDDA1P1	0		50	ms

12 Layout

12.1 Layout Guidelines

12.1.1 Signal Traces

PCB traces are lossy and long traces can degrade the signal quality. Traces must be kept short as possible. Unless mentioned otherwise, all signal traces should be 50-Ω, single-ended impedance. Differential traces should be 50-Ω, single-ended and 100-Ω differential. Take care that the impedance is constant throughout. Impedance discontinuities cause reflections leading to EMI and signal integrity problems. Stubs must be avoided on all signal traces, especially the differential signal pairs. See 图 118.

Within the differential pairs, the trace lengths must run parallel to each other and matched in length. Matched lengths minimize delay differences, avoiding an increase in common-mode noise and increased EMI.

Length matching is also important on MAC interface. All Transmit signal trace lengths must match to each other and all Receive signal trace lengths must match to each other.

Ideally, there should be no crossover or via on the signal paths. Vias present impedance discontinuities and should be minimized. Route an entire trace pair on a single layer if possible.

Layout Guidelines (接下页)

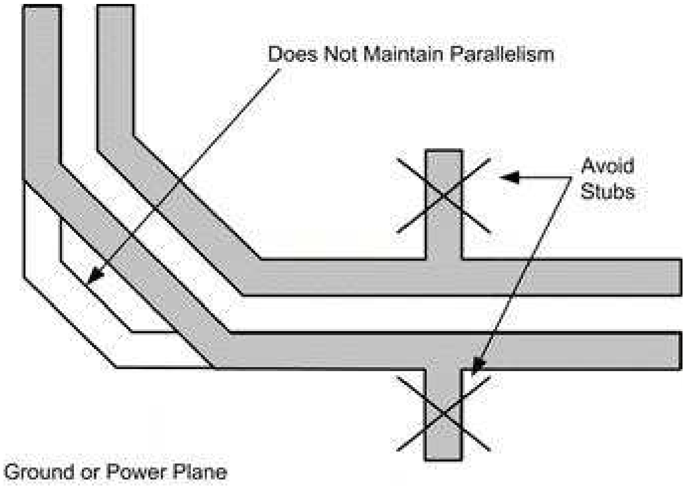


图 118. Avoiding Stubs in a Differential Signal Pair

Signals on different layers should not cross each other without at least one return path plane between them.

Coupling between traces is also an important factor. Unwanted coupling can cause cross talk problems. Differential pairs on the other hand, should have a constant coupling distance between them.

For convenience and efficient layout process, start by routing the critical signals first.

12.1.1.1 MAC Interface Layout Guidelines

The Media Independent Interface (SGMII / RGMII) connects the DP83869 to the Media Access Controller (MAC). The MAC may in fact be a discrete device, integrated into a microprocessor, CPU, or FPGA.

12.1.1.1.1 SGMII Layout Guidelines

- All SGMII connections must be AC-coupled through an 0.1-µF capacitor. Series capacitors must be 0.1 µF and the size should be 0402 or smaller.
- SGMII signals are differential signals.
- Traces must be routed with 100-Ω differential impedance.
- Skew matching within a pair must be less than 5 pS, which correlates to 30 mil for standard FR4.
- There is no requirement to match the TX pair to the RX pair.
- SGMII signals must be routed on the same layer.
- Pairs must be referenced to parallel ground plane.
- When operating in 6-wire mode, the RX pair must match the Clock pair to within 5 pS, which correlates to 30 mil for standard FR4.

12.1.1.1.2 RGMII Layout Guidelines

- RGMII signals are single-ended signals.
- Traces must be routed with impedance of 50 Ω to ground.
- Skew between TXD[3:0] lines should be less than 11 ps, which correlates to 60 mil for standard FR4.
- Skew between RXD[3:0] lines should be less than 11 ps, which correlates to 60 mil for standard FR4.
- Keep trace lengths as short as possible, Traces less than 2 inches is recommended with less than 6 inches as maximum length.
- Configurable clock skew for GTX_CLK and RX_CLK.
  - Clock skew for RX and TX paths can be optimized independently.
  - Clock skew is adjustable in 0.25-ns increments (through register).

Layout Guidelines (接下页)

12.1.1.2 MDI Layout Guidelines

The Media Dependent Interface (MDI) connects the DP83869 to the transformer and the Ethernet network.

- MDI traces must be 50 Ω to ground and 100-Ω differential controlled impedance.
- Route MDI traces to transformer on the same layer.
- Use a metal shielded RJ-45 connector, and connect the shield to chassis ground.
- Use magnetics with integrated common-mode choking devices.
- Void supplies and ground beneath magnetics.
- Do not overlap the circuit and chassis ground planes, keep them isolated. Instead, make chassis ground an isolated island and make a void between the chassis and circuit ground. Connecting circuit and chassis planes using a size 1206 resistor and capacitor on either side of the connector is a good practice.

12.1.2 Return Path

A general best practice is to have a solid return path beneath all signal traces. This return path can be a continuous ground or DC power plane. Reducing the width of the return path width can potentially affect the impedance of the signal trace. This effect is more prominent when the width of the return path is comparable to the width of the signal trace. Breaks in return path beneath the signal traces should be avoided at all cost. A signal crossing a plane split may cause unpredictable return path currents and would likely impact signal quality as well, potentially creating EMI problems. See 图 119.

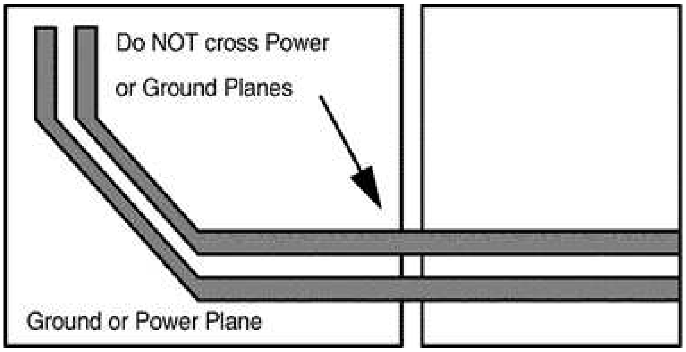


图 119. Differential Signal Pair-Plane Crossing

12.1.3 Transformer Layout

There should be no metal layer running beneath the transformer. Transformers can inject noise in metal beneath them which can affect the performance of the system.

12.1.4 Metal Pour

All metal pours which are not signals or power should be tied to ground. There should be no floating metal on the system. There should be no metal between the differential traces.

12.1.5 PCB Layer Stacking

To meet signal integrity and performance requirements, at minimum a 4-layer PCB should be used. However a 6-layer board is recommended. See 图 120 for the recommended layer stack ups for 4, 6, and 8-layer boards. These are recommendations not requirements, other configurations can be used as per system requirements.

Layout Guidelines (接下页)

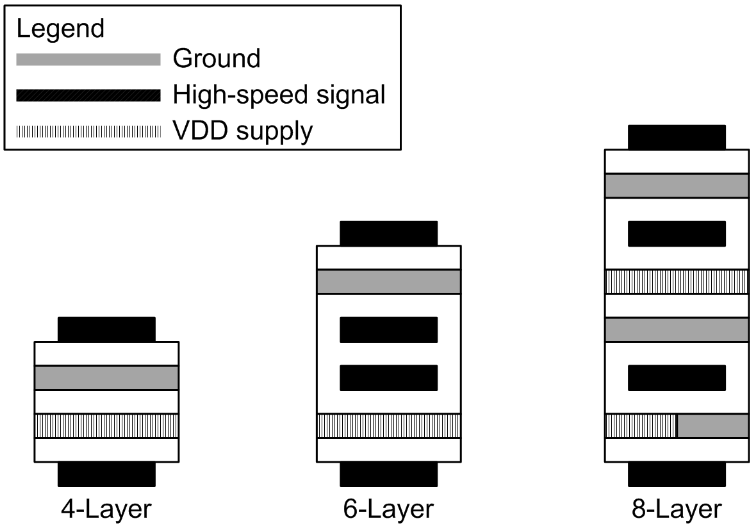


图 120. Recommended Layer Stack-Up

Within a PCB, it may be desirable to run traces using different methods, microstrip vs. stripline, depending on the location of the signal on the PCB. For example, it may be desirable to change layer stacking where an isolated chassis ground plane is used. 图 121 shows alternative PCB stacking options.

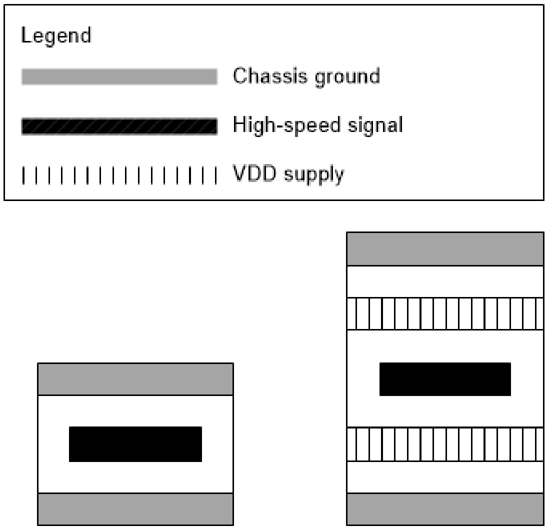


图 121. Alternative Layer Stack-Up

12.2 Layout Example

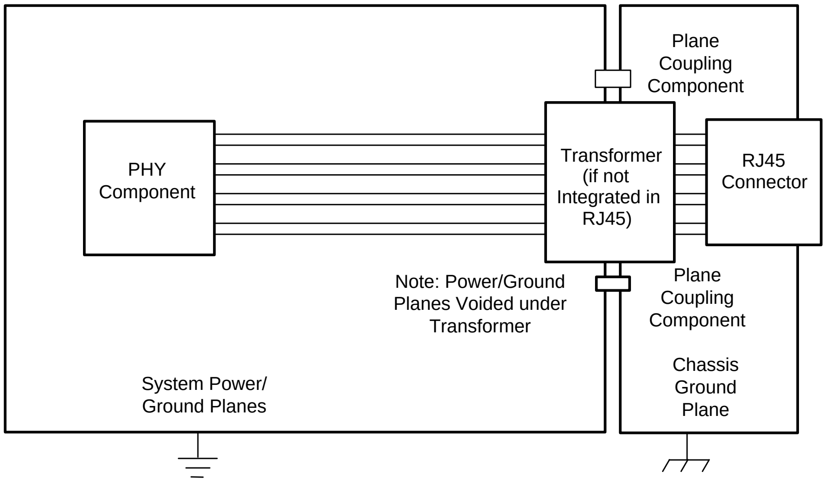


图 122. Copper Ethernet Layout Example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- *《DP83869 1000Base-X 链路检测》*(SNLA305)

13.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

13.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

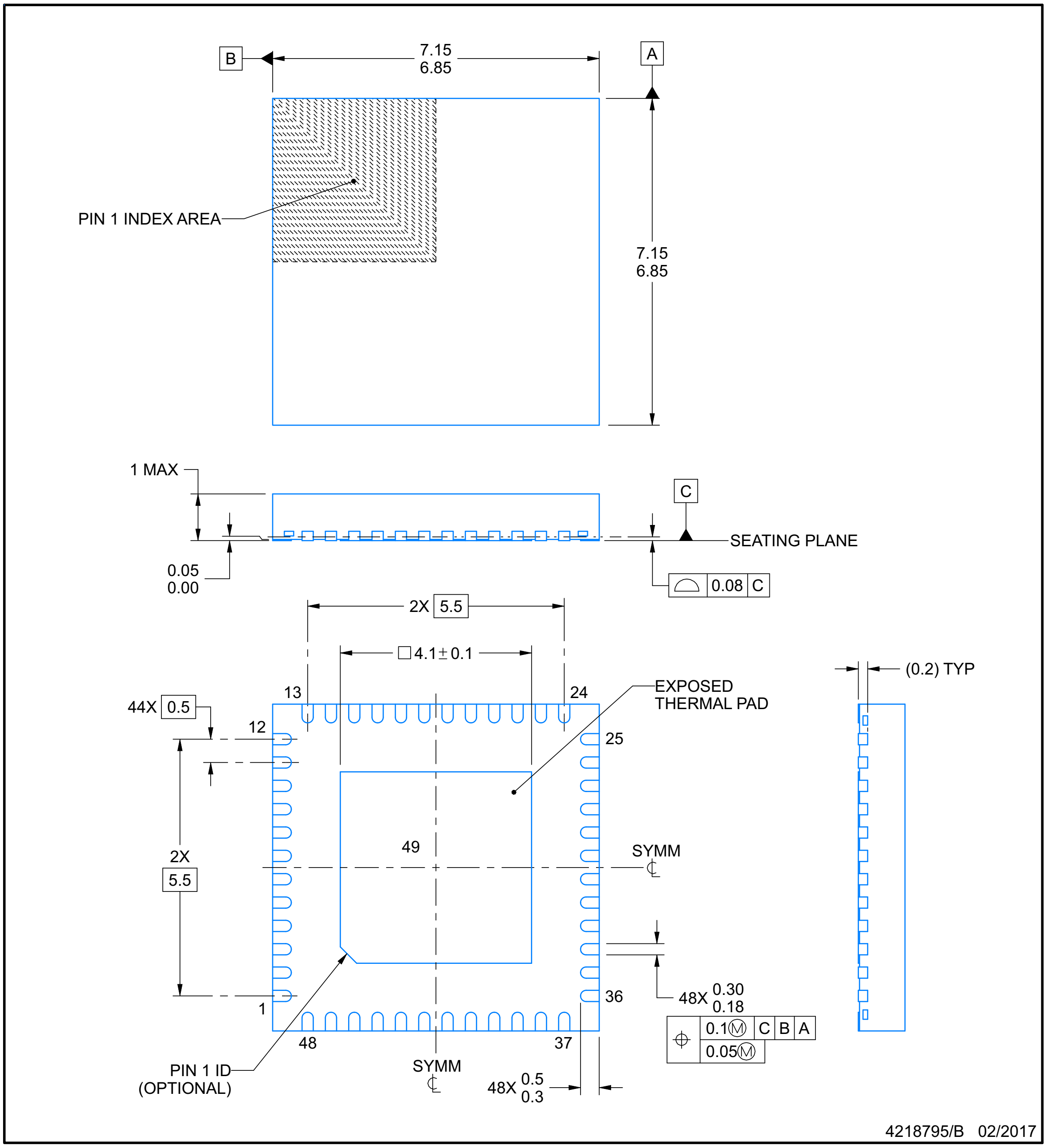
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

RGZ0048B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

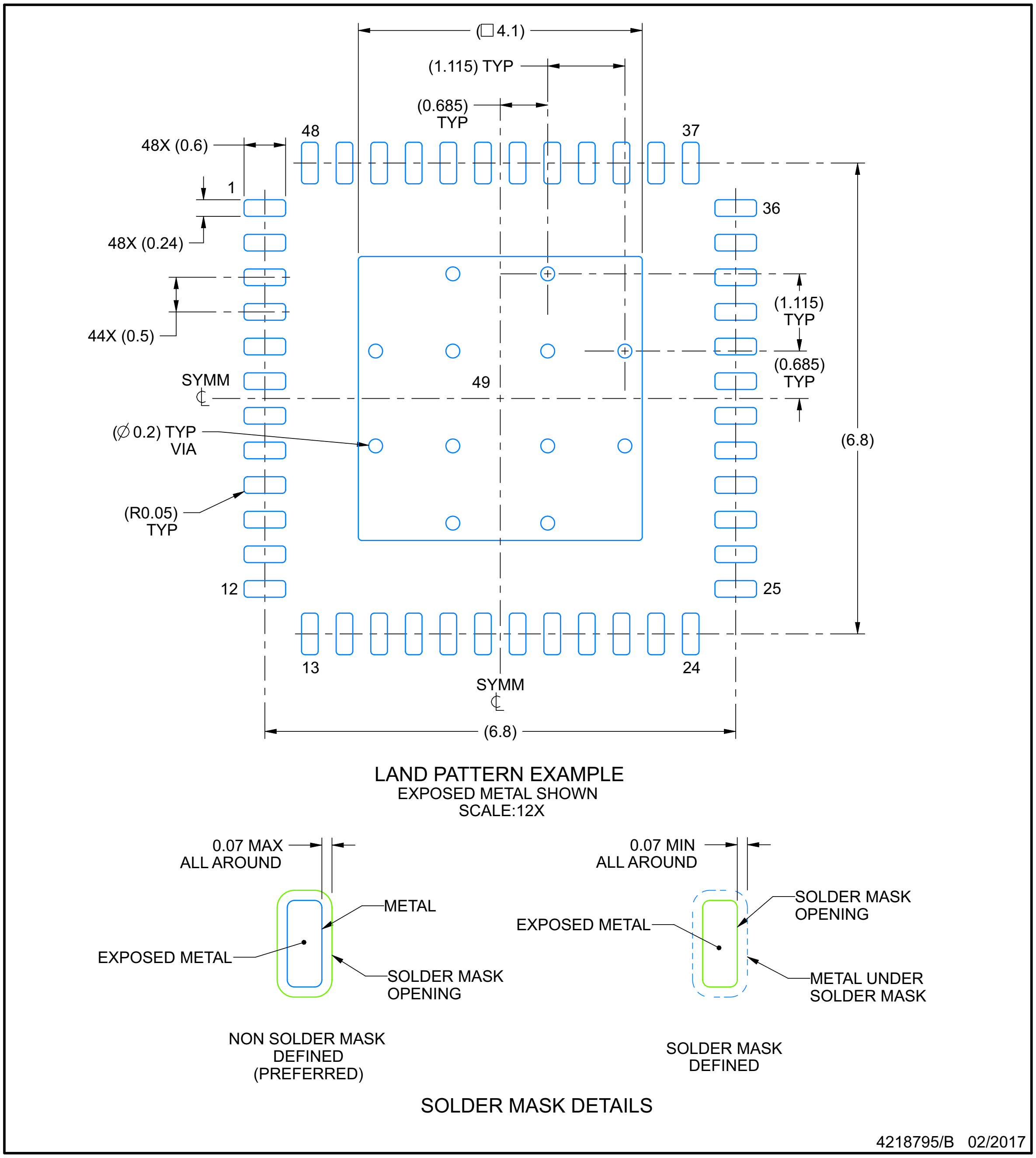
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X

SOLDER MASK DETAILS

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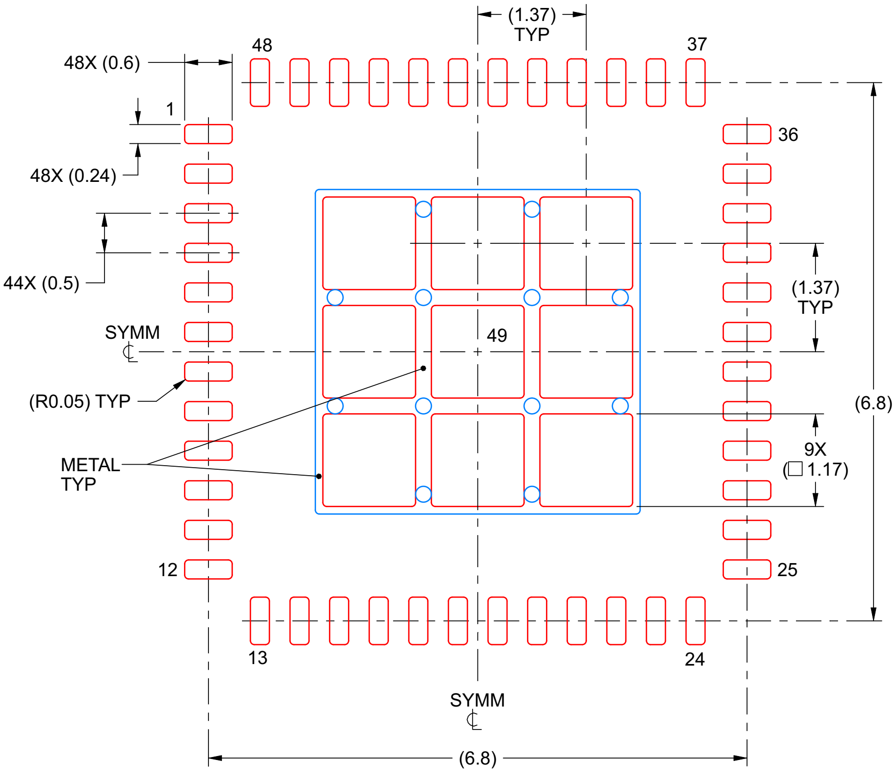
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048B **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

www.ti.com

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DP83869HMRGZR	ACTIVE	VQFN	RGZ	48	2000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DP83869HM	Samples
DP83869HMRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	DP83869HM	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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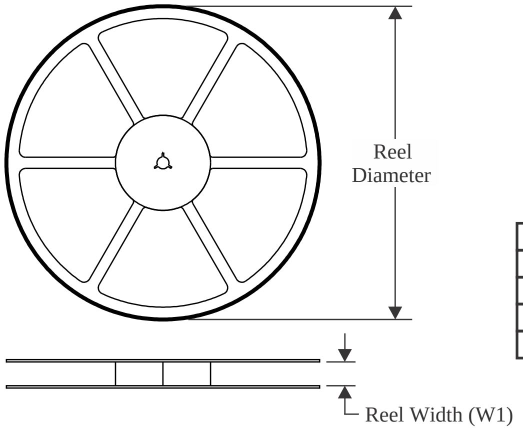
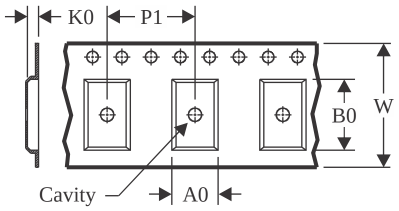
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

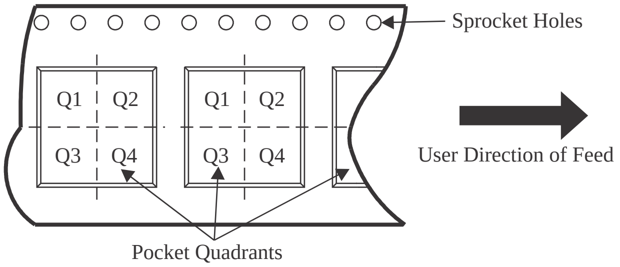


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

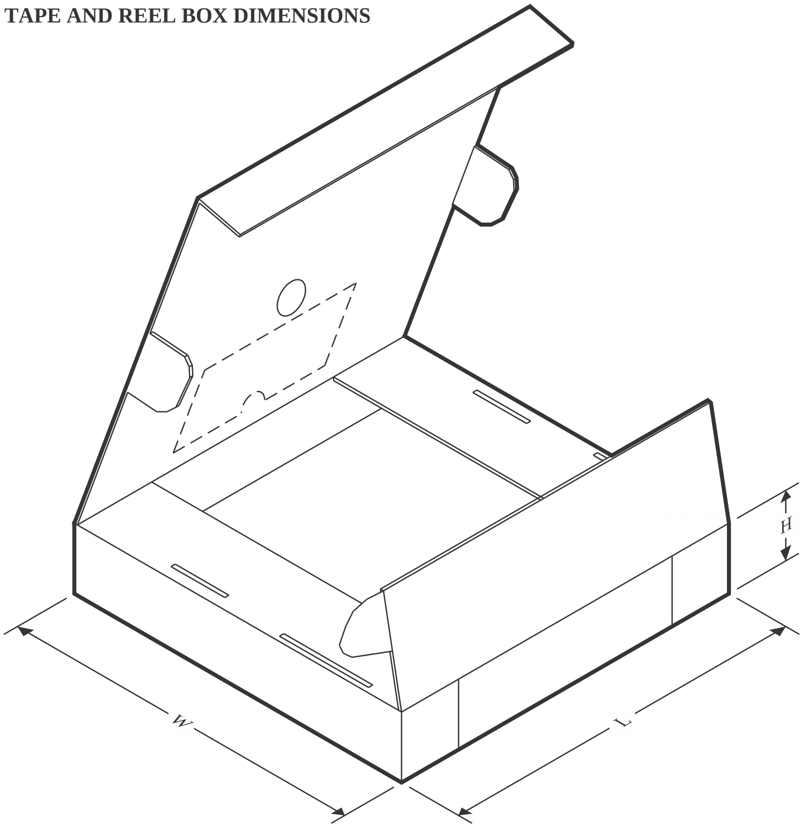
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DP83869HMRGZR	VQFN	RGZ	48	2000	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DP83869HMRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DP83869HMRGZR	VQFN	RGZ	48	2000	367.0	367.0	38.0
DP83869HMRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

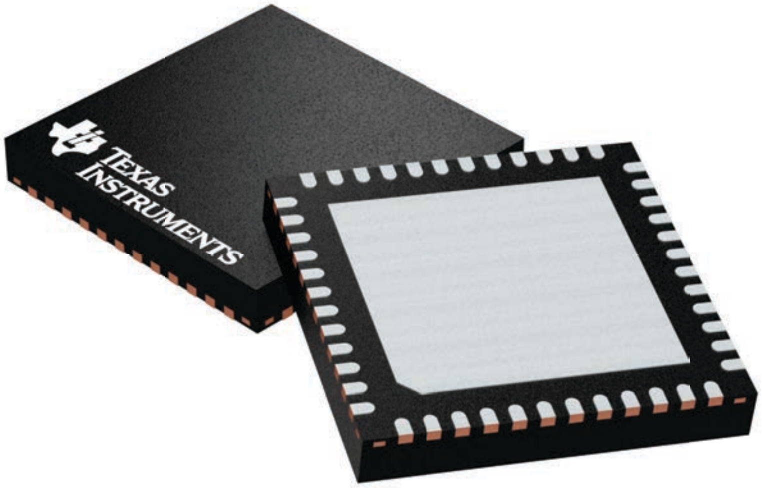
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

重要声明和免责声明

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