DRV8410 具有电流调节功能的双路 H 桥电机驱动器

1 特性

- 双路 H 桥电机驱动器，可驱动 -
  - 一个双极步进电机
  - 一到两个有刷直流电机
  - 电磁阀和其他电感负载
- 低导通电阻：HS + LS = 800mΩ（典型值，25°C）
- 宽电源电压范围
  - 1.65 至 11 V
- 与以下器件引脚对引脚兼容：
  - DRV8833：360mΩ/桥
  - DRV8833C：1735mΩ/桥
  - DRV8847：1000mΩ/桥
  - DRV8411：400mΩ/桥
  - DRV8411A：400mΩ/桥
- 高输出电流能力：2.5A 峰值
- PWM 控制接口
- 支持 1.8V、3.3V 和 5V 逻辑输入
- 集成电流调节
- 低功耗睡眠模式
  - V_{VM} = 5V、T_J = 25°C 时 ≤ 30nA
- 小型封装和外形尺寸
  - 带 PowerPAD™ 的 16 引脚 HTSSOP，5.0mm× 4.4mm
  - 带 PowerPAD™ 的 16 引脚 WQFN，3.0mm × 3.0mm
- 集成保护特性
  - VM 欠压锁定 (UVLO)
  - 自动重试过流保护 (OCP)
  - 热关断 (TSD)
  - 故障指示引脚 (nFAULT)

2 应用

- 电池供电式玩具
- POS 打印机
- 视频安保摄像机
- 办公自动化设备
- 游戏机
- 机器人
- 电子智能锁
- 通用螺线管负载

3 说明

DRV8410 是一款双路 H 桥电机驱动器，可驱动一个或两个直流有刷电机、一个步进电机、螺线管或其他电感负载。三倍电荷泵允许器件在低至 1.65V 的电压下工作，以适应 1.8V 的电源轨和电池电量不足的情况。电荷泵集成了所有电容器并允许 100% 占空比运行。输入和输出可以并联以驱动具有一半 $R_{DS(ON)}$ 的大电流有刷直流电机。

该器件通过将内部基准电压与 xISEN 引脚上的电压进行比较来实现电流调节，该电压与通过外部检测电阻器的电机电流成正比。限制电流的能力可以显著减小电机启动过程中和失速条件下的大电流。

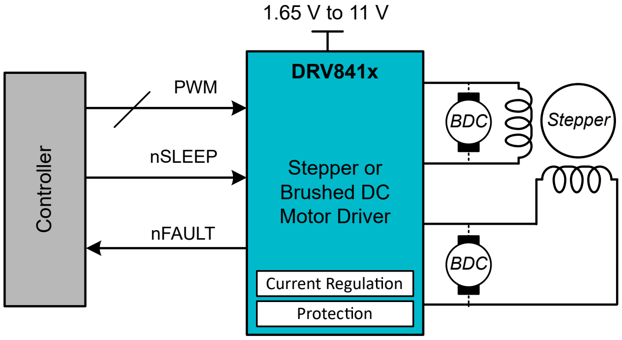
低功耗睡眠模式可通过关断大部分内部电路实现超低静态电流消耗。内部保护特性包括欠压、过流和过热保护。

DRV8410 所属的器件系列具有引脚对引脚、可扩展 $R_{DS(ON)}$ 选项，可支持不同负载，并尽可能减少设计改动。有关本产品系列中器件的信息，请参阅节 5。访问 ti.com 查看我们完整的有刷电机驱动器产品系列。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DRV8410	HTSSOP (16)	5.00mm × 4.40mm
	WQFN (16)	3.00mm × 3.00mm

(1) 有关所有的可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
September 2022	*	Initial Release

5 Device Comparison

表 5-1. Device Comparison Table

Device Name	Supply Voltage (V)	$R_{DS(on)}$ (mΩ)	Overcurrent Protection limit (A)	Current Regulation	Current-Sense Feedback	Direct Pin-to-Pin Replacement	Pin-to-Pin Replacement with Modifications
DRV8410	1.65 to 11	800	2.5	External Shunt Resistor	External Amplifier	DRV8833, DRV8833C	DRV8847
DRV8411	1.65 to 11	400	4				
DRV8411A	1.65 to 11	400		Internal current mirror (IPROPI)		N/A	DRV8833, DRV8833C, DRV8847

6 Pin Configuration and Functions

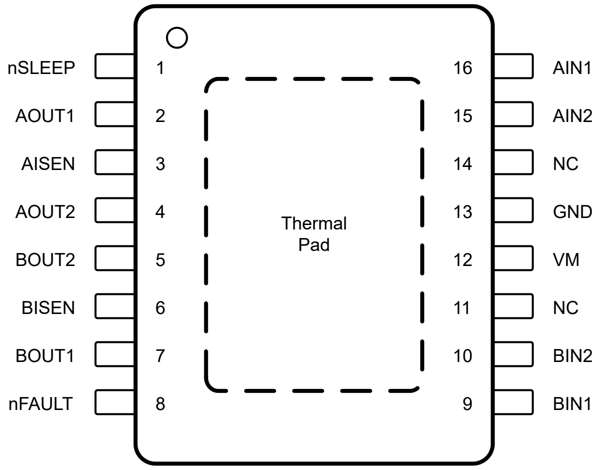


图 6-1. PWP Package 16-Pin HTSSOP Top View

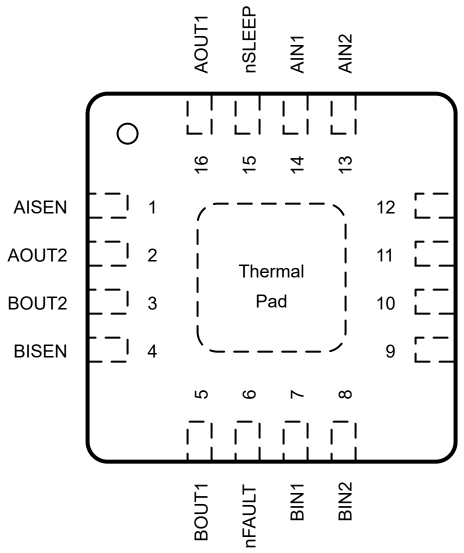


图 6-2. RTE Package 16-Pin WQFN Top View

Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	RTE	PWP		
AIN1	14	16	I	H-bridge control input for full bridge A (AOUT1, AOUT2). See 节 9.4.1. Internal pulldown resistor.
AIN2	13	15	I	H-bridge control input for full bridge A (AOUT1, AOUT2). See 节 9.4.1. Internal pulldown resistor.
AISEN	1	3	O	Full bridge A (AOUT1, AOUT2) sense. Connect this pin to a current sense resistor for full bridge A. Connect this pin to the GND pin if current regulation is not required. See 节 9.4.2.
AOUT1	16	2	O	Bridge A output 1
AOUT2	2	4	O	Bridge A output 2
BIN1	7	9	I	H-bridge control input for full bridge B (BOUT1, BOUT2). See 节 9.4.1. Internal pulldown resistor.
BIN2	8	10	I	H-bridge control input for full bridge B (BOUT1, BOUT2). See 节 9.4.1. Internal pulldown resistor.
BISEN	4	6	O	Full bridge B (BOUT1, BOUT2) sense. Connect this pin to a current sense resistor for full bridge A. Connect this pin to the GND pin if current regulation is not required. See 节 9.4.2.
BOUT1	5	7	O	Bridge B output 1
BOUT2	3	5	O	Bridge B output 2

PIN			TYPE[1]	DESCRIPTION
NAME	**RTE**	**PWP**		
GND	11	13	PWR	Device ground. Connect to system ground.
NC	9, 12	11, 14	—	Not connected
nFAULT	6	8	OD	Fault indicator output. Pulled low during a fault condition. Connect an external pullup resistor for open-drain operation. See 节 9.4.3.
nSLEEP	15	1	I	Sleep mode input. Logic high to enable device. Logic low to enter low-power sleep mode. See 节 9.5.2. Internal pulldown resistor.
PAD	—	—	—	Thermal pad. Connect to system ground.
VM	10	12	PWR	1.65-V to 11-V power supply input. Connect a 0.1-μF bypass capacitor to ground, as well as sufficient Bulk Capacitance rated for VM.

(1) PWR = power, I = input, O = output, NC = no connection, OD = open-drain

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	VM	-0.5	12	V
Power supply transient voltage ramp	VM	0	2	V/µs
Current sense pin voltage	AISEN, BISEN	-0.6	0.6	V
Logic pin voltage	nSLEEP, AIN1, AIN2, BIN1, BIN2	-0.3	5.75	V
Open-drain output pin voltage	nFAULT	0.3	5.75	V
Output pin voltage	AOUT1, AOUT2, BOUT1, BOUT2	$-V_{SD}$	$V_{VM}+V_{SD}$	V
Output current	AOUT1, AOUT2, BOUT1, BOUT2	Internally Limited	Internally Limited	A
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	VM	1.65		11	V
V_{IN}	Logic input voltage	nSLEEP, AIN1, AIN2, BIN1, BIN2	0		5.5	V
f_{PWM}	PWM frequency	AIN1, AIN2, BIN1, BIN2	0		100	kHz
V_{OD}	Open drain pullup voltage	nFAULT	0		5.5	V
I_{OD}	Open drain output current	nFAULT	0		5	mA
I_{OUT} (1)	Peak output current	OUTx	0		$I_{OCP,min}$	A
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

7.4 Thermal Information

THERMAL METRIC(1)		DEVICE	DEVICE	UNIT
		PWP (HTSSOP)	RTE (WQFN)	
		PINS	PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.3	55	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	56.7	°C/W

THERMAL METRIC[1]		DEVICE	DEVICE	UNIT
		PWP (HTSSOP)	RTE (WQFN)	
		PINS	PINS	
$R_{\theta JB}$	Junction-to-board thermal resistance	23.3	28.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.7	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23.3	28.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.5	15.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

1.65 V ⩽ V_{VM} ⩽ 11 V, –40°C ⩽ T_J ⩽ 150°C (unless otherwise noted). Typical values are at T_J = 27 °C and V_{VM} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM)						
I_{VMQ}	VM sleep mode current	nSLEEP = 0 V, V_{VM} = 5 V, T_J = 27°C		4	30	nA
I_{VM}	VM active mode current	xIN1 = 3.3 V, xIN2 = 0 V, V_{VM} = 5 V		1.3	2.5	mA
t_{WAKE}	Turnon time	Sleep mode to active mode delay			100	μs
t_{SLEEP}	Turnoff time	Active mode to sleep mode delay		5		μs
LOGIC-LEVEL INPUTS (nSLEEP, AIN1, AIN2, BIN1, BIN2)						
V_{IL}	Input logic low voltage		0		0.4	V
V_{IH}	Input logic high voltage		1.45		5.5	V
V_{HYS_nSLEEP}	nSLEEP Input hysteresis		100			mV
V_{HYS_logic}	Logic Input hysteresis (except nSLEEP)		50			mV
I_{IL}	Input logic low current	V_{xINx} = 0 V	-1		1	μA
$I_{IH,nSLEEP}$	Input logic high current	V_{nSLEEP} = 5 V			14	μA
I_{IH}	Input logic high current	V_{xINx} = 5 V	20		70	μA
$R_{PD,nSLEEP}$	Input pulldown resistance			500		kΩ
R_{PD}	Input pulldown resistance			100		kΩ
$t_{DEGLITCH}$	Input logic deglitch			50		ns
OPEN-DRAIN OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.3	V
I_{OZ}	Output logic high current	V_{OD} = 5 V	-1		1	μA
DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{HS\_DS(ON)}$	High-side MOSFET on resistance	I_{OUTx} = 0.2 A		400		mΩ
$R_{LS\_DS(ON)}$	Low-side MOSFET on resistance	I_{OUTx} = -0.2 A		400		mΩ
V_{SD}	Body diode forward voltage	I_{OUTx} = -0.5 A		1		V
t_{RISE}	Output rise time	V_{OUTx} rising from 10% to 90% of V_{VM}, V_{VM} = 5 V		100		ns
t_{FALL}	Output fall time	V_{OUTx} falling from 90% to 10% of V_{VM}, V_{VM} = 5 V		50		ns
t_{PD}	Input to output propagation delay	Input crosses 0.8 V to V_{OUTx} = 0.1×V_{VM}, I_{OUTx} = 1 A		600		ns
t_{DEAD}	Output dead time			400		ns
CURRENT REGULATION (AISEN, BISEN)						
V_{TRIP}	xISEN trip voltage		180	200	230	mV
t_{OFF}	Current regulation off time			20		μs
t_{BLANK}	Current regulation blanking time			1.8		μs
t_{DEG}	Current regulation deglitch time			1		μs

1.65 V ≤ V_{VM} ≤ 11 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical values are at T_J = 27 °C and V_{VM} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising			1.6	V
		Supply falling	1.3			V
V_{UVLO_HYS}	Supply UVLO hysteresis	Rising to falling threshold		100		mV
t_{UVLO}	Supply undervoltage deglitch time	V_{VM} falling to OUTx disabled		10		µs
I_{OCP}	Overcurrent protection trip point		2.5			A
V_{OCP_ISEN}	Overcurrent protection trip point on ISEN pin			0.6		V
t_{OCP}	Overcurrent protection deglitch time			4.2		µs
t_{RETRY}	Overcurrent protection retry time			1.6		ms
T_{TSD}	Thermal shutdown temperature		153		193	°C
T_{HYS}	Thermal shutdown hysteresis			18		°C

7.6 Timing Diagrams

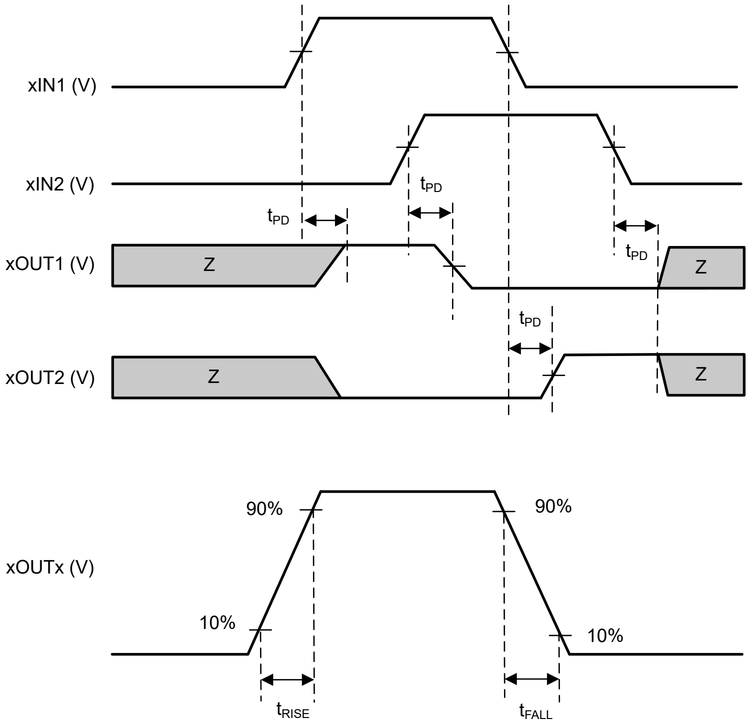


图 7-1. Input-to-Output Timing

8 Typical Characteristics

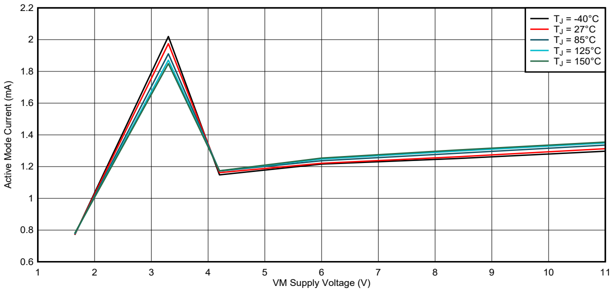


图 8-1. Active Mode Current

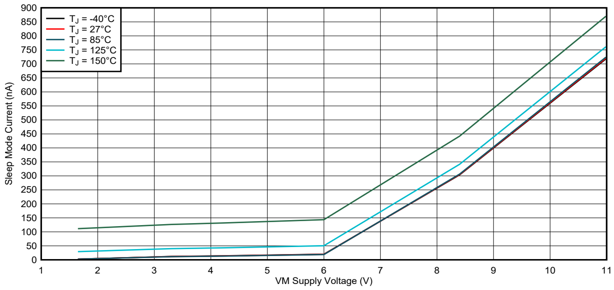


图 8-2. Sleep Mode Current

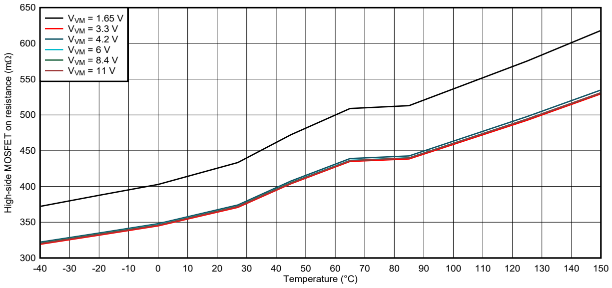


图 8-3. High-side MOSFET on resistance

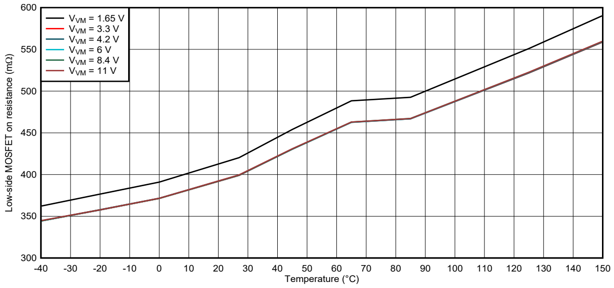


图 8-4. Low-side MOSFET on resistance

9 Detailed Description

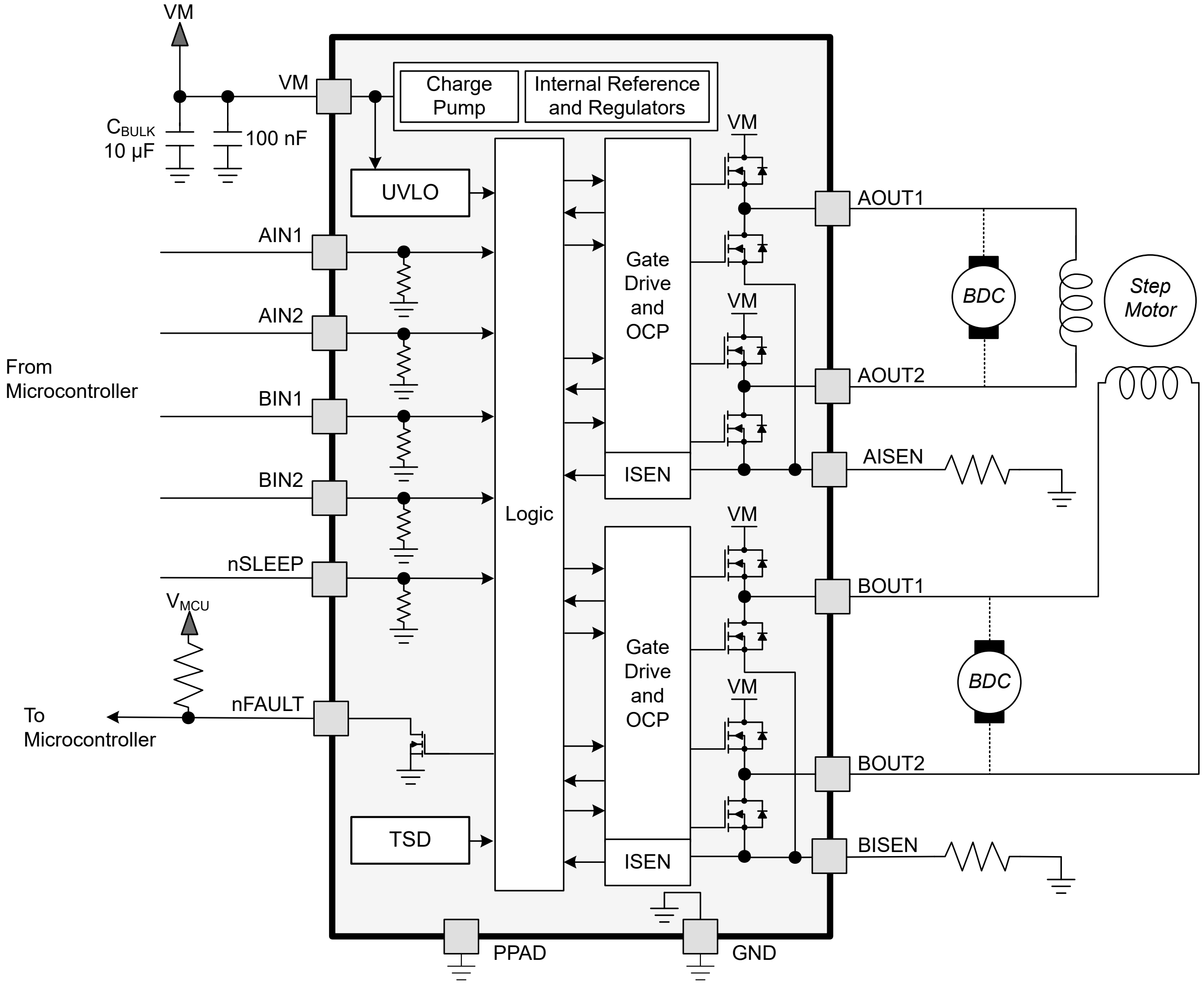
9.1 Overview

The DRV8410 is a dual H-bridge motor driver for driving two brushed DC motors or one stepper motor from a 1.65-V to 11-V supply rail. The integrated current regulation feature limits motor current to a predefined maximum based on xISEN resistors.

Two logic inputs control each H-bridge, which consists of four N-channel MOSFETs that have a typical $R_{DS(ON)}$ of 800 mΩ (including one high-side and one low-side FET). The input and output pins can be paralleled to support a single H-bridge driver with half of the $R_{DS(ON)}$ for driving higher currents. A single power input, VM, serves as both device power and the motor winding bias voltage. The integrated charge pump of the device boosts VM internally and fully enhances the high-side FETs. Motor speed can be controlled with pulse-width modulation, at frequencies between 0 to 100 kHz. The device enters a low-power sleep mode by bringing the nSLEEP pin low.

A variety of integrated protection features protect the device in the case of a system fault. These include undervoltage lockout (UVLO), overcurrent protection (OCP), and overtemperature shutdown (TSD).

9.2 Functional Block Diagram



9.3 External Components

表 9-1 lists the recommended values of the external components for the driver.

表 9-1. DRV8410 External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	VM-rated capacitor, 10 µF minimum
C_{VM2}	VM	GND	0.1-µF, VM rated ceramic capacitor
R_{nFAULT}	VEXT(1)	nFAULT	Pullup resistor, $I_{OD} \leqslant$ 5 mA
R_{AISEN}	AISEN	GND	Sense resistor, see the 节 9.4.2 for sizing
R_{BISEN}	BISEN	GND	Sense resistor, see the 节 9.4.2 for sizing

(1) VEXT is not a pin on the DRV8410, but a pullup resistor on the VEXT external supply voltage is required for the open-drain output, nFAULT.

9.4 Feature Description

9.4.1 Bridge Control

The DRV8410 has two identical H-bridge motor drivers. The input pins, AINx and BINx, control the corresponding outputs, AOUTx and BOUTx, respectively. 表 9-2 shows how the inputs control the H-bridge outputs.

表 9-2. H-Bridge Control

nSLEEP	xIN1	xIN2	xOUT1	xOUT2	DESCRIPTION
0	X	X	High-Z	High-Z	Low-power sleep mode
1	0	0	High-Z	High-Z	Coast/ fast decay; H-bridge disabled to High-Z
1	0	1	L	H	Reverse (Current OUT2 → OUT1)
1	1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	1	L	L	Brake; low-side slow decay

The inputs can be set to constant voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving (forward or reverse) and slow-decay states typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period or PWM "on" time, and IN1 = 1 and IN2 = 1 during the PWM "off" time.

Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current decay is also available. To PWM using fast decay, the PWM signal is applied to one xIN pin while the other is held low, as shown below.

表 9-3. PWM Control of Motor Speed

xIN1	xIN2	DESCRIPTION
PWM	0	Forward PWM, fast decay
1	PWM	Forward PWM, slow decay
0	PWM	Reverse PWM, fast decay
PWM	1	Reverse PWM, slow decay

图 9-1 shows how the motor current flows through the H-bridge. The input pins can be powered before VM is applied.

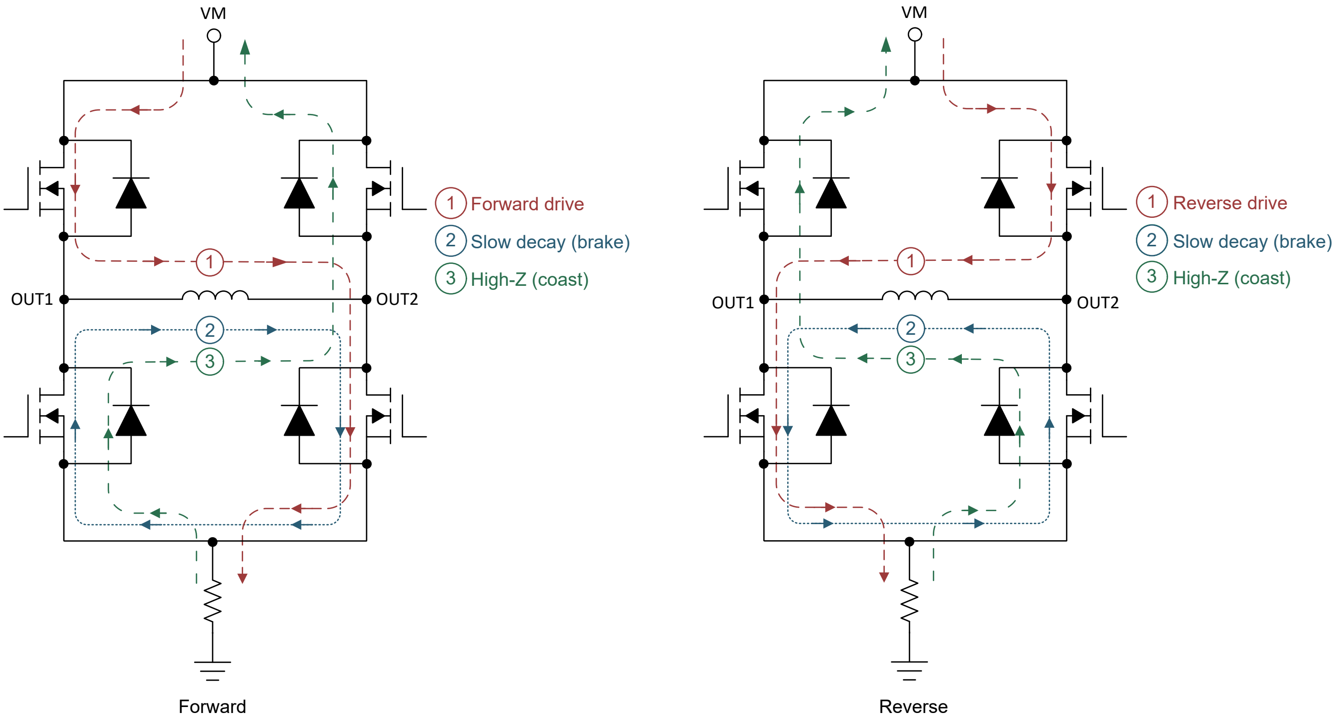


图 9-1. H-Bridge Current Paths

When an output changes from driving high to driving low, or driving low to driving high, dead time is automatically inserted to prevent shoot-through. The t_{DEAD} time is the time in the middle when the output is High-Z. If the output pin is measured during t_{DEAD}, the voltage depends on the direction of current. If the current is leaving the pin, the voltage is a diode drop below ground. If the current is entering the pin, the voltage is a diode drop above VM. This diode is the body diode of the high-side or low-side FET.

The propagation delay time (t_{PD}) is measured as the time between an input edge to output change. This time accounts for input deglitch time and other internal logic propagation delays. The input deglitch time prevents noise on the input pins from affecting the output state. Additional output slew delay timing accounts for FET turn on or turn off times (t_{RISE} and t_{FALL}).

图 9-2 below shows the timing of the inputs and outputs of the motor driver.

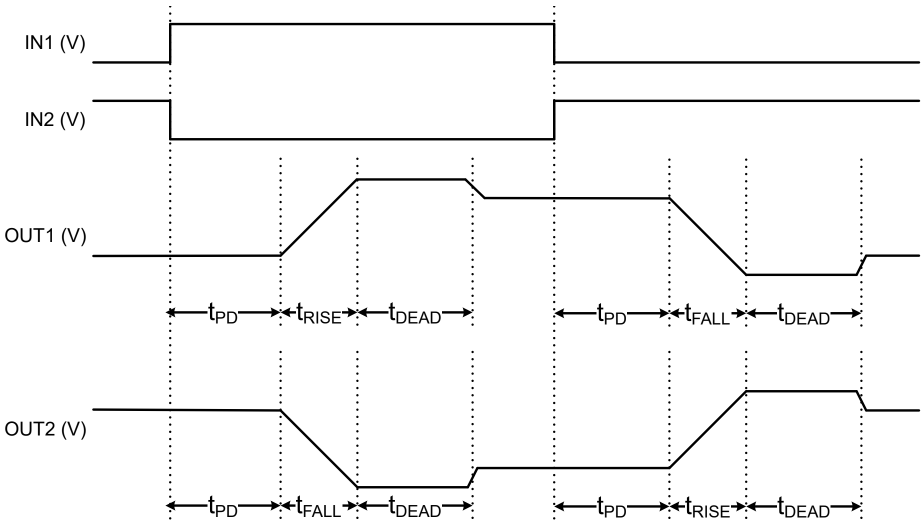


图 9-2. H-Bridge Timing Diagram

9.4.1.1 Parallel Bridge Interface

In the parallel bridge interface, the DRV8410 is configured to drive a higher current brushed-DC (BDC) motor by connecting the driver outputs in parallel to reduce the $R_{DS(ON)}$ by a factor of two. 图 9-3 shows an example of how to connect the pins on the device. To use parallel bridge interface operation, connect AIN1 and BIN1 to the same control signal, IN1, and connect AIN2 and BIN2 to the same control signal, IN2. Similarly, connect AOUT1 and BOUT1 to the same output node, OUT1, and connect AOUT2 and BOUT2 to the same output node, OUT2. AISEN and BISEN must be connected to the same ground plane.

Current regulation may be used if AISEN and BISEN are connected to the same sense resistor. The voltage of the xISEN pins will be compared to the internal V_{TRIP} reference (0.2 V) to set the current regulation level.

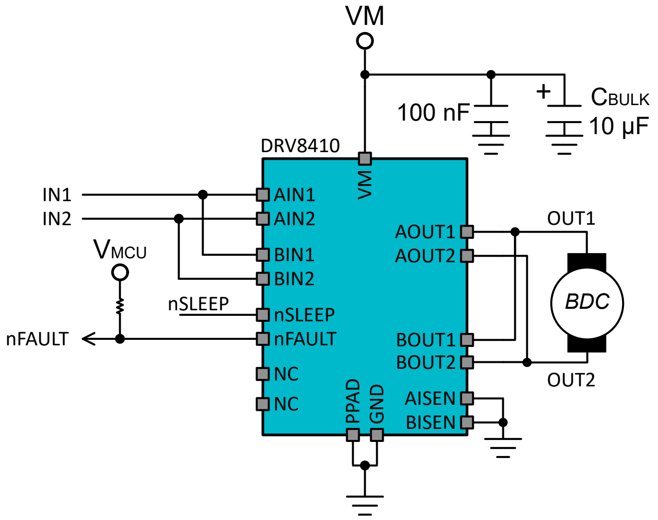


图 9-3. Parallel Mode Connections

This mode can deliver the full functionality of the BDC motor control with all four modes (forward, reverse, coast, and brake mode). 表 9-4 shows the control interface states in parallel mode.

表 9-4. Parallel H-Bridge Control

nSLEEP	IN1 (AIN1 & BIN1)	IN2 (AIN2 & BIN2)	OUT1 (AOUT1 & BOUT1)	OUT2 (AOUT2 & BOUT2)	DESCRIPTION
0	X	X	High-Z	High-Z	Low-power sleep mode
1	0	0	High-Z	High-Z	Coast; H-bridge disabled to High-Z
1	0	1	L	H	Reverse (Current OUT2 → OUT1)
1	1	0	H	L	Forward (Current OUT1 → OUT2)
1	1	1	L	L	Brake; low-side slow decay

9.4.2 Current Regulation

The current through the motor windings may be limited, by the current regulation feature of the DRV8410. For DC motors, current control is used to limit the start-up and stall current of the motor. For stepper motors, current control is often used when the supply rail rating is higher than the motor voltage rating so the winding current remains within the motor specification.

The current regulation feature is implemented with a current chopping scheme. The PWM chopping current, I_{TRIP}, is set by a comparator which compares the voltage across a current sense resistor connected to the xISEN pins with a reference voltage of 200 mV. 图 9-4 shows the relevant circuitry for current regulation of a single H-bridge in DRV8410.

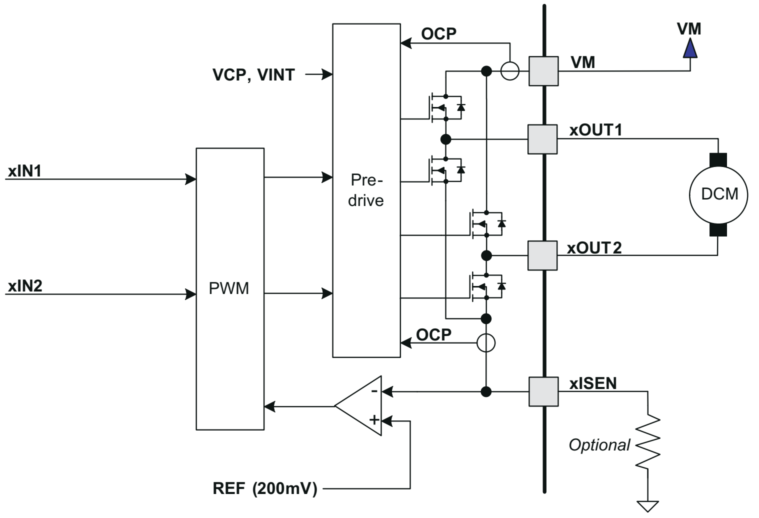


图 9-4. Current Regulation Circuit

When the motor current reaches the I_{TRIP} level, the device enforces slow current decay by enabling both low-side FETs for a duration of t_{OFF} as shown in 图 9-5.

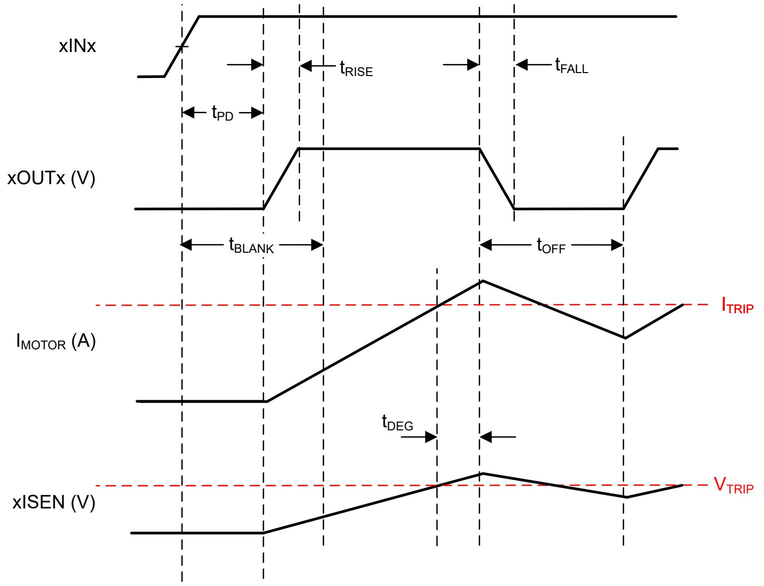


图 9-5. Current-Regulation Time Periods

After t_{OFF} elapses, the output is re-enabled according to the two inputs for that bridge, xINx. The device drives current until the motor current reaches the I_{TRIP} level again. The amount of time spent in the drive state depends on the VM voltage, the back-EMF of the motor, and the inductance of the motor. If the state of the INx control pins changes during the t_{OFF} time, the remainder of the t_{OFF} time is ignored, and the outputs will again follow the inputs.

After t_{OFF} elapses, if I_{OUT} is still greater than I_{TRIP}, the H-bridge enters another period of brake/low-side slow decay for t_{OFF} after a drive time of t_{BLANK}.

The chopping current is calculated in 方程式 1.

$$R_{SENSE} = 0.2\ V / I_{TRIP} \tag{1}$$

Example: If a 1-Ω sense resistor is used, the chopping current will be 200 mV/1 Ω = 200 mA.

If current regulation is not required, the xISEN pins should be directly connected to the PCB ground plane.

9.4.3 Protection Circuits

The DRV8410 is fully protected against undervoltage, overcurrent and overtemperature events.

9.4.3.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive internally. If this current limit persists for longer than the OCP deglitch time (t_{OCP}), all FETs in the H-bridge will disable and the nFAULT pin will assert low. The driver re-enables after the OCP retry period (t_{RETRY}) has passed. nFAULT becomes high again at this time and normal operation resumes. If the fault condition is still present, the cycle repeats as shown in 图 9-6. Please note that only the H-bridge where an overcurrent condition is detected will be disabled while the other bridge will function normally.

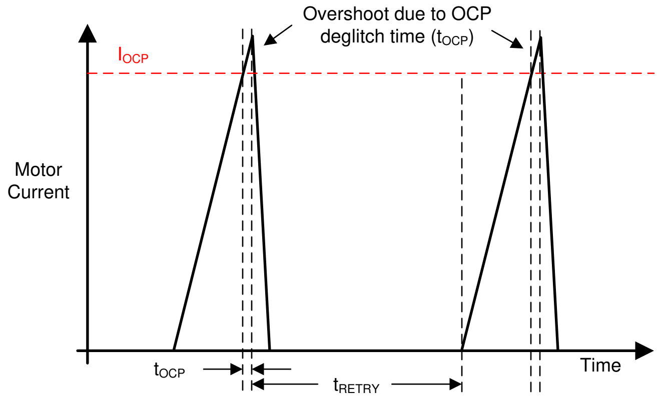


图 9-6. OCP Operation

Overcurrent conditions are detected independently on both high- and low-side FETs. This means that a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. The xISEN pins also integrate a separate overcurrent trip threshold specified by V_{OCP_ISEN} for additional protection when the VM voltage is low or the R_{SENSE} resistance on the xISEN pin is high.

9.4.3.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin asserts low. Once the die temperature has fallen to a safe level, operation will automatically resume.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or an ambient temperature outside of the Recommended Operating Conditions.

9.4.3.3 Undervoltage Lockout (UVLO)

Whenever the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, the output FETS are disabled, and all internal logic is reset. Normal operation resumes when the V_{VM} voltage rises above the UVLO rising threshold as shown in 图 9-7. The nFAULT pin is driven low during an undervoltage condition and is released after operation starts again.

When V_{VM} is close to 0 V, the internal circuitry may not bias properly, and the open-drain pull-down on the nFAULT pin may release.

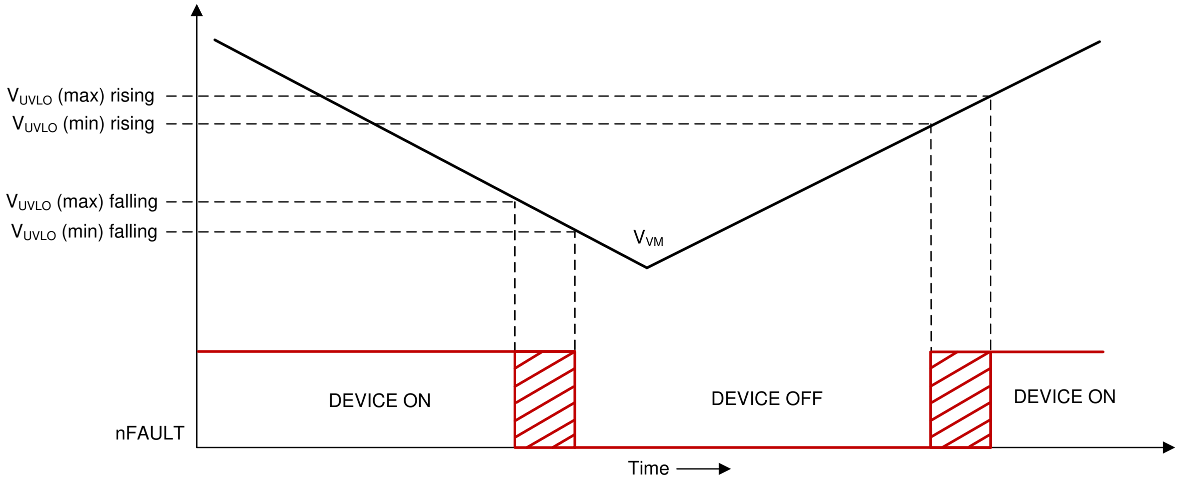


图 9-7. VM UVLO Operation

9.5 Device Functional Modes

表 9-5 summarizes the DRV8410 functional modes described in this section.

表 9-5. Modes of Operation

MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUITS
Active Mode	nSLEEP pin high	Operating	Operating
Low-Power Sleep Mode	nSLEEP pin low	Disabled	Disabled
Fault Mode	Any fault condition met	Disabled	See 表 9-6

9.5.1 Active Mode

After the supply voltage on the VM pin has crossed the undervoltage threshold V_{UVLO}, the nSLEEP pin is high, and t_{WAKE} has elapsed, the device enters active mode. In this mode, the H-bridge, charge pump, and internal logic are active and the device is ready to receive inputs.

9.5.2 Low-Power Sleep Mode

The DRV8410 device supports a low power mode to reduce current consumption from the VM pin when the driver is not active. This mode is entered by setting nSLEEP = logic low and waiting for t_{SLEEP} to elapse.

In sleep mode, the H-bridge, charge pump, internal regulator, and internal logic are disabled and the device draws minimal current from the supply pin (I_{VMQ}). The device relies on a weak pulldown to ensure all of the internal MOSFETs remain disabled. If the device is powered up while the nSLEEP pin is low, it immediately enters sleep mode. After the nSLEEP pin is high for longer than the duration of t_{WAKE}, the device becomes fully operational.

The following timing diagram shows an example of entering and leaving sleep mode.

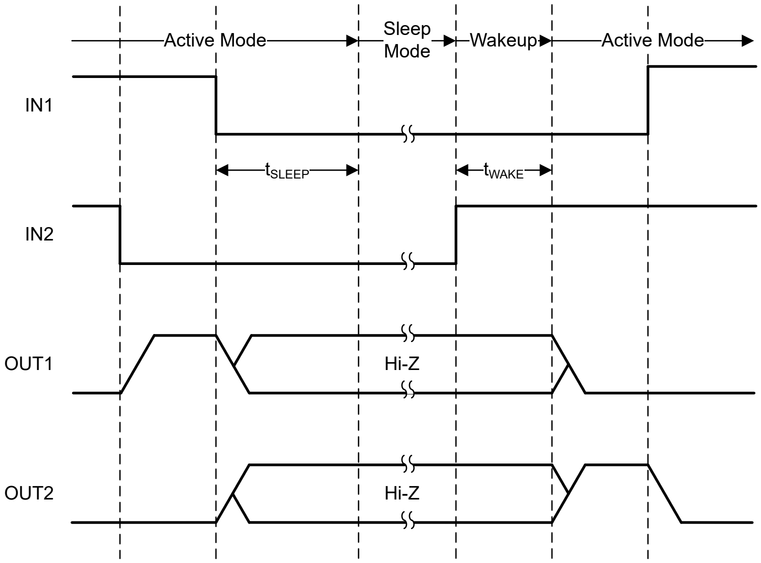


图 9-8. Sleep Mode Entry and Wakeup Timing Diagram

9.5.3 Fault Mode

The DRV8410 device enters a fault mode when a fault is encountered. This protects the device and the load on the outputs. The device behavior in the fault mode is described in 表 9-6 and depends on the fault condition. The device will leave the fault mode and re-enter the active mode when the recovery condition is met.

表 9-6. Fault Conditions Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	$V_M < V_{UVLO,falling}$	nFAULT	Disabled	Disabled	$V_M > V_{UVLO,rising}$
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$	nFAULT	Disabled	Operating	Automatic retry: t_{RETRY}
Thermal Shutdown (TSD)	$T_J > T_{TSD}$	nFAULT	Disabled	Operating	Automatic: $T_J < T_{TSD} – T_{HYS}$

9.6 Pin Diagrams

9.6.1 Logic-Level Inputs

图 9-9 shows the input structure for the logic-level input pins AIN1, AIN2, BIN1, BIN2, and nSLEEP.

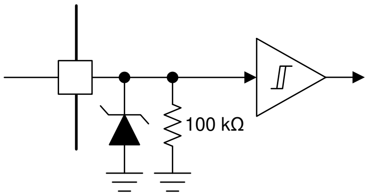


图 9-9. Logic-level input

10 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

The DRV8410 is used in brushed-DC or stepper motor control as shown in the following applications examples.

10.1.1 Typical Application

The user can configure the DRV8410 for stepper motor, dual BDC, or single BDC motor applications as described in this section.

10.1.1.1 Stepper Motor Application

图 10-1 shows the typical application of the DRV8410 device to drive a stepper motor.

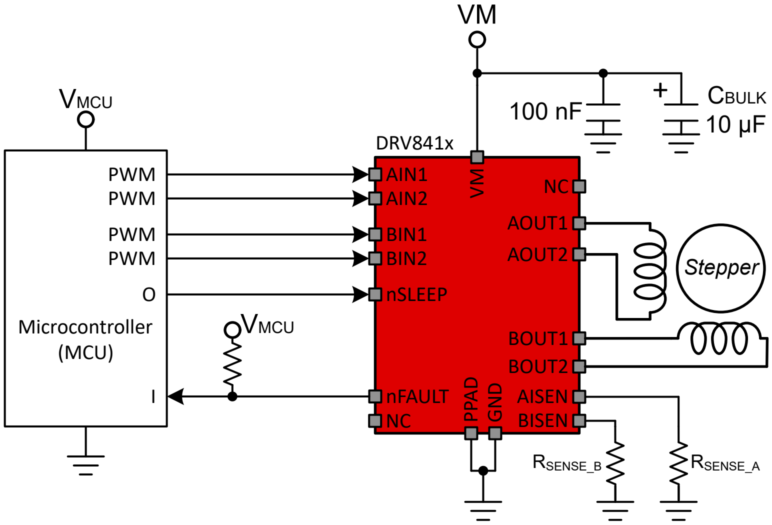


图 10-1. Typical Application Schematic of DRV8410 Driving Stepper Motor

10.1.1.1.1 Design Requirements

表 10-1 lists design input parameters for system design.

表 10-1. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	11 V
Motor winding resistance	R_L	34 Ω/phase
Motor winding inductance	L_L	33 mH/phase
Target trip current	I_{TRIP}	500 mA

10.1.1.1.2 Detailed Design Procedure

10.1.1.1.2.1 Stepper Motor Speed

The first step in configuring the DRV8410 requires the desired motor speed and stepping level. The device can support full- and half-stepping modes using the PWM interface.

If the target motor speed is too high, the motor does not spin. Ensure that the motor can support the target speed.

For a desired motor speed (v), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\,(\text{steps / s}) = \frac{v(\text{rpm}) \times n_m\,(\text{steps}) \times 360^\circ / \text{rot}}{\theta_{step}\,(^\circ / \text{step}) \times 60\ \text{s / min}} \tag{2}$$

10.1.1.1.2.2 Current Regulation

The trip current (I_{TRIP}) is the maximum current driven through either winding. This setting determines the amount of torque the stepper motor will produce when operating in full stepping or half stepping control schemes. For an I_{TRIP} value of 500 mA, the value of the sense resistor (R_{SENSE_x}) is calculated as shown in 方程式 3.

$$R_{SENSE\_A} = R_{SENSE\_B} = 0.2\ \text{V} / I_{TRIP} = 0.2\ \text{V} / 0.5\ \text{A} = 400\ \text{m}\Omega \tag{3}$$

Select the closest available value of 400 mΩ for the sense resistors.

10.1.1.1.2.3 Stepping Modes

The DRV8410 is used to drive a stepper motor in full-stepping mode or non-circulating half-stepping mode using the following bridge configurations:

- Full-stepping mode
- Half-stepping mode with slow decay
- Half-stepping mode with fast decay

10.1.1.1.2.3.1 Full-Stepping Operation

In full-stepping mode, the full-bridge operates in either of two modes (forward or reverse mode) with a phase shift of 90° between the two windings. Full stepping is simplest stepper control mode to implement in firmware and offers the best performance at high speeds.

The controller applies the PWM input to the AIN1, AIN2, BIN1, and BIN2 pins as shown in 图 10-2 and the driver operates only in forward (FRW) and reverse (REV) mode.

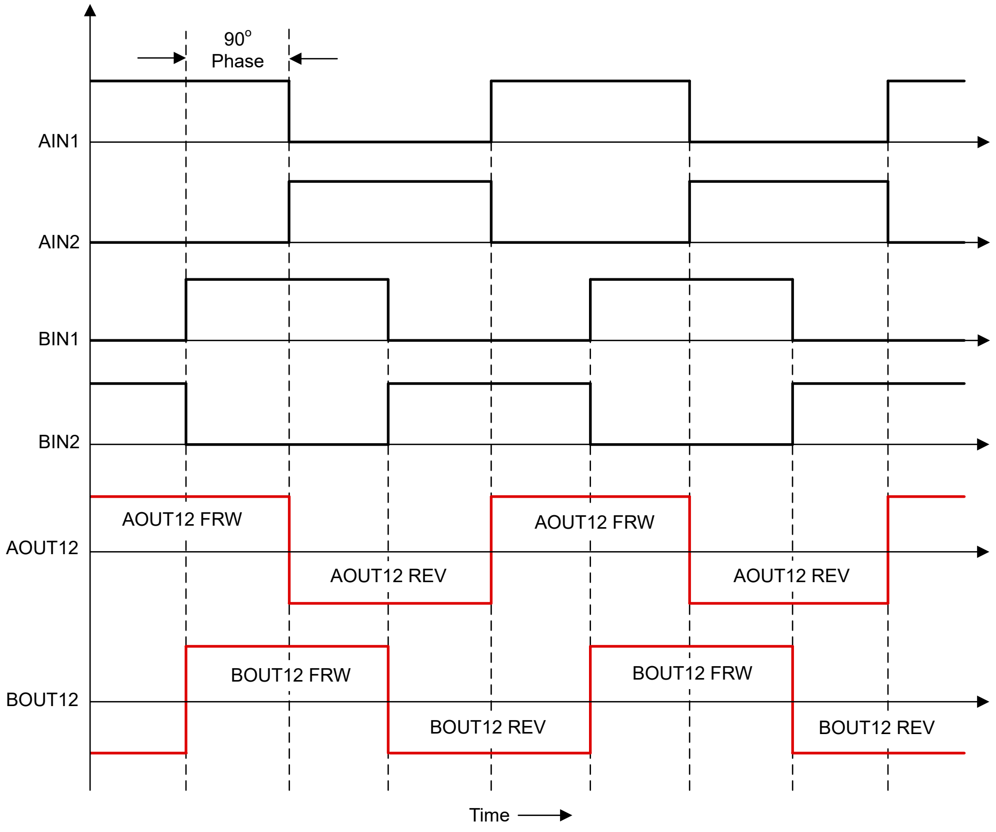


图 10-2. Timing Diagram for Full-Stepping

10.1.1.1.2.3.2 Half-Stepping Operation with Fast Decay

In half-stepping mode, the full-bridge operates in one of the three modes (forward, reverse, or coast mode) to position the rotor half-way between two full-step positions. The coast state allows the current in the motor winding to decay quickly to 0 A. This mode is best-used when half-stepping at high speeds.

The controller applies the PWM input to the AIN1, AIN2, BIN1, and BIN2 pins as shown in 图 10-3, and the driver operates in forward, reverse, and coast mode.

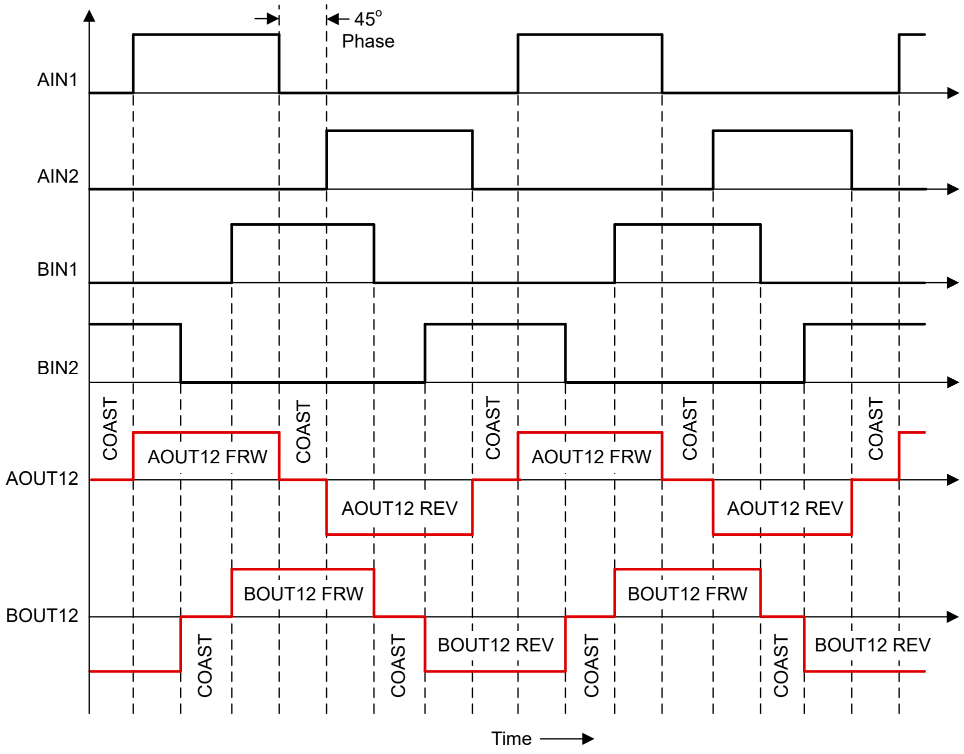


图 10-3. Timing Diagram for Half-Stepping with Fast Decay

10.1.1.1.2.3.3 Half-Stepping Operation with Slow Decay

In this half-stepping mode, the driver achieves the 0-A state using the slow decay control state (known as "brake mode" for BDC driving). Therefore, the full-bridge operates in one of the three modes (forward, reverse, or brake/slow-decay mode) to position the rotor half-way between two full-step positions. The slow decay state allows the current in the motor winding to decay slowly to 0 A. This mode is best-used when half-stepping at slow speeds and may help to reduce stepper noise and vibration.

The controller applies the PWM input to the AIN1, AIN2, BIN1, and BIN2 pins as shown in 图 10-4, and the driver operates in forward, reverse, and brake mode.

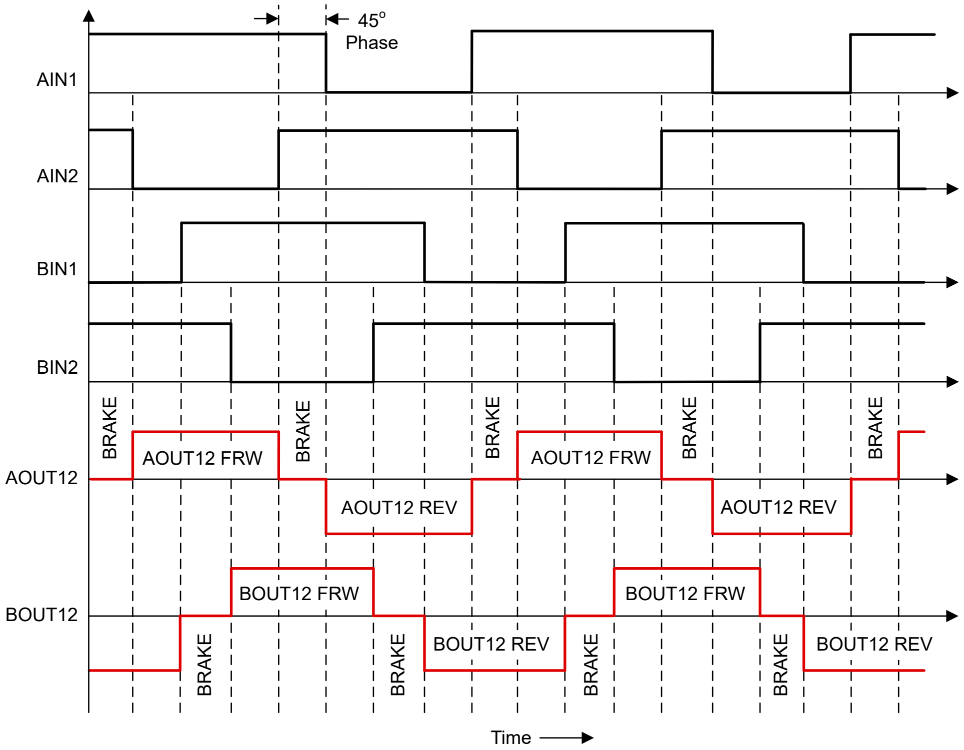


图 10-4. Timing Diagram for Half-Stepping with Slow Decay

10.1.1.1.3 Application Curves

Ch 1 = AIN1, Ch 2 = AIN2, Ch 3 = BIN1, Ch 4 = BIN2, Ch 5 = AOUT12, Ch 6 = BOUT12, Ch 7 = AOUT12 current, Ch 8 = BOUT12 current

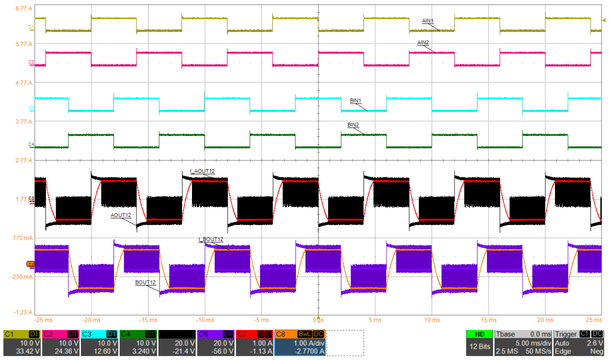


图 10-5. Stepper Motor Full-Step Operation

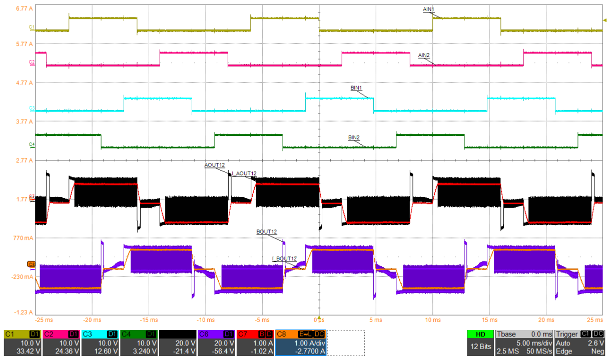


图 10-6. Stepper Motor Half-Step Operation With Fast Decay

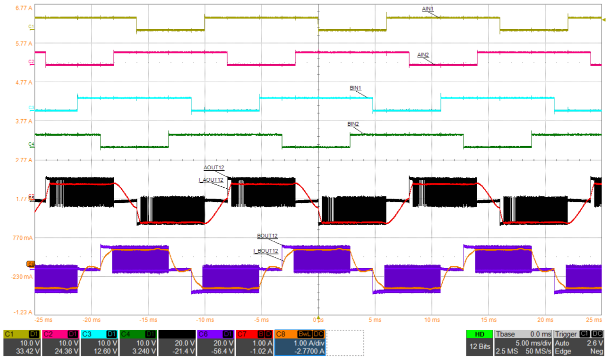


图 10-7. Stepper Motor Half-Step Operation With Slow Decay

ADVANCE INFORMATION

10.1.1.2 Dual BDC Motor Application

图 10-8 shows the typical application of DRV8410 to drive two BDC motors.

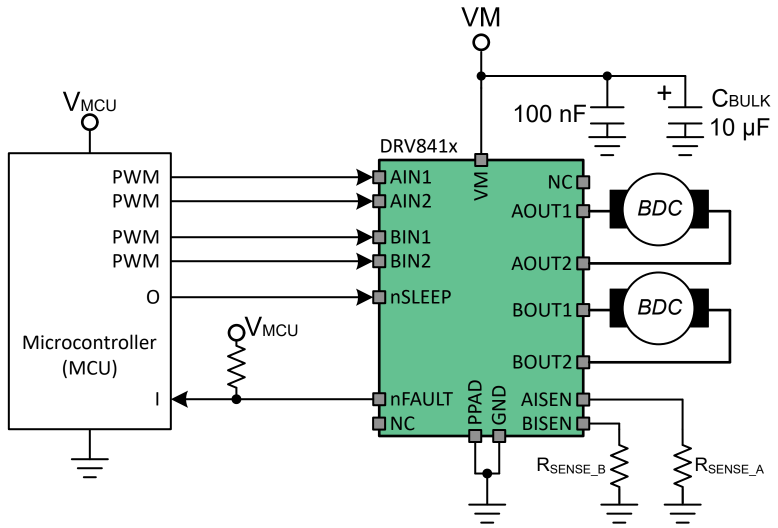


图 10-8. Typical Application Schematic of Device Driving Two BDC Motors

10.1.1.2.1 Design Requirements

表 10-2 lists the design input parameters for system design.

表 10-2. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Motor supply voltage	V_M	7 V
Motor winding resistance	R_L	13.2 Ω
Motor winding inductance	L_L	500 µH
Motor RMS current	I_{RMS}	490 mA
Motor start-up current	I_{START}	900 mA
Target trip current	I_{TRIP}	1.2 A
Trip current reference voltage (internal voltage)	V_{TRIP}	200 mV

10.1.1.2.2 Detailed Design Procedure

10.1.1.2.2.1 Motor Voltage

The motor voltage used in an application depends on the rating of the selected motor and the desired revolutions per minute (RPM). A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

10.1.1.2.2.2 Current Regulation

The trip current (I_{TRIP}) is the maximum current driven through either winding. Because the peak current (start current) of the motor is 900 mA, the I_{TRIP} current level is selected to be just greater than the peak current. The selected I_{TRIP} value for this example is 1.2 A. Therefore, use 方程式 4 to select the value of the sense resistors (R_{SENSE_A} and R_{SENSE_B}) connected to the AISEN and BISEN pins.

$$R_{SENSE\_A} = R_{SENSE\_B} = 0.2\ V / I_{TRIP} = 0.2\ V / 1.2\ A = 167\ m\Omega \qquad (4)$$

10.1.1.2.2.3 Sense Resistor

For optimal performance, the sense resistor must:

- Be a surface mount component
- Have low inductance
- Be rated for high enough power
- Be placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}{}^2 \times R$. In this example, the peak current is 900 mA, the RMS motor current is 490 mA, and the sense resistor value is 160 mΩ. Therefore, the sense resistors ($R_{SENSE12}$ and $R_{SENSE34}$) dissipate 30 mW (490 mA^2 × 160 mΩ = 38 mW). The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a printed circuit board (PCB) is shared with other components generating heat, margin should be added. For best practice, measure the actual sense resistor temperature in a final system, along with the power MOSFETs, because those components are often the hottest.

Because power resistors are larger and more expensive than standard resistors, the common practice is to use multiple standard resistors in parallel, between the sense node and ground. This practice distributes the current and heat dissipation.

10.1.1.3 Thermal Considerations

10.1.1.3.1 Maximum Output Current

In actual operation, the maximum output current achievable with a motor driver is a function of die temperature. This, in turn, is greatly affected by ambient temperature and PCB design. Basically, the maximum motor current will be the amount of current that results in a power dissipation level that, along with the thermal resistance of the package and PCB, keeps the die at a low enough temperature to stay out of thermal shutdown.

The dissipation ratings given in the data sheet can be used as a guide to calculate the approximate maximum power dissipation that can be expected to be possible without entering thermal shutdown for several different PCB constructions. However, for accurate data, the actual PCB design must be analyzed through measurement or thermal simulation.

10.1.1.3.2 Power Dissipation

Power dissipation in the device is dominated by the DC power dissipated in the output FET resistance, or $R_{DS(ON)}$. There is additional power dissipated due to PWM switching losses, which are dependent on PWM frequency, rise and fall times, and VM supply voltages.

The DC power dissipation of one H-bridge can be roughly estimated by 方程式 5.

$$P_{TOT} = \left(HS - R_{DS(ON)} \times I_{OUT(RMS)}{}^2\right) + \left(LS - R_{DS(ON)} \times I_{OUT(RMS)}{}^2\right) \qquad (5)$$

where

- P_{TOT} is the total power dissipation
- HS - $R_{DS(ON)}$ is the resistance of the high-side FET
- LS - $R_{DS(ON)}$ is the resistance of the low-side FET
- $I_{OUT(RMS)}$ is the RMS output current being applied to the motor

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when estimating the maximum output current.

10.1.1.3.3 Thermal Performance

The datasheet-specified junction-to-ambient thermal resistance, $R_{\theta JA}$, is primarily useful for comparing various drivers or approximating thermal performance. However, the actual system performance may be better or worse than this value depending on PCB stackup, routing, number of vias, and copper area around the thermal pad. The length of time the driver drives a particular current will also impact power dissipation and thermal performance. This section considers how to design for steady-state and transient thermal conditions.

The data in this section was simulated using the following criteria:

HTSSOP (PWP package)

- 2-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness. Thermal vias are only present under the thermal pad (12 vias in 4 x 3 array, 1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: HTSSOP package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Bottom layer: ground plane thermally connected through vias under the thermal pad for the driver. Bottom layer copper area varies with top copper area.
- 4-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness. Inner planes are kept at 1-oz. Thermal vias are only present under the thermal pad (12 vias in 4 x 3 array, 1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: HTSSOP package footprint and copper plane heatsink. Top layer copper area is varied in simulation.
  - Mid layer 1: GND plane thermally connected to thermal pad through vias. The area of the ground plane is 74.2 mm x 74.2 mm.
  - Mid layer 2: power plane, no thermal connection. The area of the power plane is 74.2 mm x 74.2 mm.
  - Bottom layer: signal layer with small copper pad underneath the driver and thermally connected through via stitching from the TOP and internal GND plane. Bottom layer thermal pad is the same size as the package (5 mm x 4.4 mm). Bottom pad size remains constant as top copper plane is varied.

图 10-9 shows an example of the simulated board for the HTSSOP package. 表 10-3 shows the dimensions of the board that were varied for each simulation.

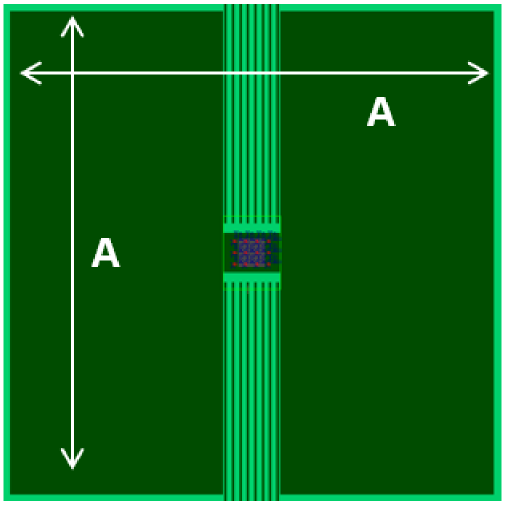


图 10-9. HTSSOP PCB model top layer

表 10-3. Dimension A for 16-pin PWP package

Cu area (cm^2)	Dimension A (mm)
2	16.43
4	22.23
8	30.59
16	42.37

WQFN (RTE package)

- 2-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4, 1-oz (35 mm copper thickness) or 2-oz copper thickness. Thermal vias are only present under the package footprint (5 vias, 1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).

  - Top layer: WQFN package footprint and traces.
  - Bottom layer: ground plane thermally connected through vias under the package footprint. Bottom layer copper area is varied in simulation.
- 4-layer PCB (size 114.3 x 76.2 x 1.6 mm), standard FR4. Outer planes are 1-oz (35 mm copper thickness) or 2-oz copper thickness. Inner planes are kept at 1-oz. Thermal vias are only present under the package footprint (5 vias, 1 mm pitch, 0.2 mm diameter, 0.025 mm Cu plating).
  - Top layer: WQFN package footprint and traces.
  - Mid layer 1: GND plane thermally connected under package footprint through vias. The area of the ground plane is 74.2 mm x 74.2 mm.
  - Mid layer 2: power plane, no thermal connection. The area of the power plane is 74.2 mm x 74.2 mm.
  - Bottom layer: signal layer with small copper pad underneath the driver and thermally connected through via stitching from the TOP and internal GND plane. Bottom layer thermal pad is 1.55 mm x 1.55 mm. Bottom layer thermal pad is the same size as the package (3 mm x 3 mm). Bottom pad size remains constant.

图 10-10 shows an example of the simulated board for the HTSSOP package. 表 10-4 shows the dimensions of the board that were varied for each simulation.

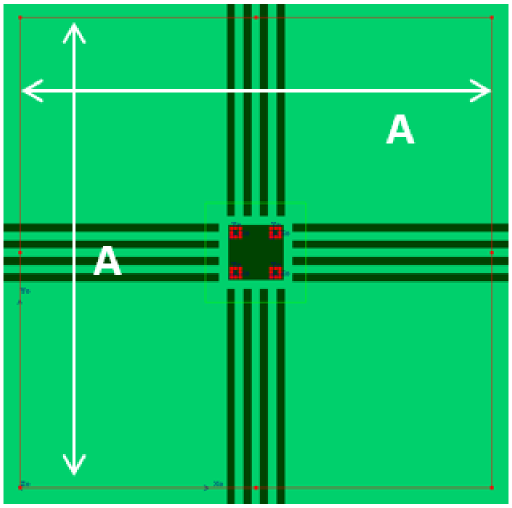


图 10-10. WQFN PCB model top layer

表 10-4. Dimension A for 16-pin RTE package

Cu area (cm^2)	Dimension A (mm)
2	14.14
4	20.00
8	28.28
16	40.00

10.1.1.3.3.1 Steady-State Thermal Performance

"Steady-state" conditions assume that the motor driver operates with a constant RMS current over a long period of time. The figures in this section show how $R_{\theta JA}$ and Ψ_{JB} (junction-to-board characterization parameter) change depending on copper area, copper thickness, and number of layers of the PCB. More copper area, more layers, and thicker copper planes decrease $R_{\theta JA}$ and Ψ_{JB}, which indicate better thermal performance from the PCB layout.

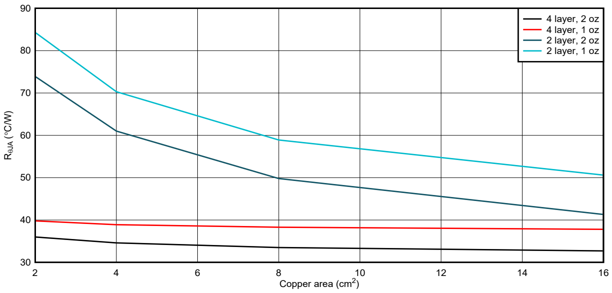


图 10-11. HTSSOP, PCB junction-to-ambient thermal resistance vs copper area

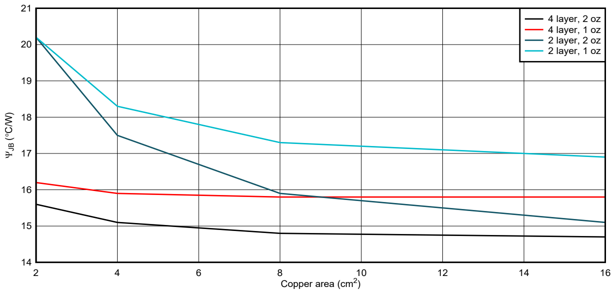


图 10-12. HTSSOP, junction-to-board characterization parameter vs copper area

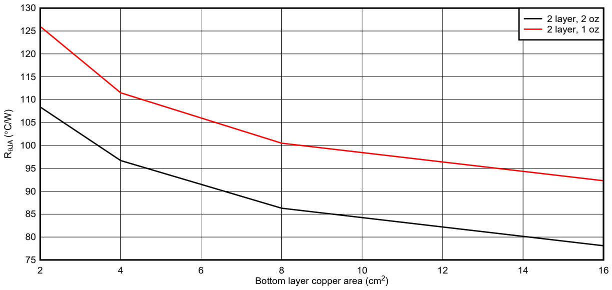


图 10-13. WQFN, PCB junction-to-ambient thermal resistance vs copper area

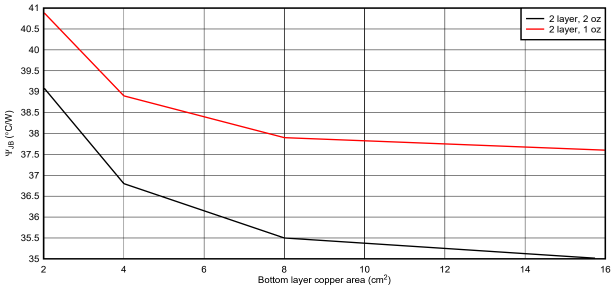


图 10-14. WQFN, junction-to-board characterization parameter vs copper area

10.1.1.3.3.2 Transient Thermal Performance

The motor driver may experience different transient driving conditions that cause large currents to flow for a short duration of time. These may include -

- Motor start-up when the rotor is initially stationary.
- Fault conditions when there is a supply or ground short to one of the motor outputs, and the overcurrent protection triggers.
- Briefly energizing a motor or solenoid for a limited time, then de-energizing.

For these transient cases, the duration of drive time is another factor that impacts thermal performance in addition to copper area and thickness. In transient cases, the thermal impedance parameter $Z_{\theta JA}$ denotes the junction-to-ambient thermal performance. The figures in this section show the simulated thermal impedances for 1-oz and 2-oz copper layouts for the HTSSOP and WQFN packages. These graphs indicate better thermal performance with short current pulses. For short periods of drive time, the device die size and package dominates the thermal performance. For longer drive pulses, board layout has a more significant impact on thermal performance. Both graphs show the curves for thermal impedance split due to number of layers and copper area as the duration of the drive pulse duration increases. Long pulses can be considered steady-state performance.

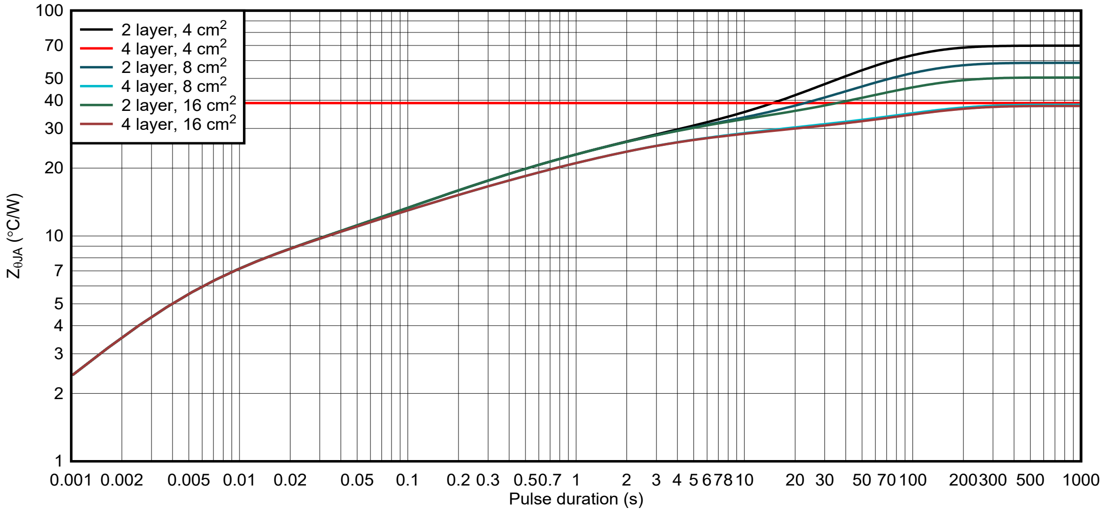


图 10-15. HTSSOP package junction-to-ambient thermal impedance for 1-oz copper layouts

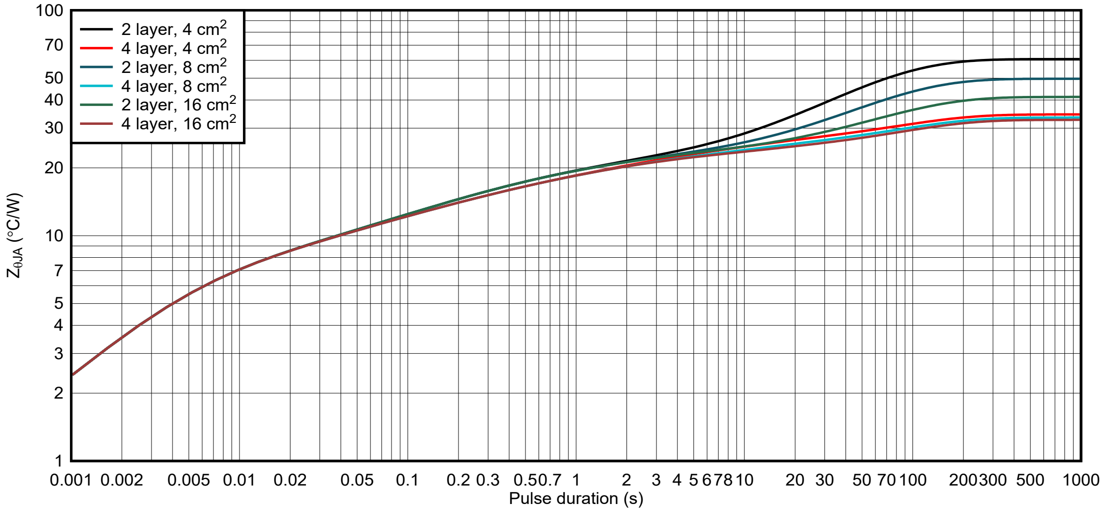


图 10-16. HTSSOP package junction-to-ambient thermal impedance for 2-oz copper layouts

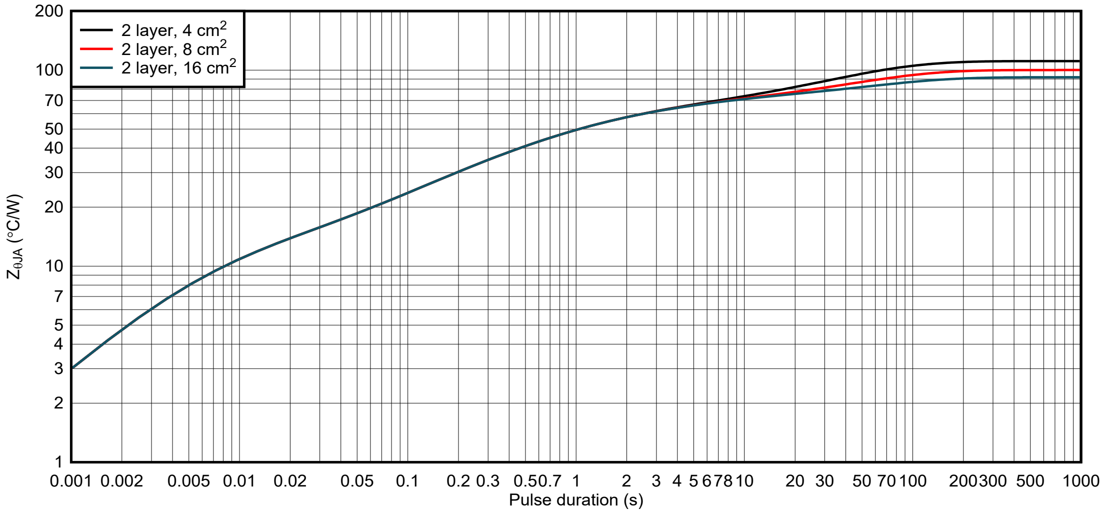


图 10-17. WQFN package junction-to-ambient thermal impedance for 1-oz copper layouts

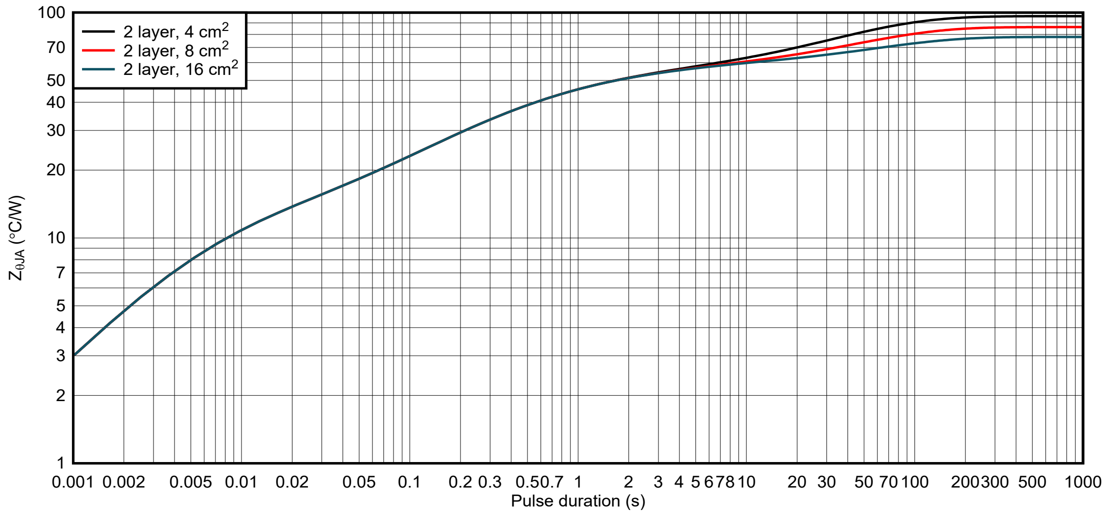


图 10-18. WQFN package junction-to-ambient thermal impedance for 2-oz copper layouts

10.1.1.4 Multi-Sourcing with Standard Motor Driver Pinout

The devices come in industry standard package footprints in the PWP and RTE packages.

As shown in 节 5, the DRV8410/11/11A devices are pin-to-pin compatible with the DRV8833 and DRV8833C. Many drivers from other suppliers have footprints similar to DRV8833 and DRV8833C.

- When replacing a device similar to DRV8833, user should remove the capacitors for the internal regulator (VINT) and the charge pump (VCP) by setting them as DNP (do not place) in the design files.
- The internal voltage reference for current regulation is 200 mV, just like the DRV8833 and DRV8833C. Because the voltage reference is the same, the system can still use the same xISEN resistor values designed for DRV8833 or other second source drivers with the same pinout.
- DRV841xPWP can use the same footprint as DRV8833 and DRV8833C in the HTSSOP package as shown in 图 10-19 and 图 10-20.
- DRV841xRTE are only footprint compatible with DRV8833C and other suppliers in the 3 mm x 3 mm QFN package.

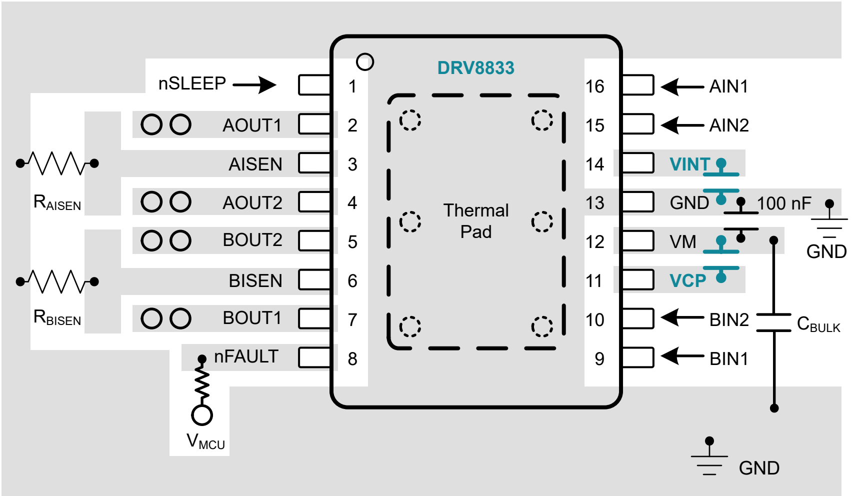


图 10-19. DRV8833 Layout Example

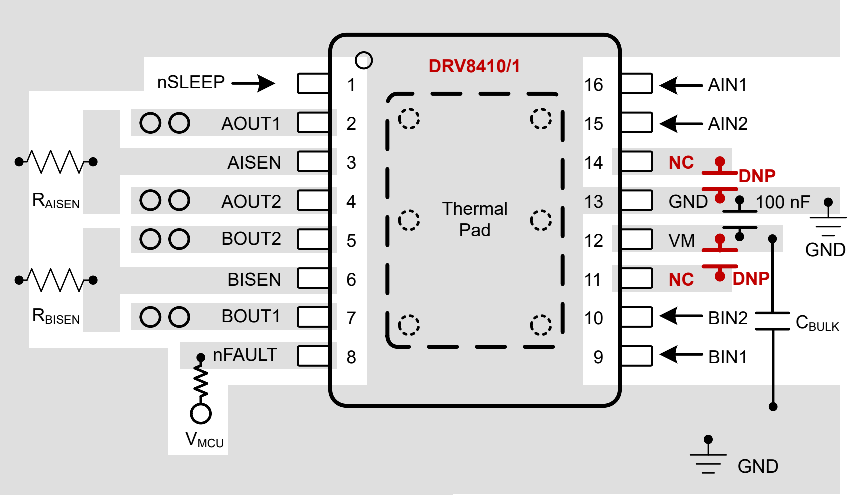


图 10-20. DRV8410/1 Footprint Compatible Layout Example

11 Power Supply Recommendations

11.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

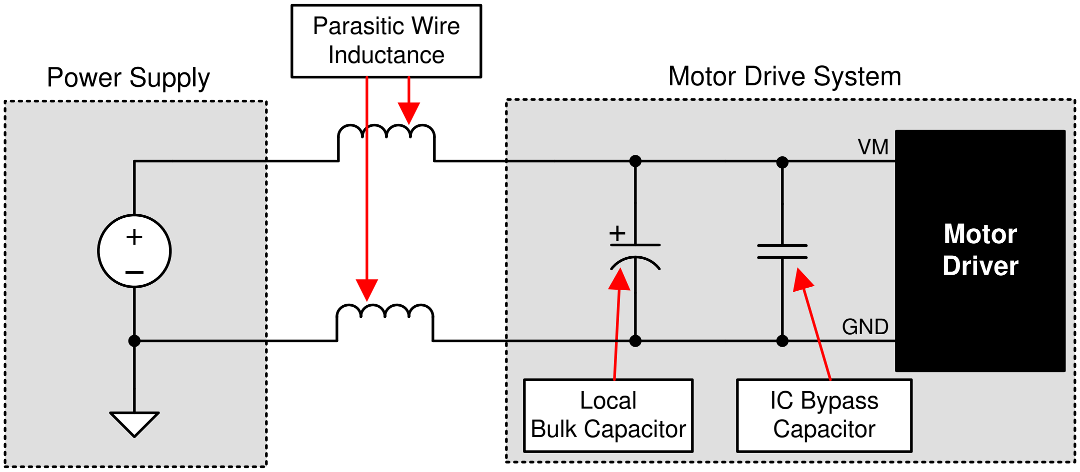


图 11-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

11.2 Power Supply and Logic Sequencing

There is no specific sequence for powering up the DRV8410. The presence of digital input signals is acceptable before VM is applied. After VM is applied to the DRV8410, the device begins operation based on the status of the control pins.

12 Layout

12.1 Layout Guidelines

Since the DRV8410 device has integrated power MOSFETs capable of driving high current, careful attention should be paid to the layout design and external component placement. Some design and layout guidelines are provided below. For more information on layout recommendations, please see the application note *Best Practices for Board Layout of Motor Drivers*.

- Low ESR ceramic capacitors should be utilized for the VM-to-GND. X5R and X7R types are recommended.
- The VM power supply capacitor should be placed as close to the device as possible to minimize the loop inductance.
- The VM power supply bulk capacitor can be of ceramic or electrolytic type, but should also be placed as close as possible to the device to minimize the loop inductance.
- VM, xOUTx, and GND pins carry the high current from the power supply to the outputs and back to ground. Thick metal routing should be utilized for these traces as is feasible.
- GND should connect directly on the PCB ground plane.
- The device thermal pad should be attached to the PCB top layer ground plane and internal ground plane (when available) through thermal vias to maximize the PCB heat sinking.
- The copper plane area attached to the thermal pad should be maximized to ensure optimal heat sinking.

12.2 Layout Example

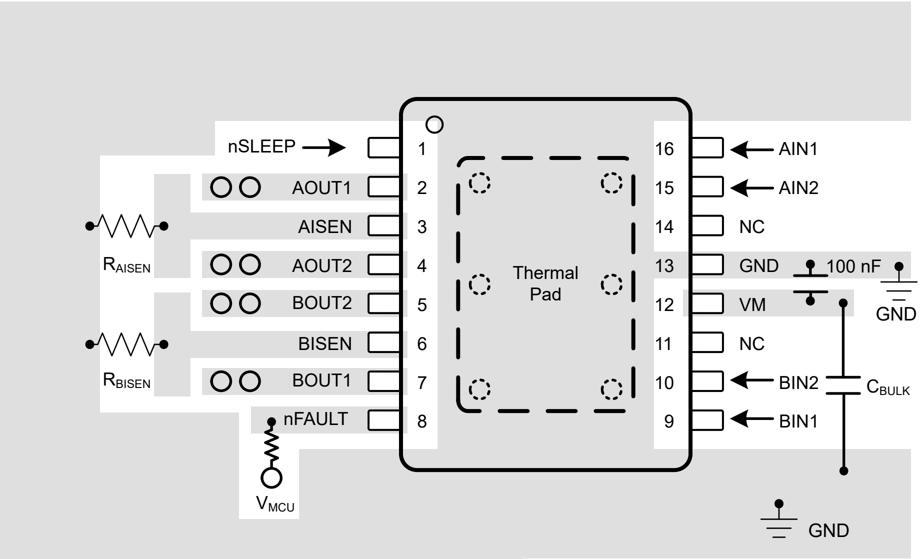


图 12-1. Recommended Layout Example for PWP (HTSSOP) Package

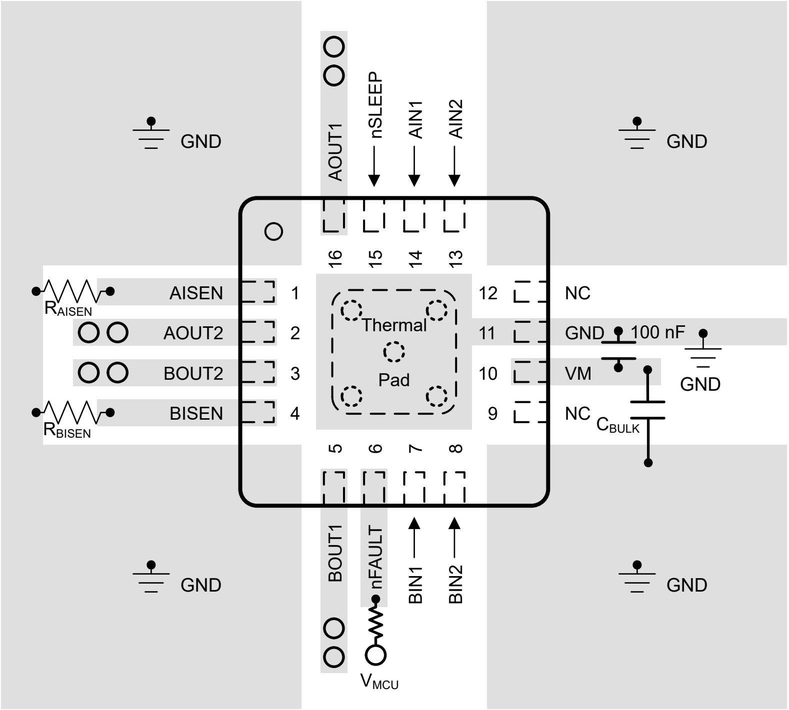


图 12-2. Recommended Layout Example for RTE (WQFN) Package

ADVANCE INFORMATION

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Calculating Motor Driver Power Dissipation* application report
- Texas Instruments, *PowerPAD™ Made Easy application report* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *Understanding Motor Driver Current Ratings* application report
- Texas Instruments, *Best Practices for Board Layout of Motor Drivers* application report

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need. Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

所有商标均为其各自所有者的财产。

14 Mechanical, Packaging, and Orderable Information

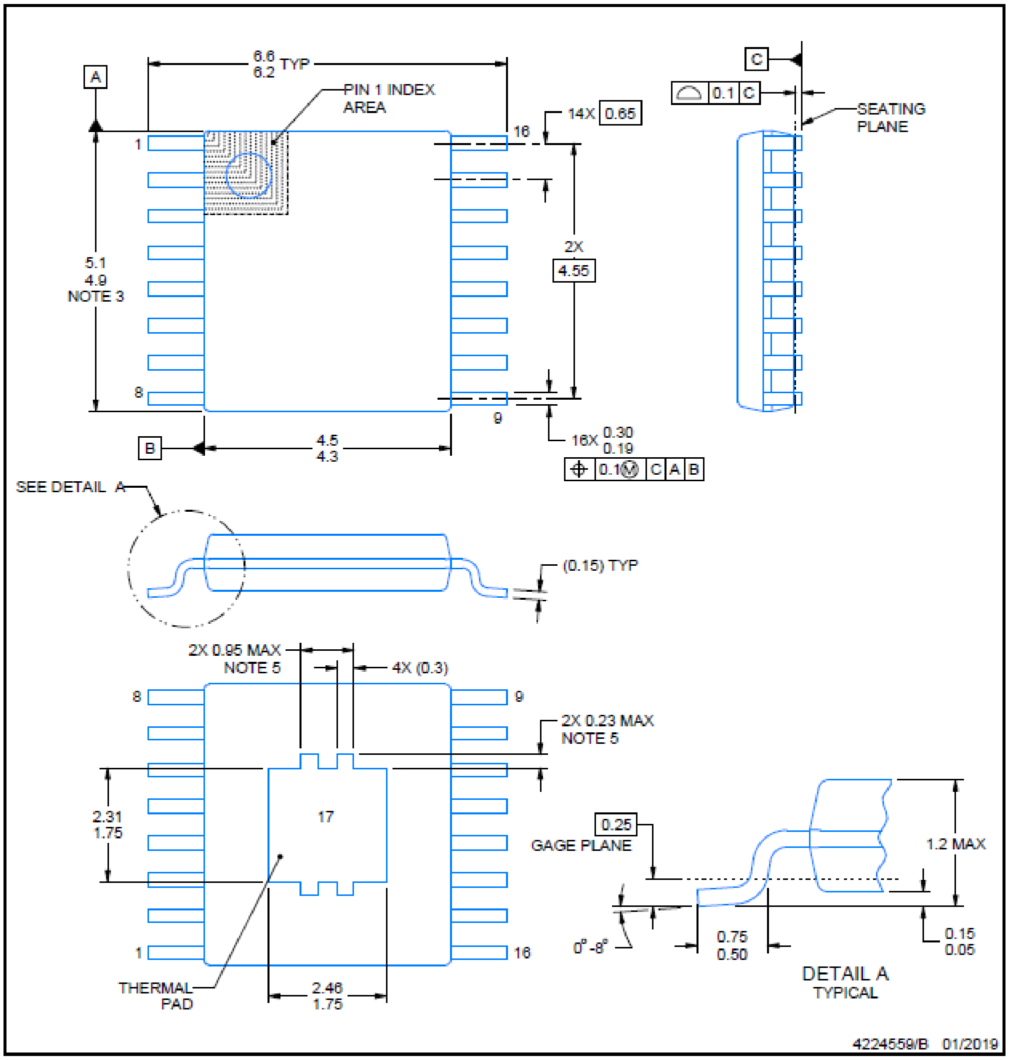
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

PWP0016C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

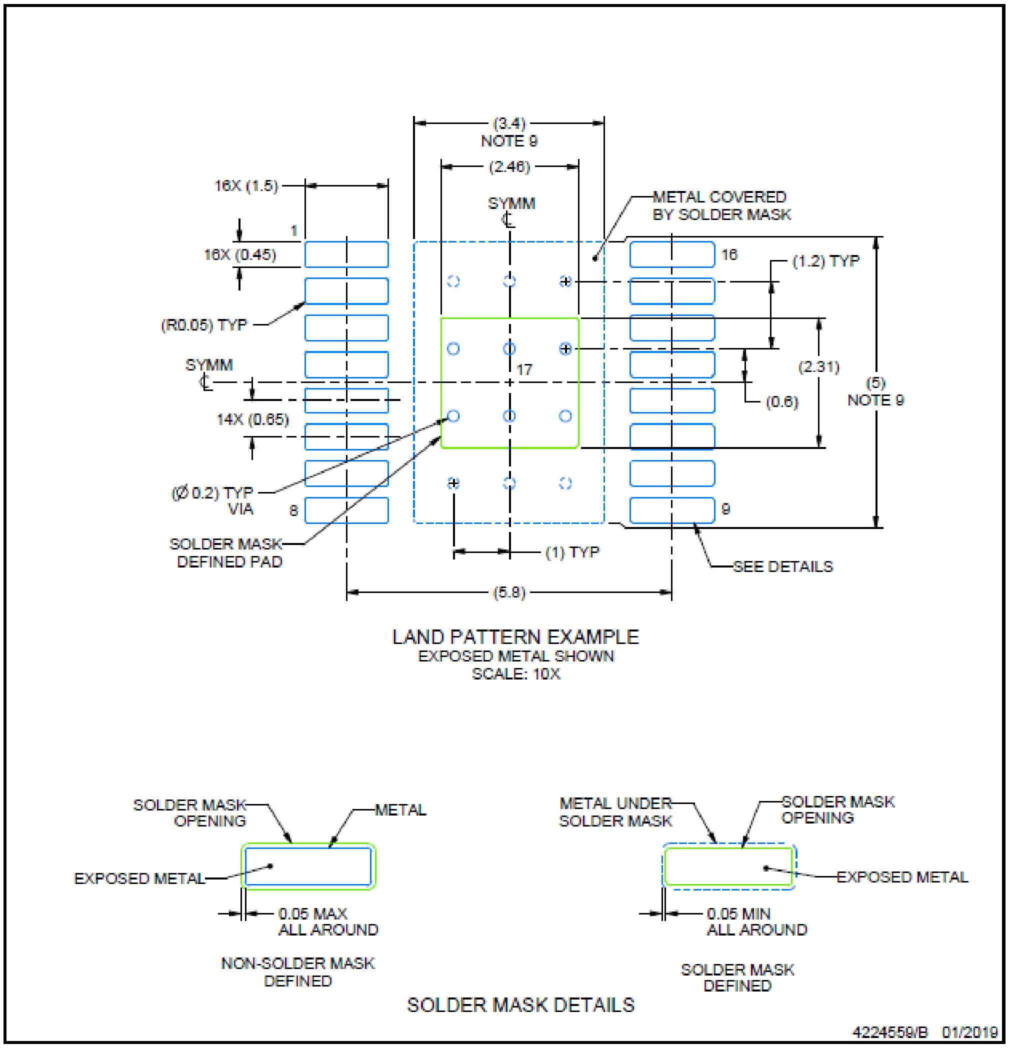
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

PWP0016C **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



NOTES: (continued)

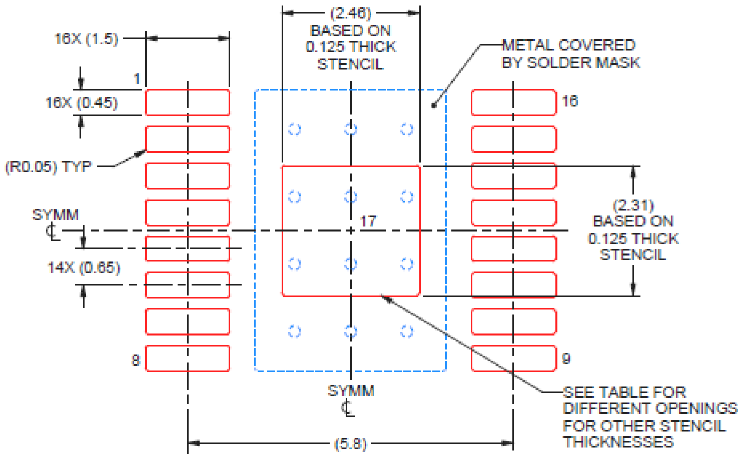
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0016C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

4224559/B 01/2019

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

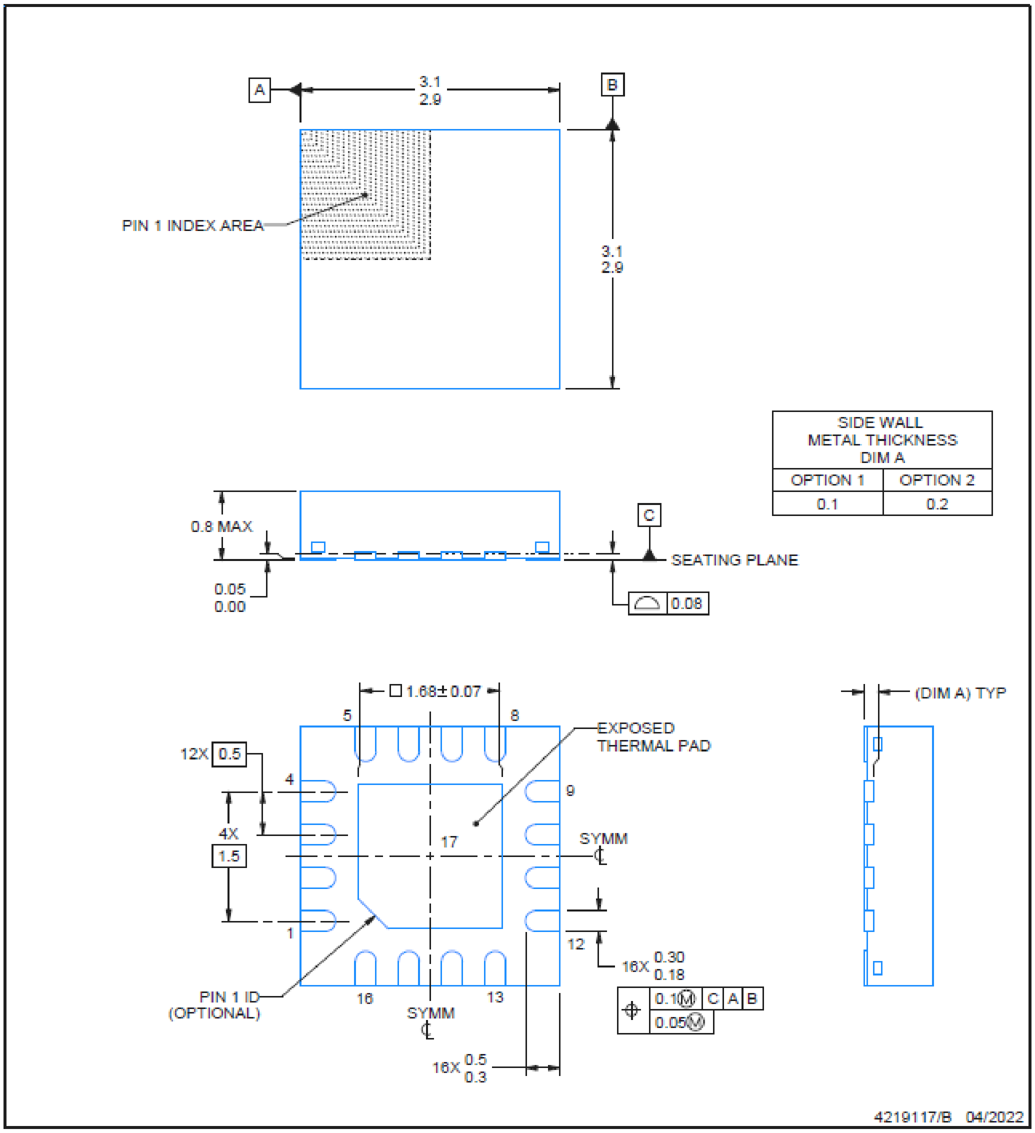
ADVANCE INFORMATION

PACKAGE OUTLINE

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



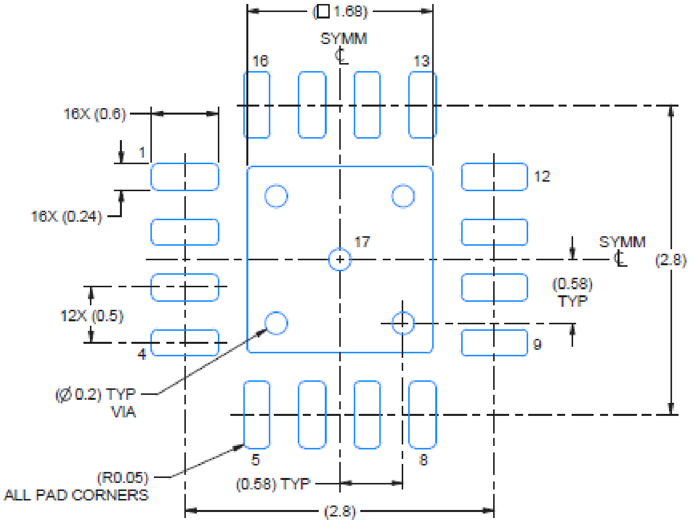
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

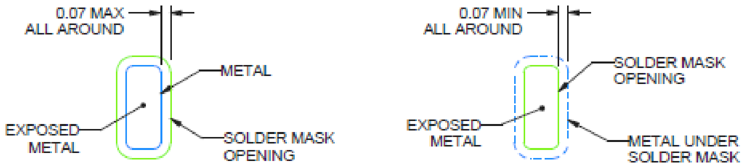
EXAMPLE BOARD LAYOUT

RTE0016C **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

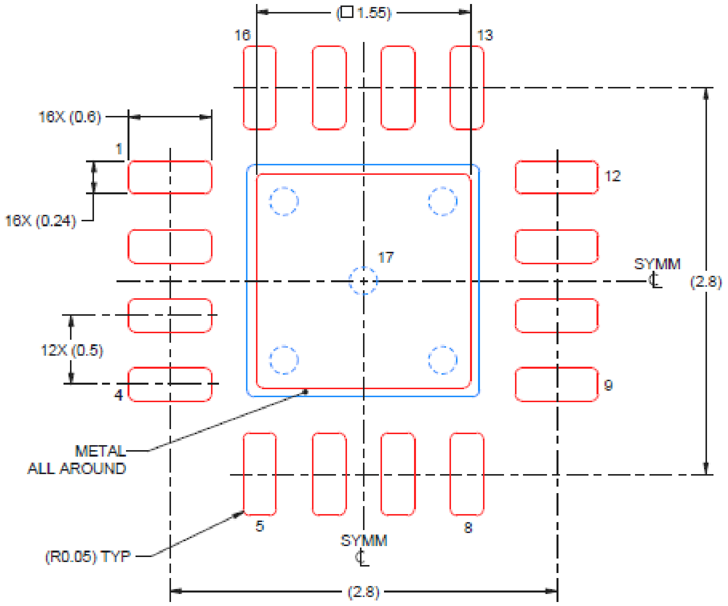
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RTE0016C **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

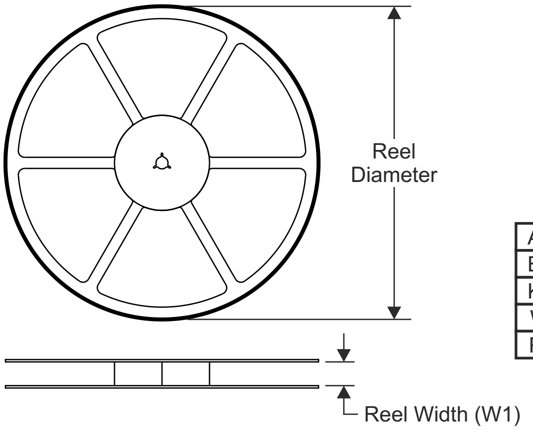
4219117/B 04/2022

NOTES: (continued)

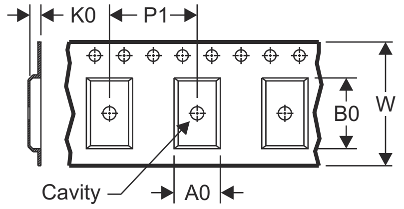
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

14.1 Tape and Reel Information

REEL DIMENSIONS

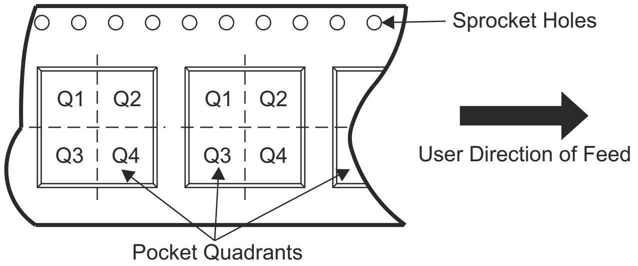


TAPE DIMENSIONS



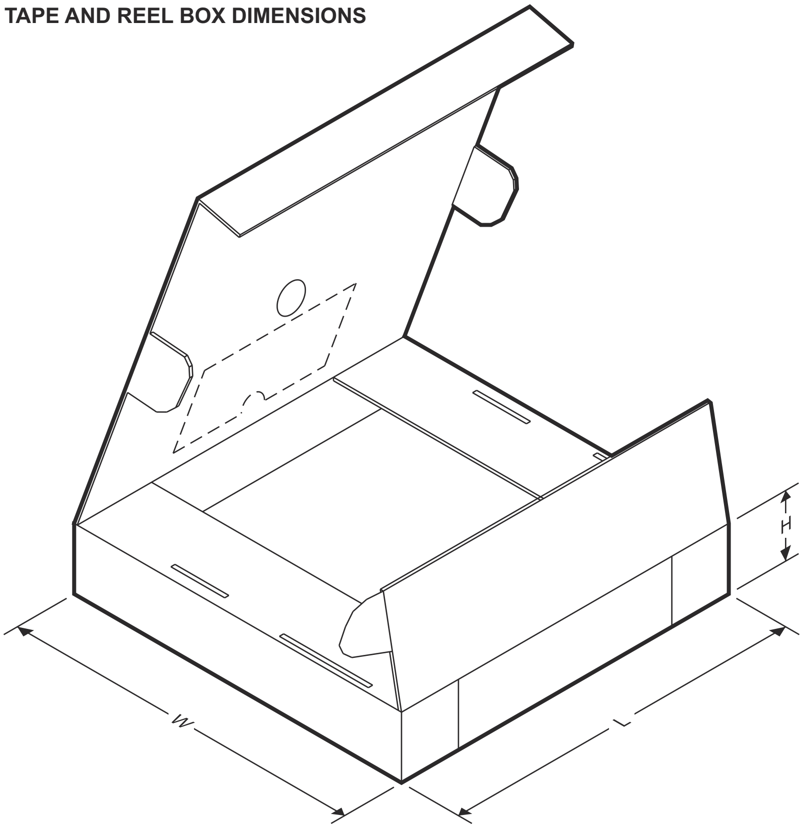
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8410	HTSSOP	PWP	16	3000	330	12.4	6.9	5.6	1.6	8	12	Q1
DRV8410	WQFN	RTE	16	5000	330	12.4	3.3	3.3	1.1	8	12	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8410	HTSSOP	PWP	16	3000	356	356	35
DRV8410	WQFN	RTE	16	5000	367	367	35

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265