DS90CR485 133-MHz, 48-Bit Channel Link Serializer (6.384 Gbps)

1 Features

- Up to 6.384-Gbps Throughput
- 66-MHz to 133-MHz Input Clock Support
- Reduces Cable and Connector Size and Cost
- Pre-Emphasis Reduces Cable Loading Effects
- DC Balance Reduces ISI Distortion
- 24-Bit Double Edge Inputs
- 3-V Tolerant LVCMOS/LVTTL Inputs
- Low Power, 2.5-V Supply
- Flow-Through Pinout
- 100-Pin TQFP Package
- Conforms With TIA/EIA-644-A LVDS Standard

2 Applications

- Backplane
- Cable Interconnect

3 Description

The DS90CR485 device serializes the 24 LVCMOS/LVTTL double-edge inputs (48 bits data latched in per clock cycle) onto eight Low Voltage Differential Signaling (LVDS) streams. A phase-locked transmit clock is also in parallel with the data streams over a 9th LVDS link. The reduction of the wide TTL bus to a few LVDS lines reduces cable and connector size and cost. The double-edge input strobes data on both the rising and falling edges of the clock. This minimizes the pin count required and simplifies PCB routing between the host chip and the serializer.

This chip can help resolve EMI and interconnect size problems for high throughput point-to-point applications.

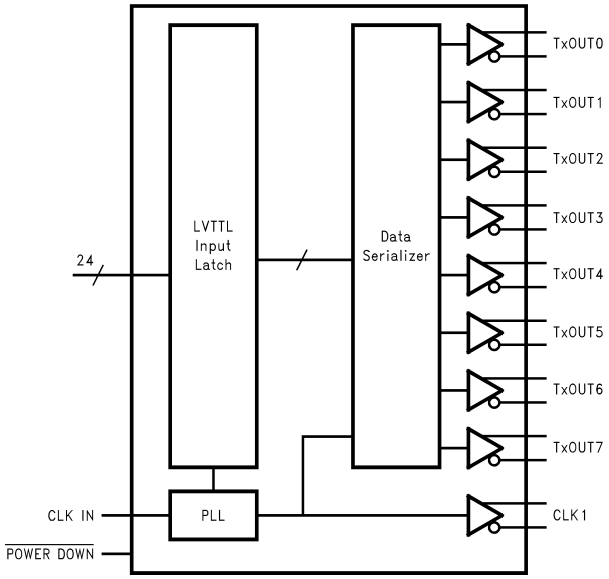
The DS90CR485 is compatible with the DS90CR486 Channel-Link receiver. The device is also backward-compatible with other Channel-Link receivers such as the DS90CR482 and DS90CR484.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS90CR485	TQFP (100)	14.00 mm × 14.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Generalized Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

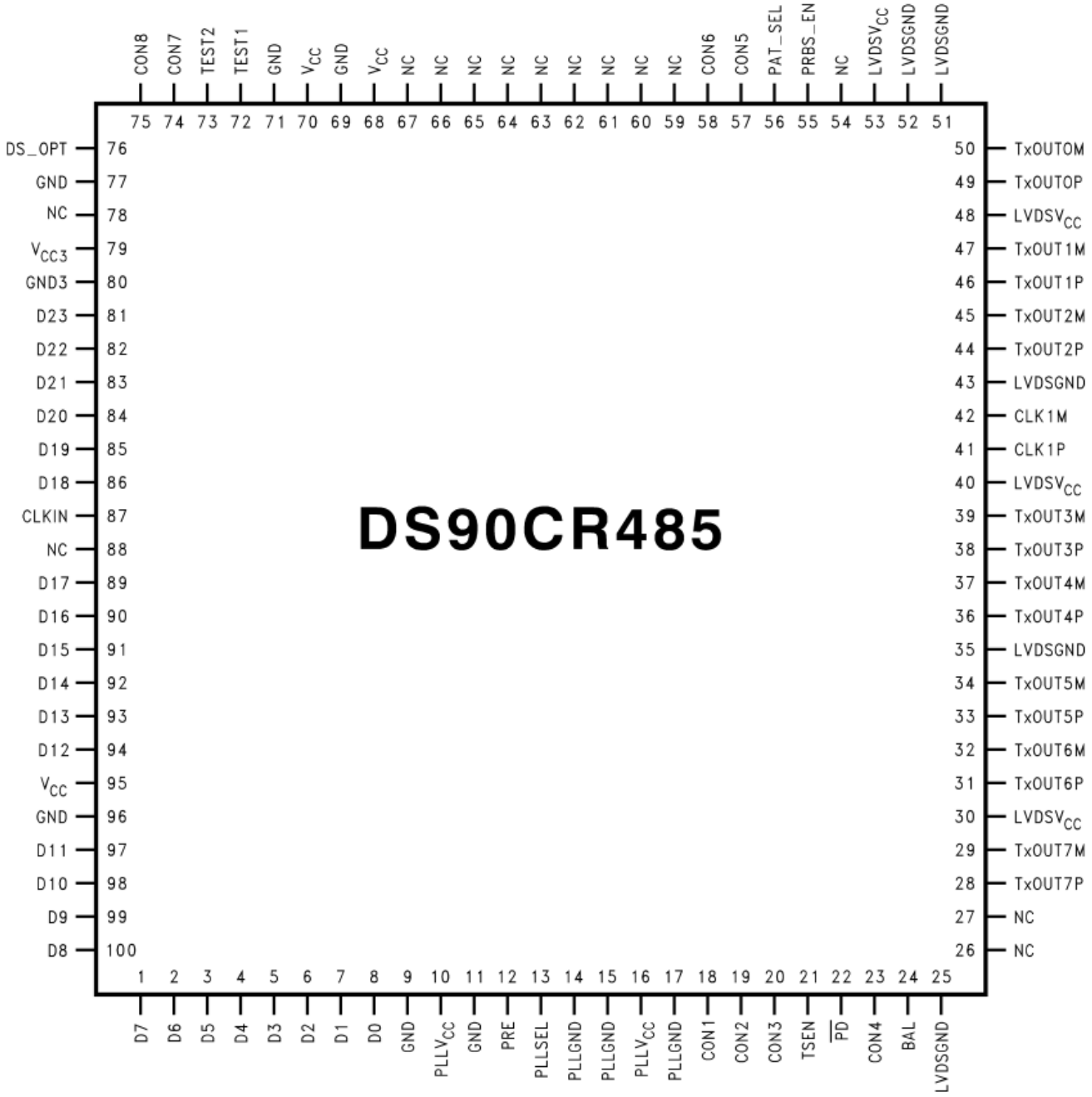
- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed pinout and *Pin Functions* table ... 3
- Moved ESD ratings to *ESD Ratings* table ... 7

Changes from Revision C (March 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 1

5 Pin Configuration and Functions

NEZ Package
100-Pin TQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BAL	24	I	LVCMOS/LVTTL level single-ended inputs. TTL level input. Tied this pin to Vcc to enable DC Balance function. When tied low or left open, the DC Balance function is disabled. Refer to the *Application and Implementation* on the back for more information. See Figure 9 and Figure 10. 3 V tolerant when V_{CC3V} = 3.3 V.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
CLK1P	41	O	Positive LVDS differential clock output.
CLK1M	42	O	Negative LVDS differential clock output.
CLKIN	87	I	LVCMOS/LVTTL level clock input. Samples data on both edges. See Figure 5 and Figure 9. 3 V tolerant when V_{CC3V} = 3.3 V.
CON1	18	I	Control pin. This pin is reserved for future use. Tied to Low or NC.
CON2	19	I	Control pin. **This pin must be tied High or pulled to high for normal operation** Tied to Low for internal BIST function only. Do not float. 3V tolerant when V_{CC3V} = 3.3 V.
CON3	20	I	Control pin. **This pin must be tied Low to configure the device for specific operation.** Tied to High or floating is reserved for future use.
CON4	23	I	Control pin. When tied High, all eight LVDS output channels (A0-A7) are enabled. Tied to Low will disable LVDS output channels A4-A7. Must tie High for standard operation. 3 V tolerant when V_{CC3V} = 3.3 V.
CON5	57	I	Control pins. Tied to Low for normal operation.
CON6	58	I	Control pins. Tied to Low for normal operation.
CON7	74	I	Control pins. Tied to Low for normal operation.
CON8	75	I	Control pins. Tied to Low for normal operation.
D0	8	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D1	7	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D2	6	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D3	5	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D4	4	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D5	3	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D6	2	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D7	1	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D8	100	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D9	99	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D10	98	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D11	97	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D12	94	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D13	93	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D14	92	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D15	91	I	LVCMOS/LVTTL level single-ended inputs. 3V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D16	90	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D17	89	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
D18	86	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D19	85	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D20	84	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D21	83	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D22	82	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
D23	81	I	LVCMOS/LVTTL level single-ended inputs. 3 V tolerant when V_{CC3V} = 3.3 V. Note, external pulldown resistor of 1 kΩ is required on all unused input data pins.
DS_OPT	76	I	LVCMOS/LVTTL level single-ended inputs. Cable Deskew performed when TTL level input is low. No TxIN data is sampled during Deskew. To perform Deskew function, input must be held low for a minimum of 4096 clock cycles. The Deskew operation is normally conducted after the TX and RX PLLs have locked. It should also be conducted after a system reset, or a reconfiguration event. Refer to the *Application and Implementation* section in back of this datasheet for more information. 3 V tolerant when V_{CC3V} = 3.3 V.
GND	9	G	Ground pins for 2.5-V power supply.
	11		
	69		
	71		
	96		
GND_{3V}	80	G	Ground pin for 3.3-V power supply.
LVDSGND	25	G	Ground pins for LVDS outputs.
	35		
	43		
	51		
	52		
$LVDSV_{CC}$	30	P	Power supply pins for LVDS outputs. Connect to 2.5-V power supply.
	40		
	48		
	53		
NC	26	—	No connect. Make NO Connection to these pins - leave open.
	27		
	54		
	59		
	60		
	61		
	62		
	63		
	64		
	65		
	66		
	67		
	78		
	88		
PAT_SEL	56	I	PRBS-23 or PRBS-15 mode selection pin. PRBS-23 mode is enabled when this pin is tied High. Tie Low or float to enable PRBS-15 mode. 3 V tolerant when V_{CC3V} = 3.3 V.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{PD}$	22	I	LVCMOS/LVTTL level input. $\overline{PD}$ = low activates the power-down function and minimizes power dissipation. 3 V tolerant when V_{CC3V} = 3.3 V. (1)
PLLGND	14	G	Ground pins for PLL circuitry.
	15		
	17		
PLLSEL	13	I	LVCMOS/LVTTL level single-ended inputs. Control input for PLL range select. This pin must be tied to V_{CC} for 66-MHz to 133-MHz operation. No connect or tied to low is reserved for future use. 3 V tolerant when V_{CC3V} = 3.3 V. (1)
$PLLV_{CC}$	16	P	Power supply pins for PLL circuitry. Connect to 2.5-V power supply.
	10		
PRBS_EN	55	I	PRBS generator enable pin. The Pseudo Random Binary Sequence (PRBS) generator is enable when this pin is tied High. Tie Low or float to disable the PRBS generator. 3 V tolerant when V_{CC3V} = 3.3 V.
PRE	12	I	LVCMOS/LVTTL level single-ended inputs. Pre-emphasis level select. Pre-emphasis is active when input is tied to V_{CC} through external pullup resistor. Resistor value determines pre-emphasis level (see table in *Application and Implementation* section). For normal LVDS levels (no pre-emphasis), leave this pin open (do not tie to ground). 3 V tolerant when V_{CC3V} = 3.3 V.
TEST1	72	I	This pin should be tied low or left open. Tied to high (V_{CC}) or pulled to high (V_{CC}) is reserved for future use. (1)
TEST2	73	I	This pin should be tied low or left open. Tied to high (V_{CC}) or pulled to high (V_{CC}) is reserved for future use. (1)
TSEN	21	O	Termination Sense pin. The logic state output of this pin reports the presence of a remote termination resistor. TSEN is LOW when NO termination has been detected. TSEN is HIGH when a termination of 100 Ω has been detected. Note, TSEN pin is an open-collector output, an external pullup resistor of 1 kΩ is required for the TSEN pin to function.
TxOUT0M	50	O	Negative LVDS differential data output.
TxOUT0P	49	O	Positive LVDS differential data output.
TxOUT1M	47	O	Negative LVDS differential data output.
TxOUT1P	46	O	Positive LVDS differential data output.
TxOUT2M	45	O	Negative LVDS differential data output.
TxOUT2P	44	O	Positive LVDS differential data output.
TxOUT3M	39	O	Negative LVDS differential data output.
TxOUT3P	38	O	Positive LVDS differential data output.
TxOUT4M	37	O	Negative LVDS differential data output.
TxOUT4P	36	O	Positive LVDS differential data output.
TxOUT5M	34	O	Negative LVDS differential data output.
TxOUT5P	33	O	Positive LVDS differential data output.
TxOUT6M	32	O	Negative LVDS differential data output.
TxOUT6P	31	O	Positive LVDS differential data output.
TxOUT7M	29	O	Negative LVDS differential data output.
TxOUT7P	28	O	Positive LVDS differential data output.
V_{CC}	68	P	2.5-V Power supply pins for core logic.
	70		
	95		
V_{CC3V}	79	P	3.3-V Power supply pin for 3-V tolerant input support. (2)

(1) Inputs default to “low” when left open due to internal pulldown resistor.
(2) V_{CC3V} pins must proceed power up before other V_{CC} pins. See *Application and Implementation* section for detail.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

		MIN	MAX	UNIT
Supply Voltage (V_{CC})		−0.2	2.7	V
Supply Voltage (V_{CC3})		−0.3	3.6	V
LVCMOS/LVTTL Input Voltage		−0.3	(V_{CC3} + 0.3)	V
LVDS Output Voltage		−0.3	(V_{CC} + 0.3)	V
LVDS Short Circuit Duration		Continuous		
Maximum Package Power Dissipation at 25°C	100 TQFP Package		2.9	W
	Derate TQFP Package	23.8mW/°C above +25°C		
Lead Temperature (Soldering, 4 sec.)			260	°C
Junction Temperature			150	°C
Storage Temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Supply and GND pins	±1500	V
			I/O and Control Pins	±2000	
		EIAJ (0 Ω, 200 pF)		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply Voltage (V_{CC})	2.37	2.5	2.62	V
Supply Voltage (V_{CC3})	2.37	2.5/3.3	3.46	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Supply Noise Voltage			100	mV_{p-p}
Clock Rate	66		133	MHz

6.4 Thermal Information

THERMAL METRIC(1)		DS90CR485 NEZ (TQFP) 100 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics(1)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS/LVTTL DC SPECIFICATIONS (All input pins.)							
V_{IH}	High Level Input Voltage			2		V_{CC3}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.8	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4 V or V_{CC}			+1.8	+15	µA
		V_{IN} = GND		−15	0		µA
LVDS DC SPECIFICATIONS (All output pins TxOUTnP, TxOUTnM, CLKnP and CLKnM)							
V_{OD}	Differential Output Voltage	R_L = 100 Ω		250	345	450	mV
ΔV_{OD}	Change in V_{OD} Between Complimentary Output States					35	mV
V_{OS}	Offset Voltage			0.8	1.125	1.35	V
ΔV_{OS}	Change in V_{OS} Between Complimentary Output States					35	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V, R_L = 100 Ω			−3.5	−15	mA
I_{OZ}	Output TRI-STATE Current	$\overline{PD}$ = 0 V, OUTM = OUTP = 0 V or V_{CC}			±1	±10	µA
SUPPLY CURRENT							
I_{CCTW}	2.5-V Supply Current Worst Case	R_L = 100 Ω, C_L = 5 pF, Worst Case Pattern, 100% Pre-emphasis BAL = Low, Figure 1	f = 66 MHz		160	230	mA
			f = 100 MHz		180	270	mA
			f = 133 MHz		210	310	mA
	3.3-V Supply Current Worst Case	R_L = 100 Ω, C_L = 5 pF, Worst Case Pattern, No Pre-emphasis BAL = Low, Figure 1,			68	105	µA
I_{CCTZ}	Supply Current Power Down	$\overline{PD}$ = Low			5	50	µA

(1) Typical values are given for V_{CC} = 2.5 V and T_A = +25°C.

6.6 Recommended Input Requirements

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER			MIN	TYP(1)	MAX	UNIT
TCIP	TxCLK IN Period (Figure 4)		7.52	T	15.15	ns
TCIH	TxCLK in High Time (Figure 4)		0.35T	0.5T	0.65T	ns
TCIL	TxCLK in Low Time (Figure 4)		0.35T	0.5T	0.65T	ns
TCIT	TxCLK IN Transition Time (Figure 3)	66 MHz	0.5		2.4	ns
		133 MHz	0.5		1.2	ns
TXIT	D0 to D23 Transition Time	66 MHz	0.5		2.9	ns
		133 MHz	0.5		1.75	ns

(1) Typical values are given for V_{CC} = 2.5 V and T_A = +25°C.

6.7 Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1)

PARAMETER		MIN	TYP	MAX	UNIT
LLHT	LVDS Low-to-High Transition Time (No pre-emphasis, PRE = open) (Figure 2) (2)		0.2	0.4	ns
	LVDS Low-to-High Transition Time (maximum pre-emphasis, PRE = V_{CC}) (Figure 2) (2)		0.12	0.2	ns

(1) Typical values are given for V_{CC} = 2.5 V and T_A = +25°C.
(2) LLHT and LHLT are measurements of transmitter LVDS data outputs rise and fall time over the recommended frequency range. The limits are based on bench characterization and Specified By Design (SBD) using statistical analysis.

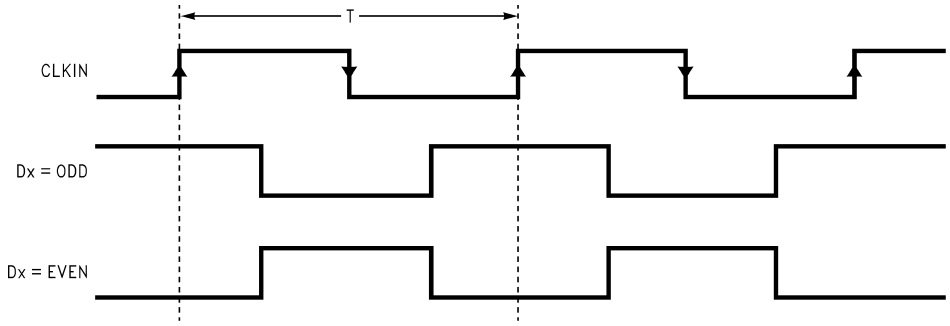
Switching Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1)

PARAMETER			MIN	TYP	MAX	UNIT
LHLT	LVDS High-to-Low Transition Time (No pre-emphasis, PRE = open) (Figure 2) (2)			0.19	0.4	ns
	LVDS High-to-Low Transition Time (maximum pre-emphasis, PRE = V_{CC}) (Figure 2) (2)			0.1	0.2	ns
TCCS	TxOUT Channel-to-Channel Skew			20		ps
TPPOS	Transmitter Output Pulse Position. (3)	f = 133 MHz	−100		+100	ps
		f = 100 MHz	−150		+150	ps
		f = 66 MHz	−200		+ 200	ps
TSTC	TxIN Setup to CLKIN at 133 MHz (4), (Figure 5)		0.5			ns
THTC	CLKIN to TxIN Hold at 133 MHz (4), (Figure 5)		0.5			ns
TJCC	Transmitter Jitter Cycle-to-Cycle (5)	f = 133 MHz		40	70	ps
		f = 100 MHz		45	80	ps
		f = 66 MHz		50	100	ps
BWPLL	PLL Bandwidth ≥ 66 MHz			600		kHz
TPLLS	Transmitter Phase Lock Loop Set (Figure 6)				10	ms
TPDD	Transmitter Power-down Delay (Figure 7)				100	ns
TPDL	Transmitter Input to Output Latency (Figure 8)		6(TCIP)	7(TCIP)	8(TCIP)	ns

(3) TPPOS is a measure of transmitter output pulse position in comparison with the ideal pulse position over the recommended frequency range. The limits are based on bench characterization and Specified By Design (SBD) using statistical analysis.
(4) TSTC and THTC are measurements of transmitter data inputs setup and hold time with clock input, CLKIN. The limits are based on bench characterization and Specified By Design (SBD) using statistical analysis.
(5) The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of ±10% at a 1-µs rate applied to the transmitter's input clock signal (CLKIN) while data inputs are switching with internal PRBS generator enabled without DC-Balance. The typical data is measured with a cycle-to-cycle jitter of ±100 ps applied to the transmitter's input clock signal (CLKIN).

6.8 AC Timing Diagrams



The worst case test pattern produces a maximum toggling of digital circuits, LVCMOS/LVTTL I/O.

Figure 1. "Worst Case" Test Pattern

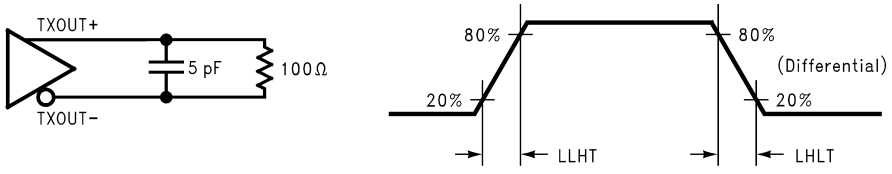


Figure 2. LVDS Output Load and Transition Times

AC Timing Diagrams (continued)

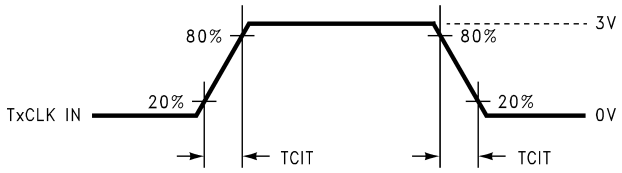


Figure 3. Input Clock Transition Time

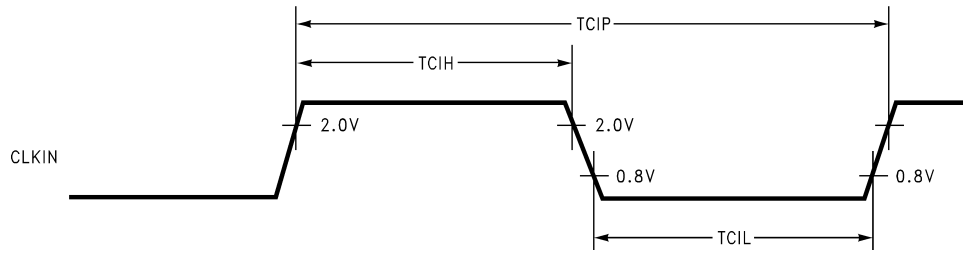


Figure 4. Input Clock High/Low Times

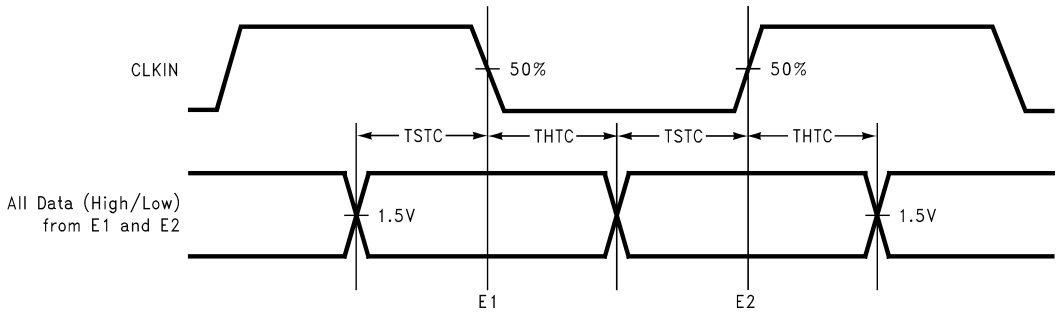


Figure 5. Setup/Hold With CLKIN

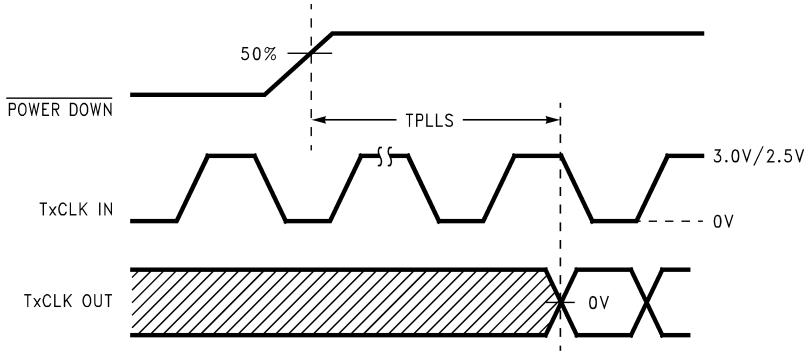


Figure 6. Phase Lock Loop Set Time (V_{CC} ≥ 2.37 V)

AC Timing Diagrams (continued)

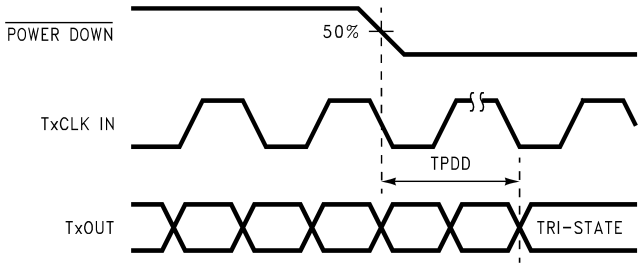


Figure 7. Power Down Delay

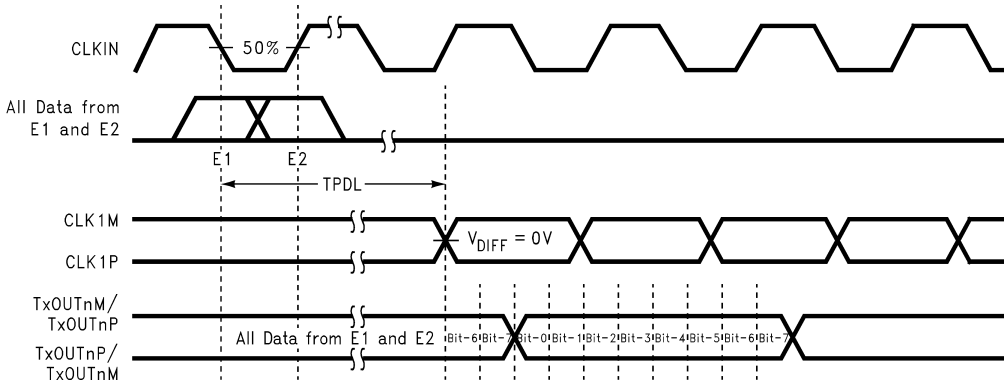


Figure 8. Input to Output Latency

6.9 LVDS Interface

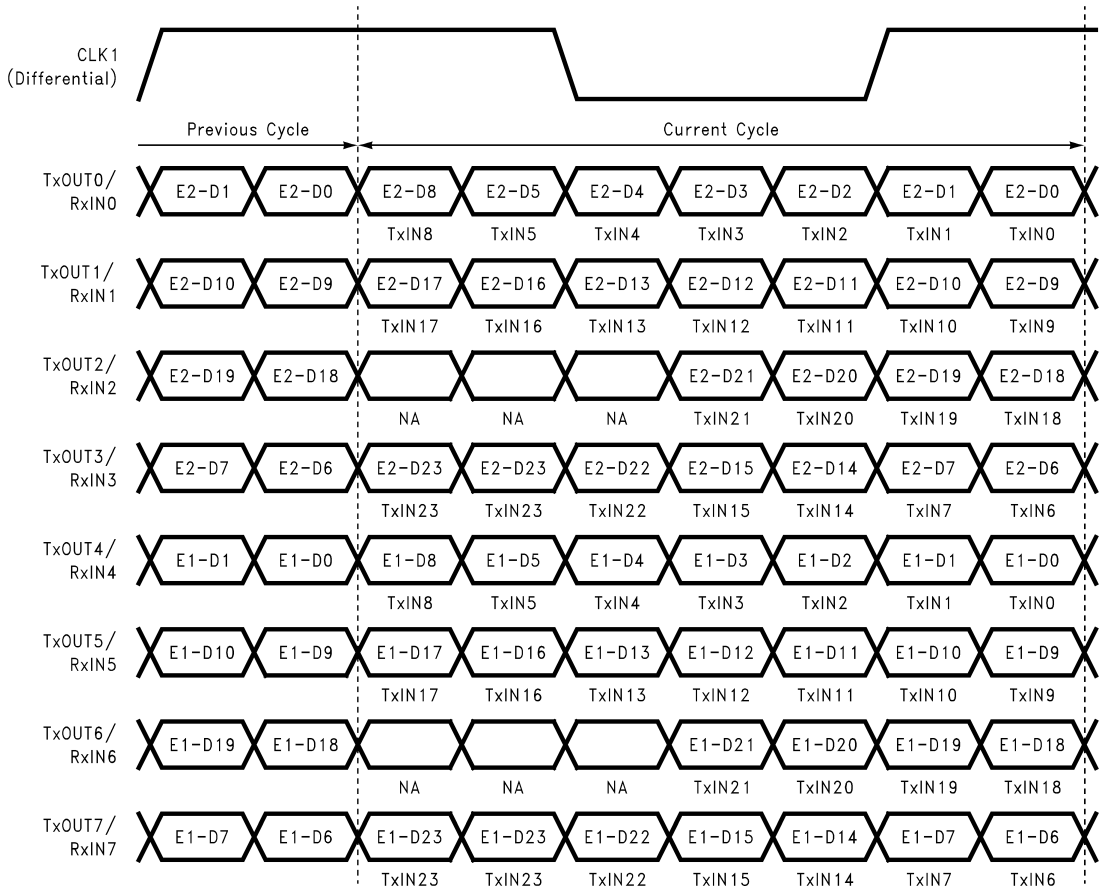


Figure 9. 48 LVCMOS/LVTLL Inputs Mapped to 8 LVDS Outputs (DC Balance Mode- Disabled; BAL = Low) (E1 - Falling Edge; E2 - Rising Edge)

LVDS Interface (continued)

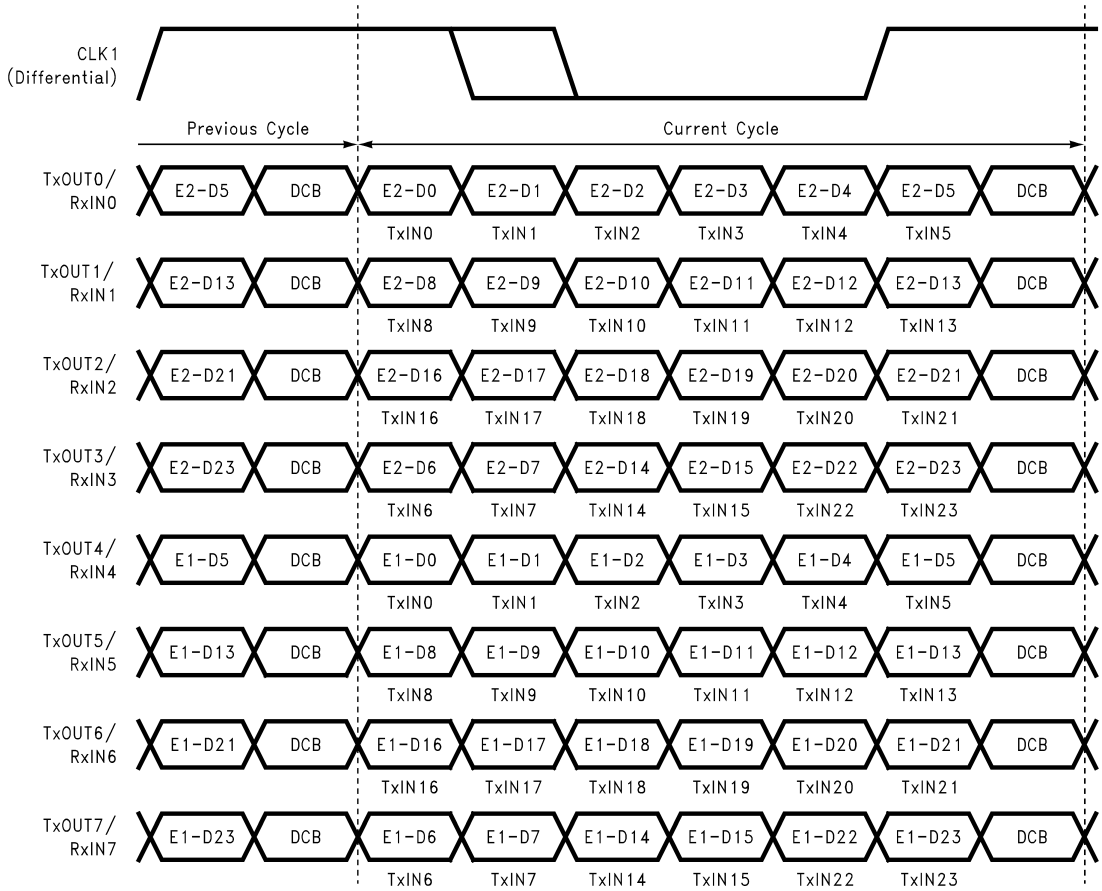


Figure 10. 48 LVCMOS/LVTLL Inputs Mapped to 8 LVDS Outputs (DC Balance Mode- Enabled; BAL = High) (E1 - Falling Edge; E2 - Rising Edge)

Table 1. DS90CR483 Inputs Mapped to DS90CR485 Inputs

DS90CR483 Tx Input	DS90CR485 Tx Input(1)	DS90CR485 Strobe Edge
TxIN0	D0	E2
TxIN1	D1	E2
TxIN2	D2	E2
TxIN3	D3	E2
TxIN4	D4	E2
TxIN5	D5	E2
TxIN6	D6	E2
TxIN7	D7	E2
TxIN8	D8	E2
TxIN9	D9	E2
TxIN10	D10	E2
TxIN11	D11	E2
TxIN12	D12	E2
TxIN13	D13	E2
TxIN14	D14	E2

(1) E1 Falling and E2 Rising

LVDS Interface (continued)

Table 1. DS90CR483 Inputs Mapped to DS90CR485 Inputs (continued)

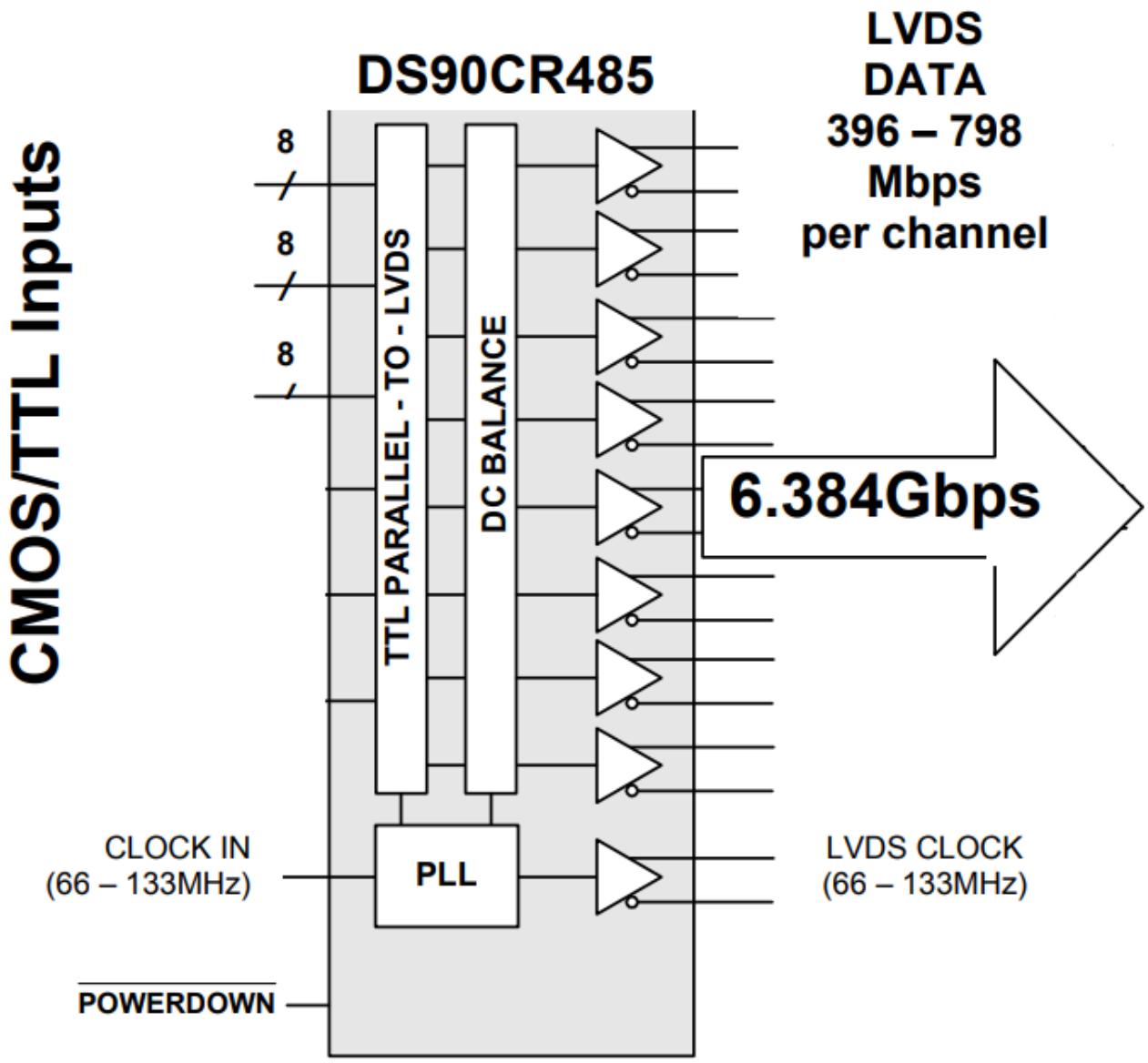
DS90CR483 Tx Input	DS90CR485 Tx Input(1)	DS90CR485 Strobe Edge
TxIN15	D15	E2
TxIN16	D16	E2
TxIN17	D17	E2
TxIN18	D18	E2
TxIN19	D19	E2
TxIN20	D20	E2
TxIN21	D21	E2
TxIN22	D22	E2
TxIN23	D23	E2
TxIN24	D0	E1
TxIN25	D1	E1
TxIN26	D2	E1
TxIN27	D3	E1
TxIN28	D4	E1
TxIN29	D5	E1
TxIN30	D6	E1
TxIN31	D7	E1
TxIN32	D8	E1
TxIN33	D9	E1
TxIN34	D10	E1
TxIN35	D11	E1
TxIN36	D12	E1
TxIN37	D13	E1
TxIN38	D14	E1
TxIN39	D15	E1
TxIN40	D16	E1
TxIN41	D17	E1
TxIN42	D18	E1
TxIN43	D19	E1
TxIN44	D20	E1
TxIN45	D21	E1
TxIN46	D22	E1
TxIN47	D23	E1

7 Detailed Description

7.1 Overview

The DS90CR485 serializes 24 LVCMOS/LVTTL double edge inputs (48 bits data latched in per clock cycle) onto 8 LVDS streams. A phase-locked clock is also transmitted in parallel with the data streams over a 9th LVDS pair. A receiver (like the DS90CR484 and DS90CR486) can be used to convert the 8 LVDS data streams plus clock back to 48 LVCMOS/LVTTL data bits plus clock.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pre-Emphasis

Adds extra current during LVDS logic transition to reduce cable loading effects. Pre-emphasis strength is set through a DC voltage level applied from min to max (0.75 V to V_{CC}) at the “PRE” pin. A higher input voltage on the ”PRE” pin increases the magnitude of dynamic current during data transition. The “PRE” pin requires one pullup resistor (Rpre) to V_{CC} to set the DC level. There is an internal resistor network, which causes a voltage drop. Refer to Table 2 on value of Rpre to set the voltage level.

Depending upon interconnect performance and clock rate, pre-emphasis, DC balance, and deskew enhancements allow cables 2 to 7 meters in length to be driven.

Table 2. Pre-Emphasis With (Rpre)

Rpre	Effects (Typ)
10kΩ or NC	Standard LVDS
3.5kΩ	12.5% pre-emphasis
1.75KΩ	25% pre-emphasis
900Ω	50% pre-emphasis
500Ω	75% pre-emphasis
50Ω	100% pre-emphasis

7.3.2 Information on Jitter Rejection

The transmitter is designed to reject cycle-to-cycle jitter which may be seen at the transmitter input clock. Very low cycle-to-cycle jitter is passed on to the transmitter outputs. Cycle-to-cycle jitter has been measured over frequency to be less than 100 ps with input step function jitter applied. This significantly reduces the impact of input clock source jitter and improves the accuracy of data sampling. Transmitter output jitter is effected by PLLVCC noise and input clock jitter. Minimize supply noise and use a low jitter clock source to limit output jitter.

7.3.3 DC Balance Mode

DC Balance mode is set when the BAL pin on the transmitter and receiver are tied HIGH - see *Pin Configuration and Functions*.

In addition to data information an additional bit is transmitted on every LVDS data signal line during each cycle as shown in Figure 10. This bit is the DC balance bit (BAL). The purpose of the DC Balance bit is to minimize the short- and long-term DC bias on the signal lines. This is achieved by selectively sending the data either unmodified or inverted.

The value of the DC balance bit is calculated from the running word disparity and the data disparity of the current word to be sent. The data disparity of the current word is calculated by subtracting the number of bits of value 0 from the number of bits value 1 in the current word. Initially, the running word disparity may be any value between +7 and −6. The running word disparity is the continuous sum of all the modified data disparity values, where the unmodified data disparity value is the calculated data disparity minus 1 if the data is sent unmodified and 1 plus the inverse of the calculated data disparity if the data is sent inverted. The value of the running word disparity saturates at +7 and −6 in DC balance mode. Refer to Table 3 for DC balance mode operation.

Table 3. DC Balance Mode

BAL	Running Word Disparity	Current Word Disparity	Data Sent Invert
0	X	X	NO
1	Positive	Negative/Zero	NO
1	Negative	Positive	NO
1	Positive	Positive	YES
1	Negative	Negative/Zero	YES
1	Zero	X	YES

7.3.4 TSEN

The TSEN pin reports the presence of a remote termination resistor to the local system. The TSEN pin is an open-collector output which requires an external pullup resistor of 1 kΩ at 2.5 V to function. The logic state output of this pin determines if there is termination on the far end of the LVDS clock channel. When TSEN is High, a termination of 100 Ω has been detected. When TSEN is Low, no termination has been detected indicating the likelihood that the cable is unplugged. This pin reports the line status to the local system.

7.3.5 BIST

To facilitate signal quality testing, an internal test pattern generator is provided on chip. This can be useful in checking signal quality (eye patterns) in the link. The internal BIST function is activated by driving the PRBS_EN pin High. There are two PRBS patterns available and the selections is control by the logic state of the PAT_SEL pin. When PAT_SEL is High, the transmitter generate and send out a PRBS-23 pattern. When PAT_SEL is low, a PRBS-15 pattern will be generated and sent. When PRBS_EN pin is Low, the logic state of the PAT_SEL pin will be ignored and the transmitter will operate as indicated by the other control and input pins. The transmitter's internally generated PRBS patterns are available for users to monitor signal quality via eye-diagrams. Depending upon external test equipment requirements, compatibility may or may not be possible.

7.3.6 Power-Up Sequence and 3-V Tolerant

The DS90CR485 inputs provide an option for 3.3 V tolerant. If this is required, the V_{CC3V} pin must be connected to a 3.3-V rail. Also when power is applied to the transmitter, V_{CC3V} pin must be applied before or simultaneously with other power supply pins (2.5 V). If 3.3-V tolerance is **not** required, this pin may be tied to the 2.5-V rail.

7.3.7 LVDS Output

This device features a modified LVDS output that provides an internal, 100-Ω termination at the source side of the link to control of reflections. An external termination resistor is required at the far end of the link and should be placed as close to the receiver inputs as possible to minimize any resulting stub length. Unused LVDS output channels should be terminated with 100 Ω at the transmitter's output pin.

7.3.8 Power Down

When the Power Down feature is asserted ($\overline{PD}$ = Low), the current draw through the supply pins is minimized and the PLL is shut down. The transmitter outputs are in TRI-STATE when in power-down mode. The $\overline{PD}$ pin should be driven HIGH to enable the device once V_{CC} is stable.

7.3.9 Deskew

The receiver will deskew or compensate the fixed interconnect skew between data signals, with respect to the rising edge of clock, on each of the independent differential pairs (pair-to-pair skew). For a list of deskew ranges, refer to the corresponding receiver data sheet for more information.

For the deskew function to work properly, it must be initialized or calibrated. The DS90CR486 deskew can be initialized with any data pattern with a transition over a period of three clock cycles. Therefore, there are multiple ways to initialize the deskew function depending on the setup configuration. For example, to initialize the operation of deskew for DS90CR485 and DS90CR486 in DC balance mode, the DS_OPT pin at the input of the transmitter DS90CR485 can be set High OR Low in power up. The period of this input to the DS_OPT pin must be at least 20 ms (TX and RX PLLs lock time) plus 4096 clock cycles for the receiver to complete the deskew operation. For other configuration setups with DS90CR483 and DS90CR484, refer to the flow chart in Figure 11.

The DS_OPT pin at the input of the transmitter (DS90CR485) is used to initiate the deskew calibration pattern. Depends on the configuration, it can be set High or Low in power up for the receiver to complete the deskew operation. For this reason, the LVDS clock signal with DS_OPT applied high (active data sampling) shall be 1111000 or 1110000 pattern and the LVDS data lines (TxOUT 0-7) shall be High for one clock cycle and Low for the next clock cycle. During the deskew operation with DS_OPT applied low, the LVDS clock signal shall be in a 1111100 or 1100000 pattern. The transmitter will also output a series of 1111000 or 1110000 onto the LVDS data lines (TxOUT 0-7) during deskew so that the receiver can automatically calibrate the data sampling strobes at the receiver inputs. Each data channel is deskewed independently and is tuned over a specific range. Refer to the corresponding receiver data sheet for a list of deskew ranges.

Note that the deskew initialization must be performed at least once after the PLL has locked to the input clock frequency, and it must be done at the time when the receiver is powered up and PLL has locked. If power is lost, or if the cable has been switched or disconnected, the initialization procedure must be repeated or else the receiver may not sample the incoming LVDS data correctly.

7.3.10 Input Signal Quality Requirement

The input signal quality must comply to the data sheet requirements (refer to the *Recommended Input Requirements* table for specifications). TI also recommends that no undershoots exceed the specifications listed in the *Absolute Maximum Ratings* table. If the line between the host device and the transmitter is long and acts as a transmission line, then the line should be terminated. If the transmitter is driven from a device with programmable drive strength, TI recommends that the engineer choose a weak setting on the data inputs to prevent transmission line effects. The clock signal is typically set higher to provide a clean edge that is also low jitter.

7.4 Device Functional Modes

See Figure 11 to determine the deskew configuration for the application. For the DS90CR485, only Configuration 4, 5, and 6 are supported.

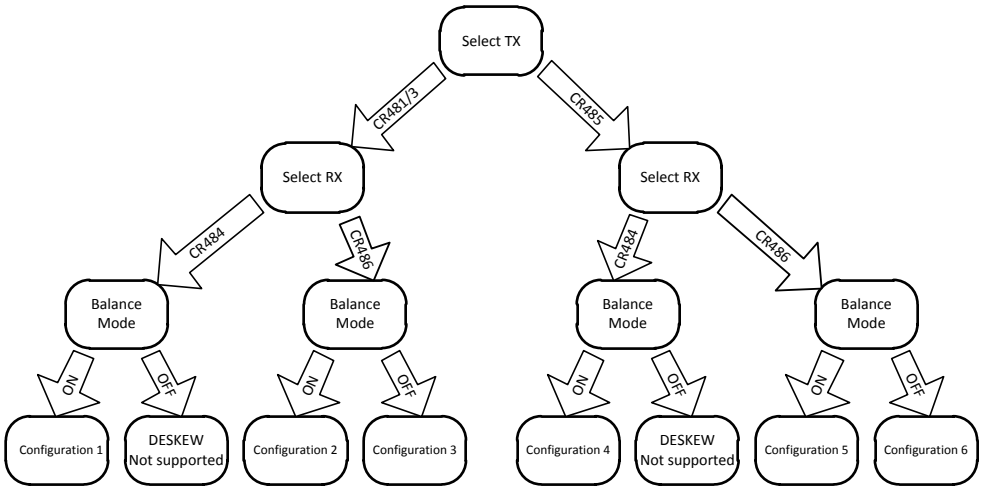


Figure 11. Deskew Configuration Setup Chart

7.4.1 Configuration 4

The DS90CR485 and DS90CR484 with DC Balance ON (BAL = High, 66 MHz to 80 MHz) − The DS_OPT pin at the input of the transmitter DS90CR485 must be applied low for a minimum of four clock cycles for the receiver to complete the deskew operation. The input to the DS_OPT pin can be applied at any time after the PLL has locked to the input clock frequency. In this setup, the "DESKEW" pin on the receiver DS90CR484 must set High.

7.4.2 Configuration 5

The DS90CR485 and DS90CR486 with DC Balance ON (DS90CR486's BAL = High and CON1 = High, 66 MHz to 133 MHz) − The DS_OPT pin at the input of the transmitter DS90CR485 can be set to High OR Low in power up. The period of this input to the DS_OPT pin must be at least 20 ms (TX and RX PLLs lock time) plus 4096 clock cycles for the receiver to complete the deskew operation. The "DESKEW" and CON1 pins on the receiver DS90CR486 must set High.

7.4.3 Configuration 6

The DS90CR485 and DS90CR486 with DC Balance OFF (DS90CR486's BAL = Low, CON1 = High, 66 MHz to 133 MHz) −The input to the DS_OPT pin of the transmitter DS90CR485 in this configuration is completely ignored. To initialize the deskew operation on the receiver DS90CR486, data and clock must be applied to the transmitter when power up. The "DESKEW" and CON1 pins on the receiver DS90CR486 must set High.

Device Functional Modes (continued)

7.4.4 Deskew Not Supported

Deskew function is NOT supported in these configuration setups. The deskew feature is only supported with DC Balance ON (BAL=High) for DS90CR484. Note that the deskew function in the DS90CR486 works in both DC Balance and NON-DC Balance modes.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 How to Configure for Backplane Applications

In a backplane application with a differential line impedance of 100 Ω, the differential line pair-to-pair skew can be controlled through the trace layout. In a backplane application with short PCB distance traces, pre-emphasis from the transmitter is typically not required. The "PRE" pin should be left open (do not tie to ground). A resistor pad provision for a pullup resistor to V_{CC} can be implemented in case pre-emphasis is required to counteract heavy capacitive loading effects.

8.1.2 How to Configure for Cable Interconnect Applications

In applications that require long cable drive capability, the DS90CR485 offers higher bandwidth support and longer cable drive with the use of DC balanced-data transmission and pre-emphasis. Cable drive is enhanced with a user-selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. This requires the use of one pullup resistor to V_{CC} (refer to Table 2 to set the level needed). Optional DC balancing on a cycle-to-cycle basis is also provided to reduce ISI (Inter-Symbol Interference) for long cable applications. With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable.

8.2 Typical Application

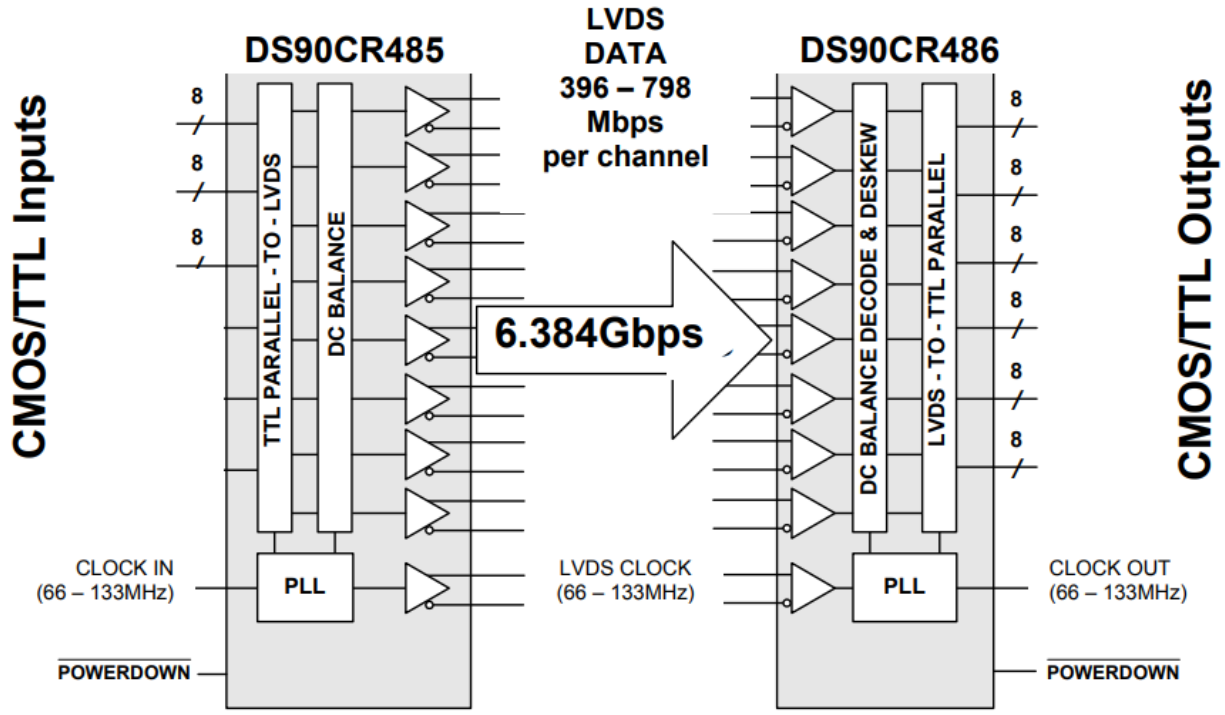


Figure 12. Serializer-Deserializer Application

Typical Application (continued)

8.2.1 Design Requirements

The DS90CR485 is used to convert 24-bit LVCMOS/LVTTL double edge data inputs onto 8 channels of LVDS datastreams.

Table 4. Design Parameters

DESIGN REQUIREMENTS	VALUE
Supply	2.5 V
Receiver	DS90CR486
Input Bit Depth	24

8.2.2 Detailed Design Procedure

8.2.2.1 LVDS Interconnect Guidelines

See *AN-1108 LVDS SerDes Gen I PCB and Interconnect Design-In Guidelines* (SNLA008) and *AN-905 Transmission Line RAPIDESIGNER Operation and Applications* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings (S = space between the pair, 2S = space between the pairs, 3S = space to TTL signal)
- Minimize the number of VIA
- Use differential connectors when operating above 500-Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Minimize skew between pairs
- Terminate as close to the RX inputs as possible

8.2.3 Application Curve

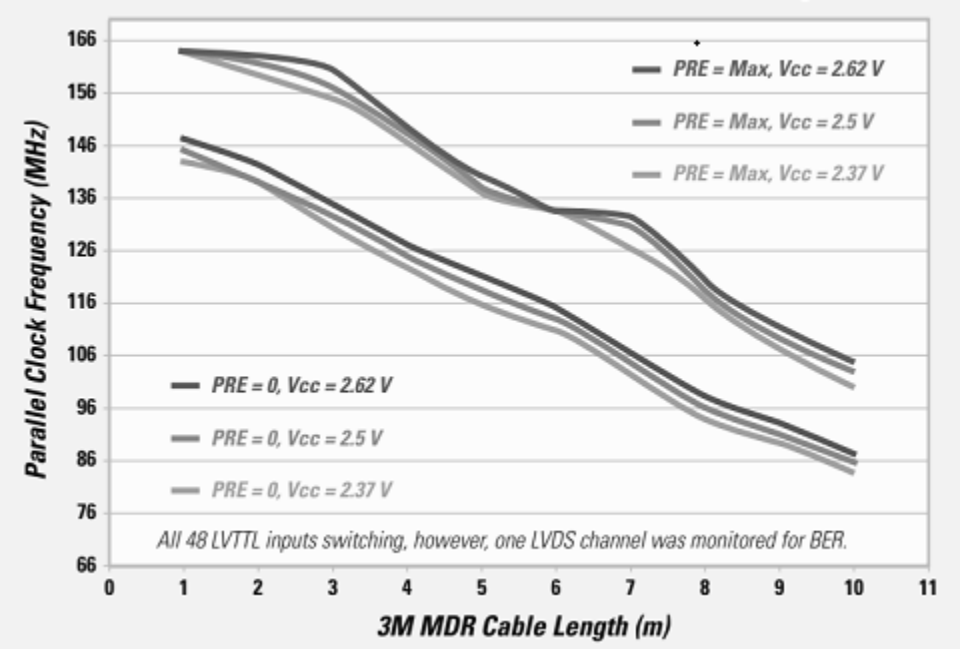


Figure 13. Data Rate vs Cable Length

9 Power Supply Recommendations

9.1 Supply Bypass Recommendations

Bypass capacitors must be used on the power supply pins. Different pins supply different portions of the circuit, therefore capacitors should be nearby all power supply pins, except as noted in the *Pin Functions* table. Use high-frequency ceramic (surface mount recommended) 0.1-μF capacitors close to each supply pin. If space allows, a 0.01-μF capacitor should be used in parallel, with the smallest value closest to the device pin. Additional scattered capacitors over the printed-circuit board will improve decoupling. Multiple (large) vias should be used to connect the decoupling capacitors to the power plane. A 4.7-μF to 10-μF bulk cap is recommended near the PLLVCC and LVDSVCC pins. Connections between the caps and the pin should use wide traces.

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS devices should be designed to provide low-noise power feed to the device. Good layout practice will also separate high-frequency or high-level inputs and outputs to minimize unwanted stray noise pickup, feedback and interference. The engineer can improve power system performance by using thin dielectrics (2 to 4 mils) for power / ground sandwiches. This arrangement provides plane capacitance for the PCB power system with low-inductance parasitics, which can be especially effective at high frequencies, and makes the value and placement of external bypass capacitors less critical. This practice is easier to implement in dense PCBs with many layers and may not be practical in simpler boards. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 uF to 0.1 uF. Tantalum capacitors may be in the 2.2 uF to 10 uF range. Voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

Surface mount capacitors are recommended due to their smaller parasitics. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. TI recommends to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with vias on both ends of the capacitor.

A small body size X7R chip capacitor, such as 0603, is recommended for external bypass. Its small body size reduces the parasitic inductance of the capacitor. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20-30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency. Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Function tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

10.2 Layout Example

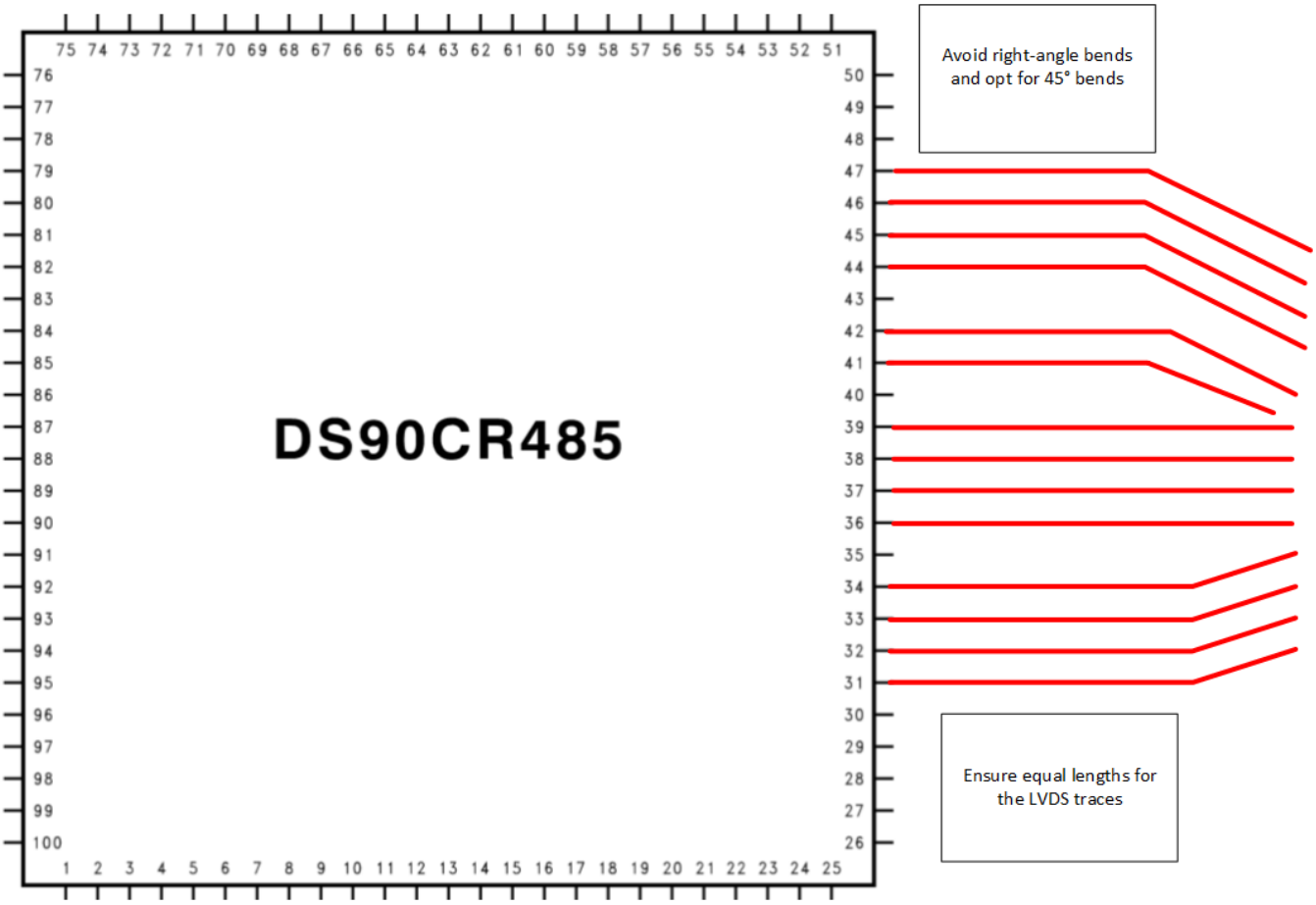


Figure 14. Layout Recommendations

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CR485VS/NOPB	ACTIVE	TQFP	NEZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 70	DS90CR485VS >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

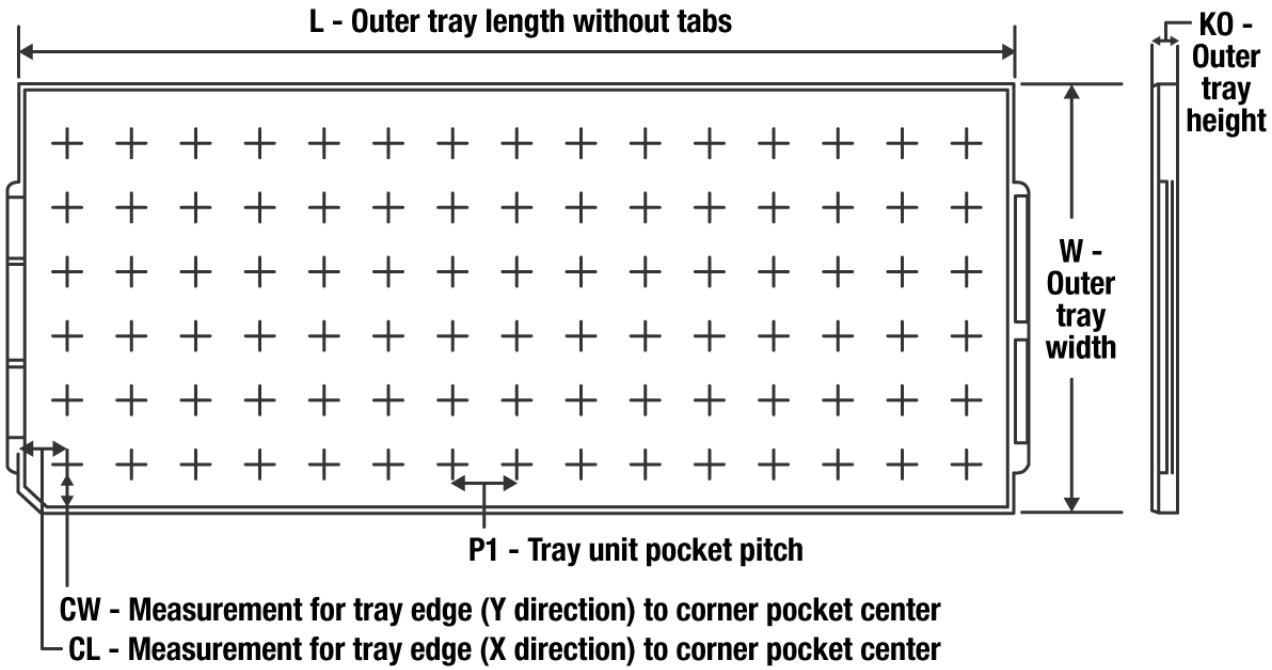
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

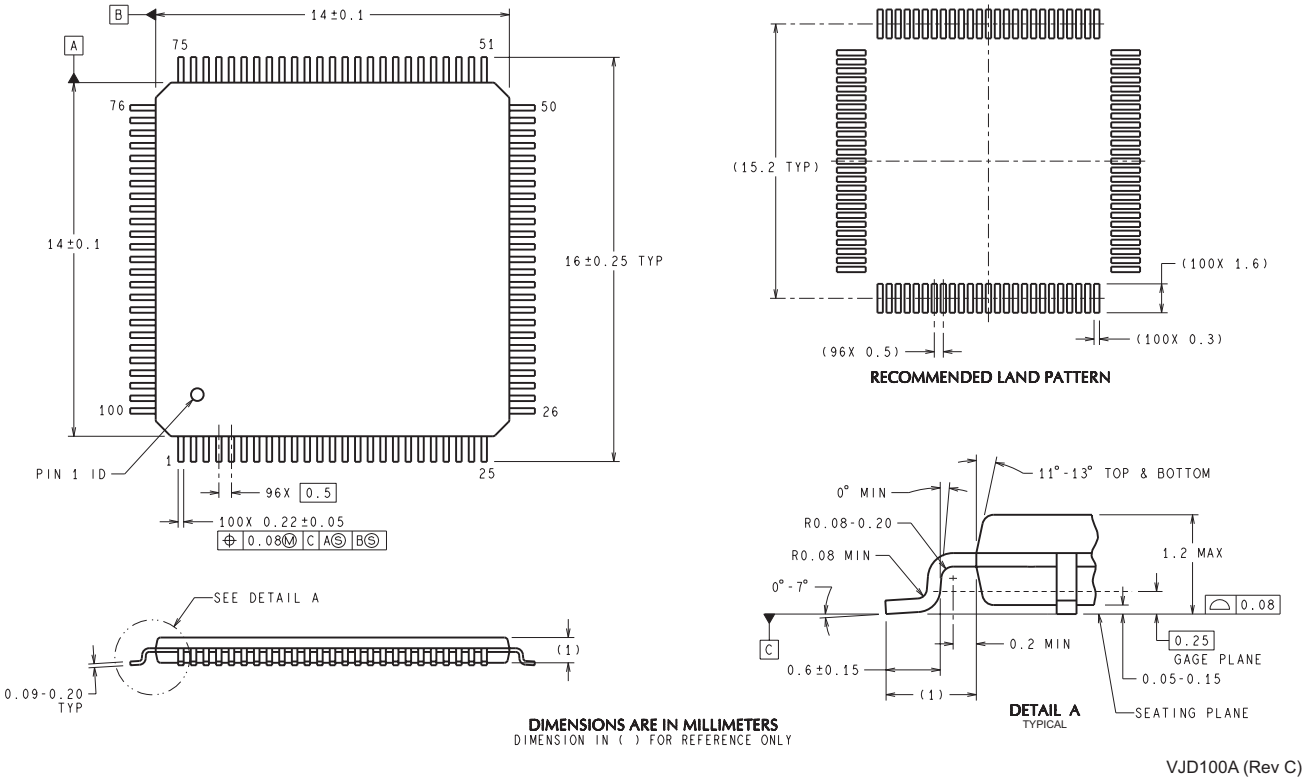


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DS90CR485VS/NOPB	NEZ	TQFP	100	90	6 x 15	150	322.6	135.9	7620	20.3	15.4	15.45

NEZ0100A



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