ESD752 and ESD7x2 采用 SOT-23 和 SOT-323/SC-70 封装且具有 5.7A 8/20µs 浪涌保护的 24V、双通道 ESD 保护二极管

1 特性

- 强大的浪涌保护：
  - IEC 61000-4-5 (8/20µs)：5.7 A
- IEC 61000-4-2 4 级 ESD 保护：
  - ±30kV 或 ±20kV 接触放电
  - ±30kV 或 ±20kV 气隙放电
- 24V 工作电压
- 双向 ESD 保护
- 双通道器件通过单个元件提供全面的 ESD 和浪涌保护
- 低钳位电压可保护下游元件
- I/O 电容 = 3pF 或 1.7pF（典型值）
- SOT-23 (DBZ) 小型、标准、通用封装
- SOT-323/SC-70 (DCK) 超小、标准、节省空间的通用封装
- 引线式封装，用于自动光学检测 (AOI)

2 应用

- USB 电力传输 (USB-PD)：
  - VBUS 保护
  - IO 保护（耐受 VBUS 短路）
- 工业控制网络：
  - 智能配电系统 (SDS)
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 和 EN 50325-4
  - 4/20mA 电路
  - PLC 浪涌保护
  - ADC 浪涌保护

3 说明

ESD752 and ESD7x2 是用于 USB 电力传输 (USB-PD) 和工业接口的双向 ESD 保护二极管。ESD752 and ESD7x2 旨在耗散达到或超出 IEC 61000-4-2 4 级标准所规定最大电平（±30kV 或 ±20kV 接触和 ±30kV 或 ±20kV 气隙）的接触式 ESD。低动态电阻和低钳位电压确保针对瞬态事件提供系统级保护。这种保护至关重要，因为工业系统对鲁棒性和可靠性的要求很高。

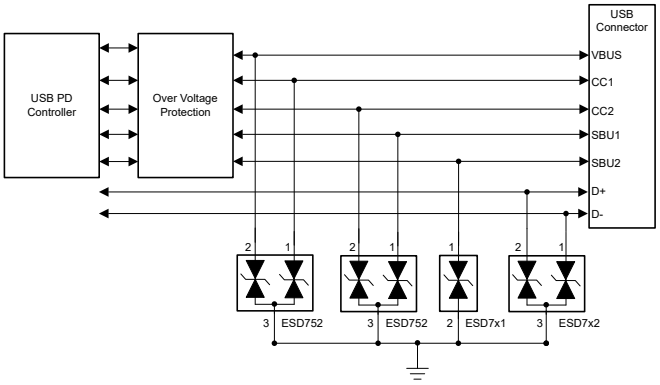
这些器件具有每通道低 IO 电容和提供两条 IO 线路的引脚排列，可防止因静电放电 (ESD) 和其他瞬变造成损坏。ESD752 的 I_{PP} = 5.7A（8/20µs 浪涌波形）能力使其适用于保护 USB VBUS 和工业 I/O 线路免受瞬态浪涌事件的影响。此外，ESD752 和 ESD7x2 的 3pF 或 1.7pF 线路电容适用于保护 USB 电力传输的低速信号和工业应用的 IO 信号。

ESD752 and ESD7x2 采用两种引线式封装，可轻松实现直通式布线。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
ESD752	DCK（SOT-323/SC-70，3）	2.00mm × 1.25mm
	DBZ（SOT-23，3）	2.92mm × 1.30mm
ESD7x2	DBZ（SOT-23，3）	2.92mm × 1.30mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



USB 电力传输典型应用

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (May 2022) to Revision A (August 2022)	Page
• 将数据表的状态从*预告信息*更改为*量产数据*	1

5 Pin Configuration and Functions

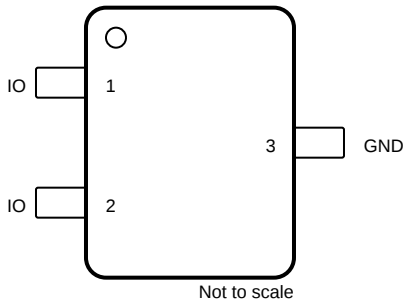


图 5-1. DCK and DBZ Package, 3-Pin SOT-323 / SC-70 and SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	—	Connect to ground.

(1) I/O = Input or Output,

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		DEVICE	MIN	MAX	UNIT
Peak pulse	IEC 61000-4-5 Power (t_p – 8/20 µs) at 25°C	ESD752		210	W
	IEC 61000-4-5 current (t_p – 8/20 µs) at 25°C	ESD752		5.7	A
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	°C
T_{stg}	Storage temperature		-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings—JEDEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	± 2500	V
		Charged device model (CDM), per JEDEC specification JS-002	± 1000	

6.3 ESD Ratings—IEC Specification

PARAMETER		TEST CONDITION	DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD752	±30000	V
		IEC 61000-4-2 Air Discharge, all pins		±30000	

6.4 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	−24		24	V
T_A	Operating free-air temperature	−55		150	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD752		ESD7x2	UNIT
		DBZ (SOT-23)	DCK (SOT-323 / SC-70)	DBZ (SOT-23)	
		3 PINS	3PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	291.5	283.0	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	147.1	164.1	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	131.1	105.1	TBD	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.0	67.1	TBD	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	130.2	104.4	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage		ESD752	– 24		24	V
V_{BRF}	Forward breakdown voltage(2)	I_{IO} = 10 mA, IO to GND	ESD752	25.5		35.5	V
V_{BRR}	Reverse breakdown voltage(2)	I_{IO} = – 10 mA, IO to GND	ESD752	– 35.5		– 25.5	V
V_{CLAMP}	Clamping voltage(4)	I_{PP} = 5.7 A, t_p = 8/20 µs, IO to GND	ESD752		37		V
	Clamping voltage(5)	I_{PP} = 16 A, TLP, IO to GND or GND to IO			35		
V_{Hold}	Holding voltage after snapback(3)	TLP	ESD752		30		V
I_{LEAK}	Leakage current	V_{IO} = ±24 V, IO to GND	ESD752	-50	5	50	nA
R_{DYN}	Dynamic resistance(5)	IO to GND	ESD752		0.35		Ω
		GND to IO			0.35		
C_L	Line capacitance(6)	V_{IO} = 0 V, f = 1 MHz, V_{pp} = 30 mV	ESD752		3	5	pF

(1) Measurements made on both IO channels.
(2) V_{BRF} and V_{BRR} are defined as the voltage when ± 10 mA is applied in the positive or negative direction respectively, before the device latches into the snapback state.
(3) V_{HOLD} is defined as the lowest voltage on the TLP plot once the trigger threshold is reached and the device snapbacks and begins clamping the voltage.
(4) Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
(5) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.
(6) Measured from IO to GND on both channels.

6.7 Typical Characteristics

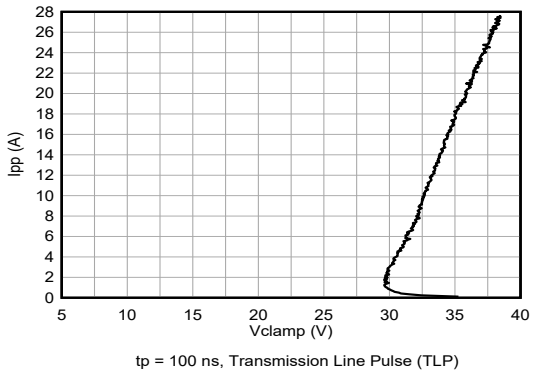


图 6-1. Positive TLP Curve

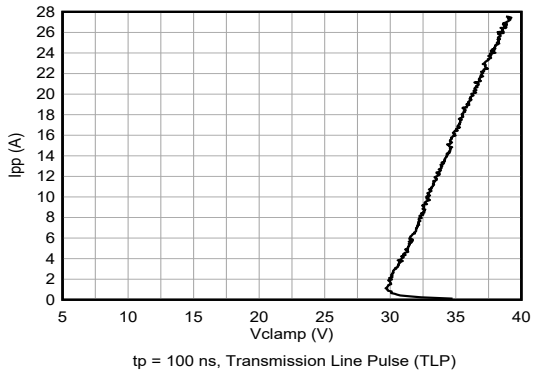


图 6-2. Negative TLP Curve

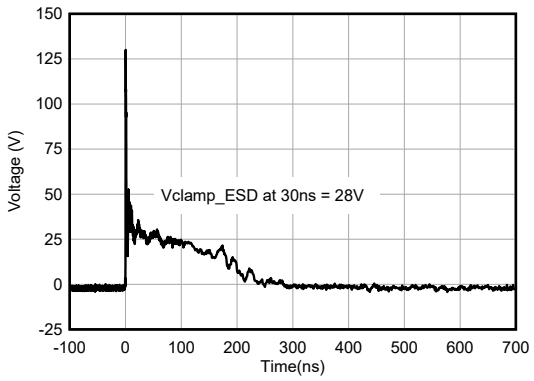


图 6-3. +8-kV Clamped IEC Waveform

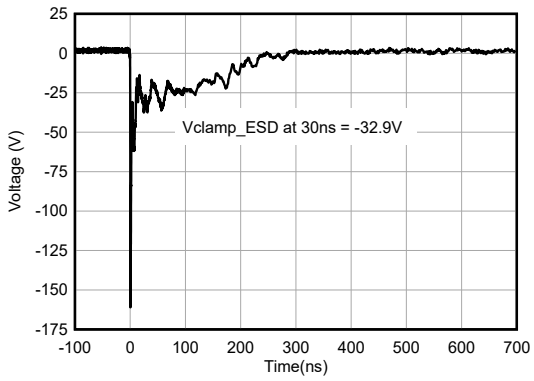


图 6-4. −8-kV Clamped IEC Waveform

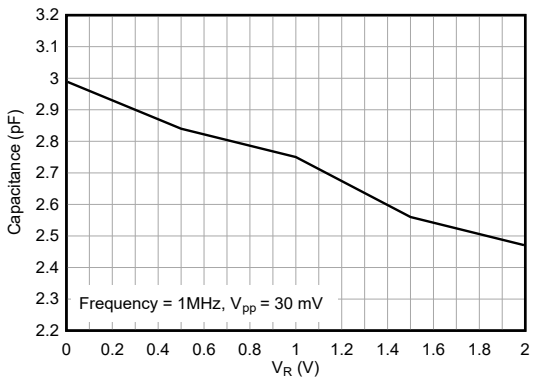


图 6-5. Capacitance vs. Bias Voltage

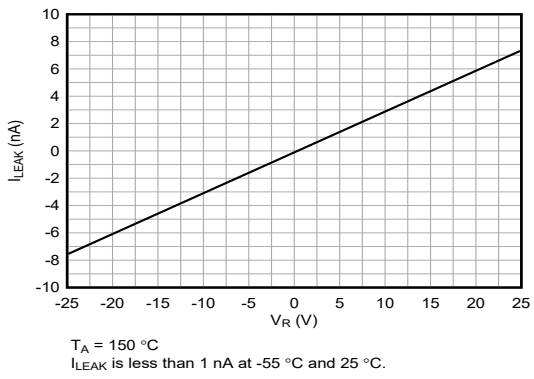


图 6-6. Leakage Current vs. Bias Voltage Across Temperature

6.7 Typical Characteristics (continued)

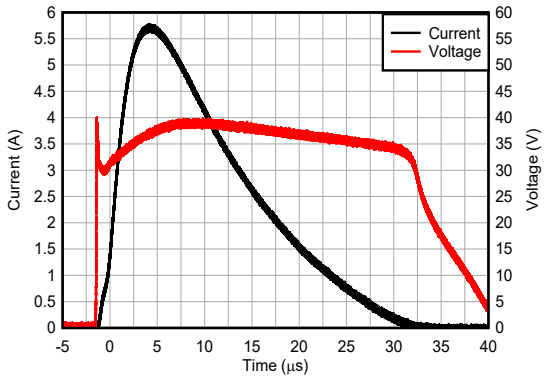


图 6-7. 8/20 µs Surge Response at 5.7 A

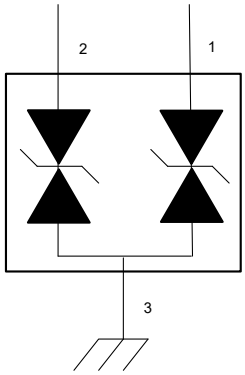
7 Detailed Description

7.1 Overview

The ESD752 and ESD7x2 are dual-channel ESD TVS diodes in SOT-23 and SOT-323 (SC-70) leaded packages which are convenient for automatic optical inspection. This product offers IEC 61000-4-2 ±30-kV or ±20-kV air-gap, ±30-kV or ±20-kV contact ESD protection respectively, and has a clamp circuit with a back-to-back TVS diode for bidirectional signal support.

A typical application of this product is the ESD protection for USB-PD slower speed signals (CC1, CC2, SBU1, SBU2, D+, and D-). The I_{PP} = 5.7 A (8/20 µs surge waveform) capability of the ESD752 makes it suitable for protecting VBUS. The ESD752 device is also a good fit for protecting industrial IOs requiring 5.7 A or less of surge current protection. The 3 pF or 1.7 pF line capacitance of these ESD protection diodes are suitable for USB-PD slower speed signals and industrial IO applications.

7.2 Functional Block Diagram



7.3 Feature Description

The ESD752 and ESD7x2 are bidirectional TVS diodes with a high ESD protection level. This device protects the circuit from ESD strikes up to ±30-kV or ±20-kV contact and ±30-kV or ±20-kV air-gap respectively as specified in the IEC 61000-4-2 standard. The ESD752 and ESD7x2 can also handle up to 5.7 A or 1.5 A of surge current (IEC 61000-4-5 8/20 µs) respectively. The I/O capacitance of 3 pF or 1.7 pF are suitable for USB power delivery slower speed signals and industrial applications. These clamping devices have a small dynamic resistance, which makes the clamping voltage low when the device is actively protecting other circuits. For example, the ESD752 clamping voltage is only 37 V when the device is taking 5.7 A transient current. The breakdown is bidirectional so these protection devices are a good fit for applications requiring postive and negative polarity protection. Low leakage allows these diodes to conserve power when working below the V_{RWM}. The temperature range of −55°C to +150°C makes this ESD device work at extensive temperatures in most environments. The leaded SOT-23 and SOT-323 (SC-70) packages are good for applications requiring automatic optical inspection (AOI).

7.3.1 Temperature Range

These devices are qualified to operate from –55°C to +150°C.

7.3.2 IEC 61000-4-5 Surge Protection

The IO pins can withstand surge events up to 5.7 A and 1.5 A (8/20 µs waveform) for the ESD752 and ESD7x2 respectively. An ESD-surge clamp diverts this current to ground.

7.3.3 IO Capacitance

The capacitance between the I/O pins is 3 pF and 1.7 pF for the ESD752 and ESD7x2 respectively. These capacitances are suitable for USB power delivery slower speed signals and industrial applications.

7.3.4 Dynamic Resistance

The IO pins feature an ESD clamp that has a low R_{DYN} of 0.35 Ω for the ESD752 device, and 0.57 Ω for the ESD7x2 device, which prevents system damage during ESD events.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage between the IO pins is a minimum of ± 25.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ± 24 V.

7.3.6 Ultra Low Leakage Current

The IO pins feature an ultra-low leakage current of 50 nA (maximum) with a bias of ± 24 V.

7.3.7 Clamping Voltage

The IO pins feature an ESD clamp that is capable of clamping the voltage to 37 V (I_{PP} = 5.7 A for 8/20 µs surge waveform), 35 V (I_{PP} = 16 A for TLP), 36 V (I_{PP} = 1.5 A for 8/20 µs surge waveform), and 38 V (I_{PP} = 16 A for TLP) for the ESD752 and ESD7x2, respectively.

7.3.8 Industry Standard Leaded Packages

These devices feature industry standard SOT-23 (DBZ) and SC-70 (DCK) leaded packages for automatic optical inspection (AOI).

7.4 Device Functional Modes

The ESD752 and ESD7x2 are dual channel passive clamp devices that have low leakage during normal operation when the voltage between IO and GND is below V_{RWM}, and activate when the voltage between IO and GND goes above V_{BR}. During IEC 61000-4-2 ESD events, transient voltages as high as ±30 kV can be clamped on either channel. When the voltages on the protected lines fall below the V_{HOLD}, the device reverts back to the low leakage passive state.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD752 and ESD7x2 are dual channel TVS diodes which are used to provide a path to ground for dissipating ESD events on USB-PD or industrial IO signal lines. As the current from the ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC.

8.2 Typical Application

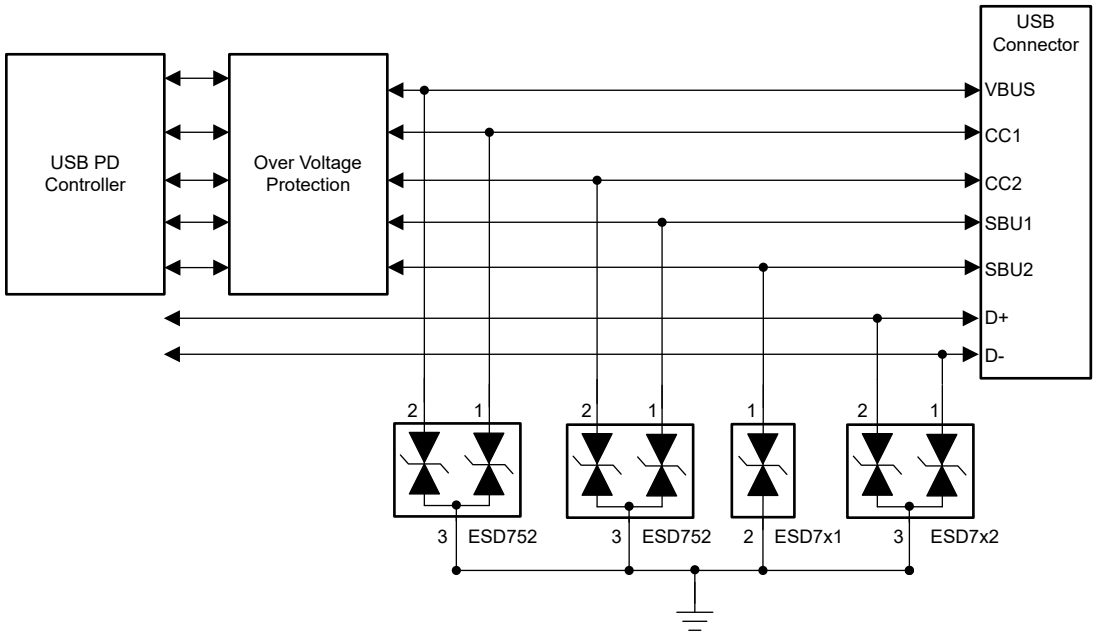


图 8-1. USB Power Delivery Typical Application

8.2.1 Application

8.2.2 Design Requirements

For this design example, the ESD752 and ESD7x2 are used to provide ESD protection on a USB-PD connector. 表 8-1 lists the known design parameters for this application.

表 8-1. Design Parameters for the USB Power Delivery Typical Application

Design Parameter	Value
Diode configuration	Bidirectional
VBUS Voltage	+ 20 V
V_{IO} signal range	+ 3.3 V
V_{RWM}	± 24 V
Short to VBUS event on V_{IO}	± 20 V
Data rate	Up to 480 Mbps

8.2.3 Detailed Design Procedure

The ESD752 and ESD7x2 has a V_{RWM} of ± 24 V to prevent the diode from being damaged during a short event that can occur when one of the USB-PD slower speed lines (CC1, CC2, SBU1, SBU2, D+, and D-) is shorted to VBUS. The bidirectional characteristic ensures both positive and negative polarity are protected. The low 1.7 pF capacitance of the ESD7x2 device ensures data rates up to 480 Mbps, which allows the designer to meet the requirements for the D+ and D- signals. The ESD752 has an I_{PP} = 5.7 A (8/20 µs) surge current capability making it suitable for protecting the VBUS power rail.

8.2.4 Application Curves

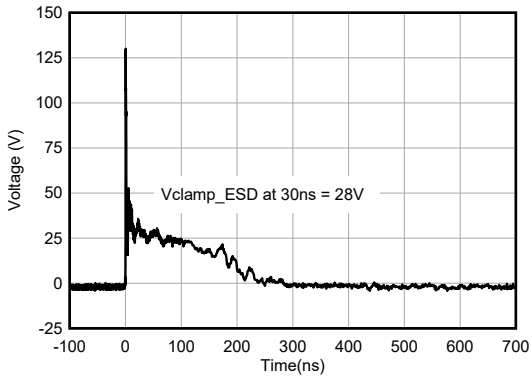


图 8-2. +8-kV Clamped IEC Waveform

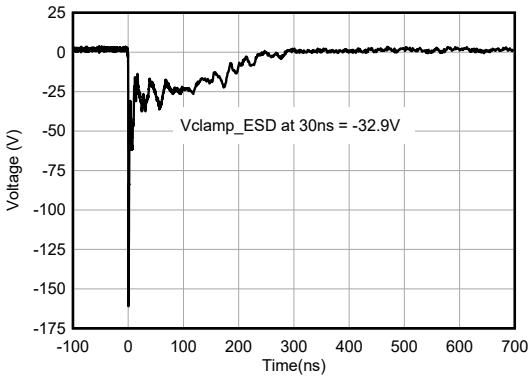


图 8-3. −8-kV Clamped IEC Waveform

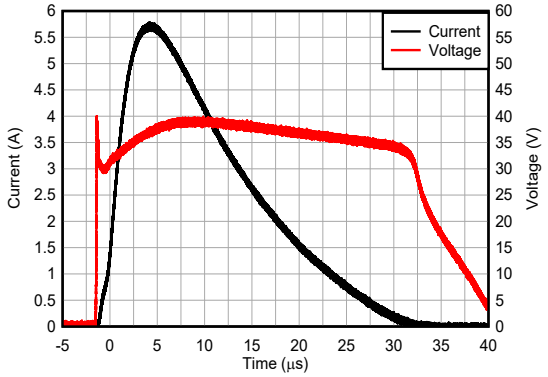


图 8-4. 8/20 µs Surge Response at 5.7 A

9 Power Supply Recommendations

These are passive TVS diode-based ESD protection devices; therefore, there is no requirement to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

- If pin 3 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

This is a typical example of a dual channel IO routing.

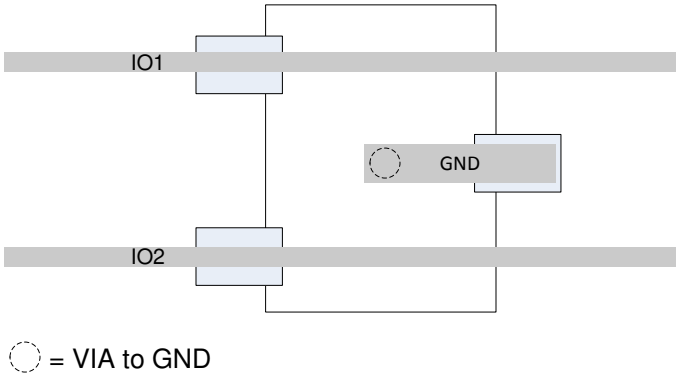


图 10-1. Routing with DBZ and DCK Package

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD and Surge Protection for USB Interfaces* application note
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD752DBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2RP8	Samples
ESD752DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 150	1MP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

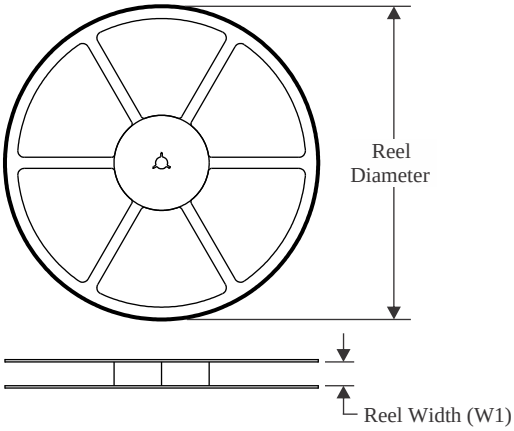
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

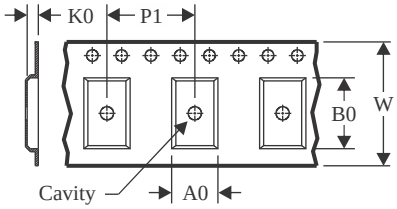
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

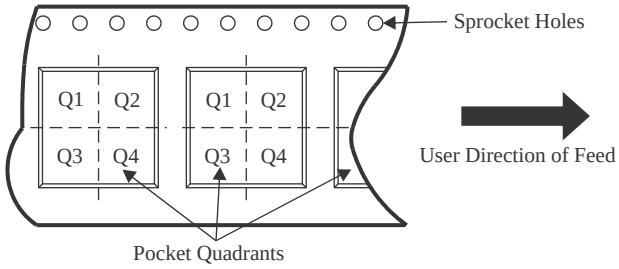


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

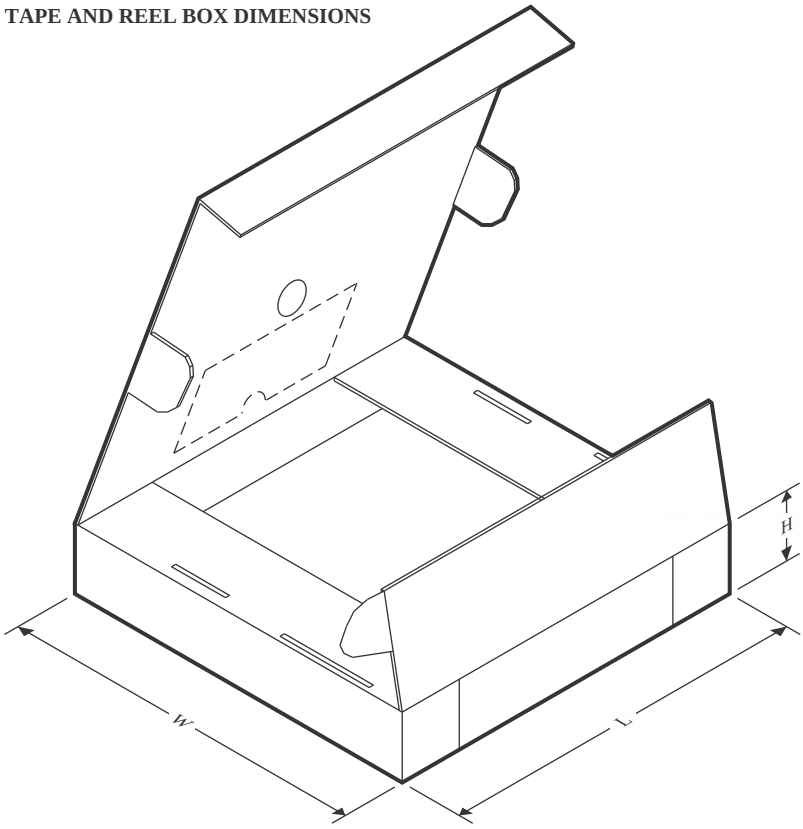
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD752DBZR	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD752DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



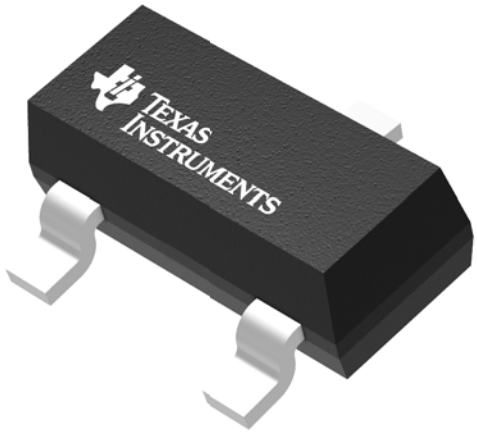
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD752DBZR	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD752DCKR	SC70	DCK	3	3000	180.0	180.0	18.0

GENERIC PACKAGE VIEW

DBZ 3 SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



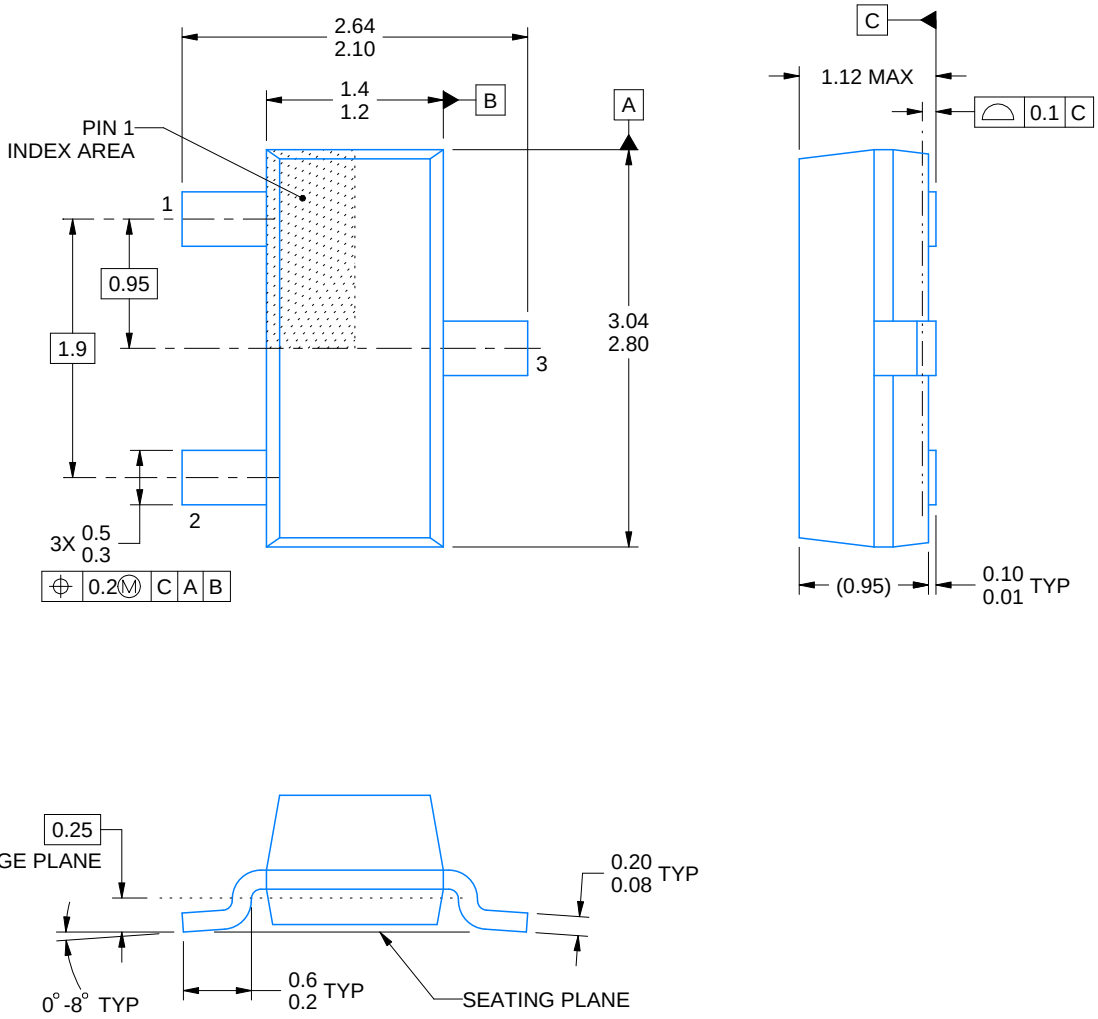
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

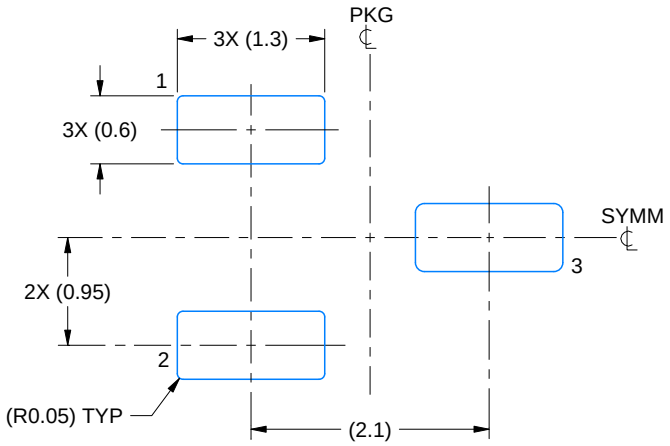
SMALL OUTLINE TRANSISTOR



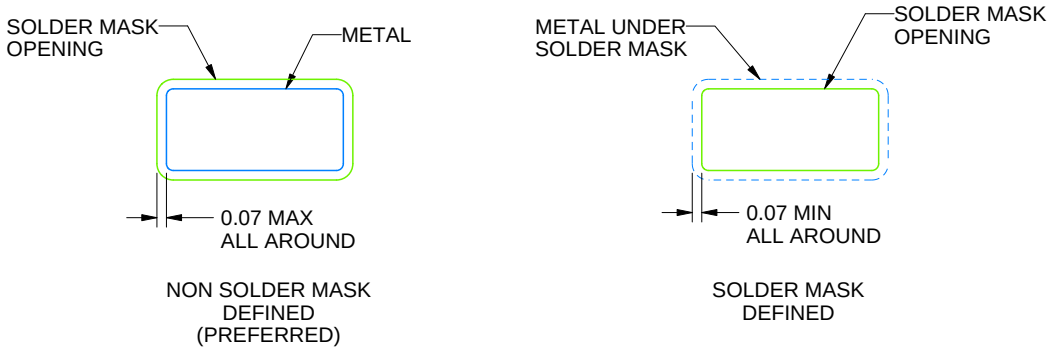
4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.



LAND PATTERN EXAMPLE
SCALE:15X

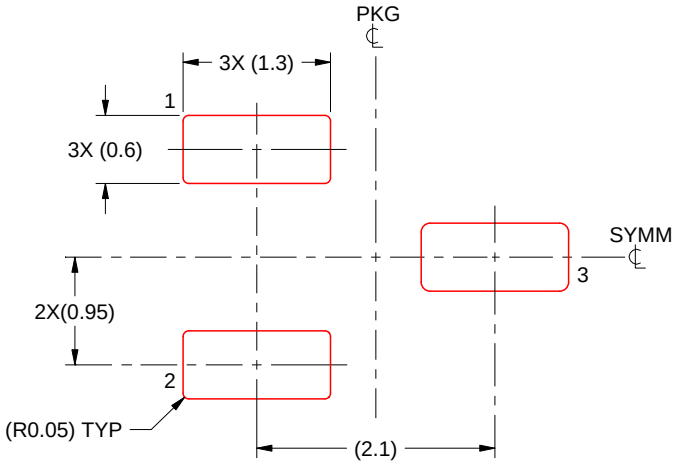


SOLDER MASK DETAILS

4214838/C 04/2017

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

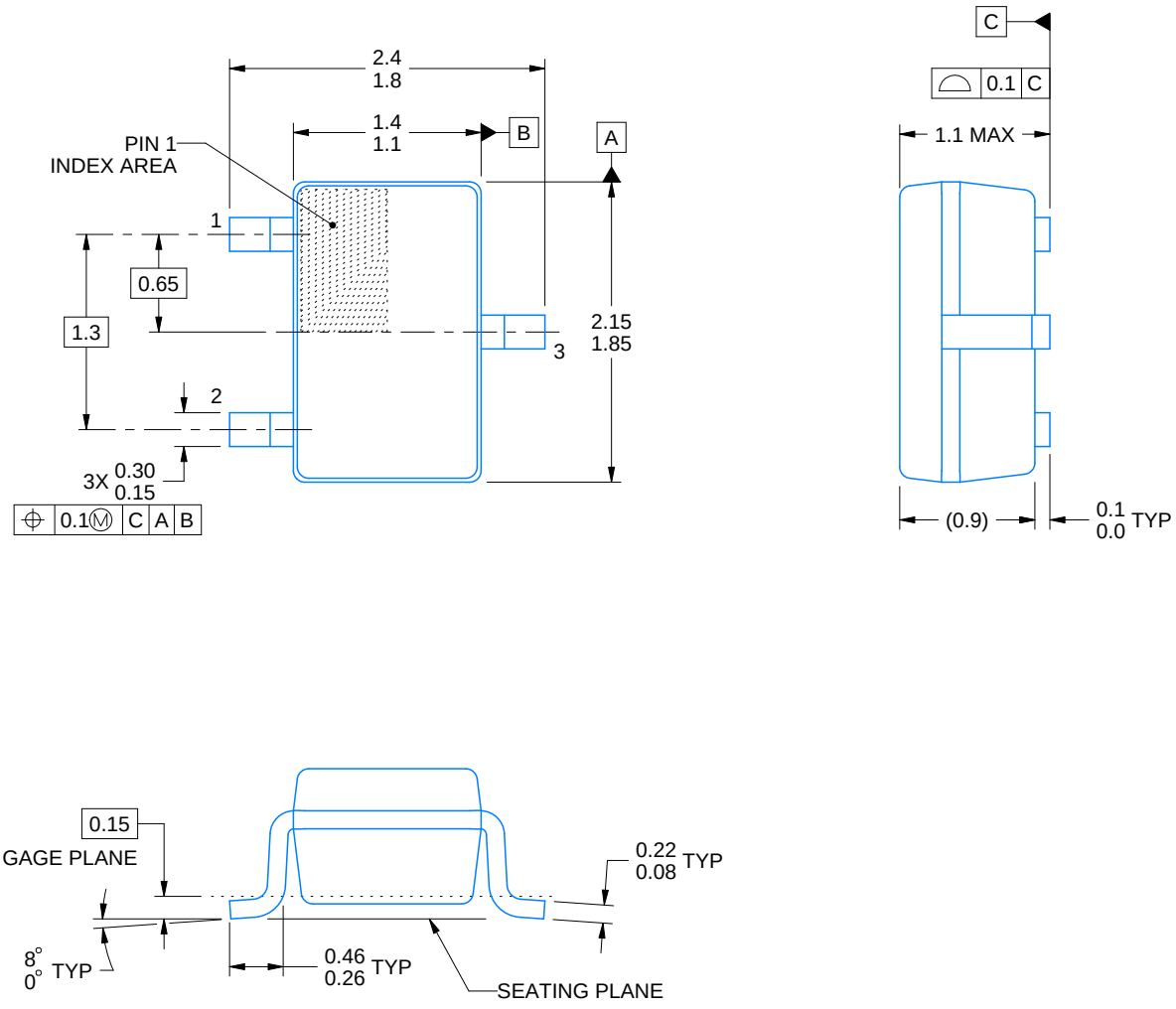
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DCK0003A

PACKAGE OUTLINE

SOT-SC70 - 1.1 max height

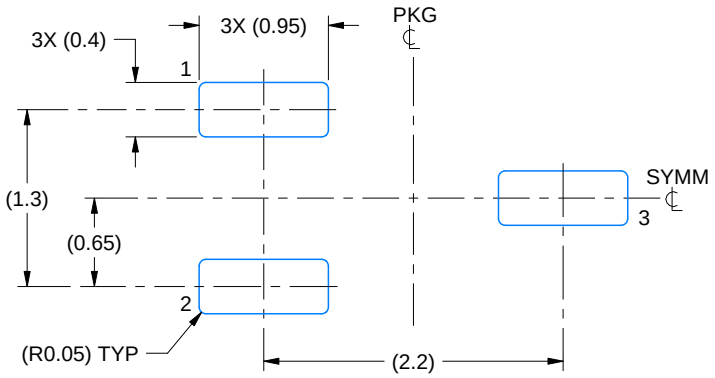
SMALL OUTLINE TRANSISTOR SC70



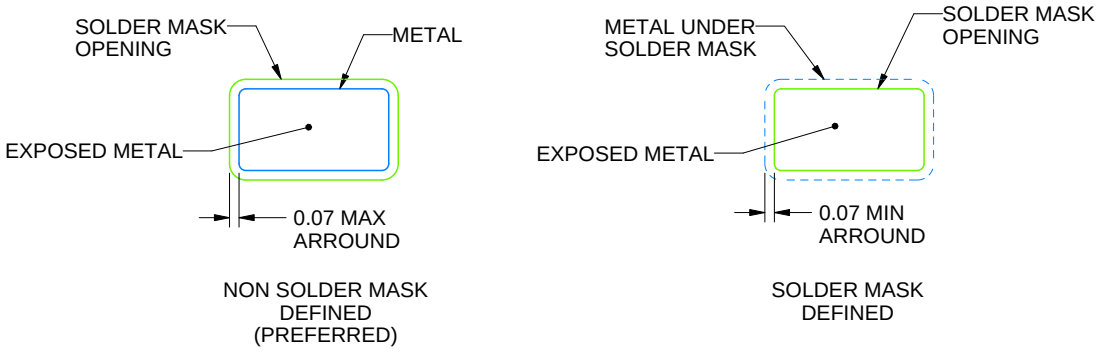
4220745/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

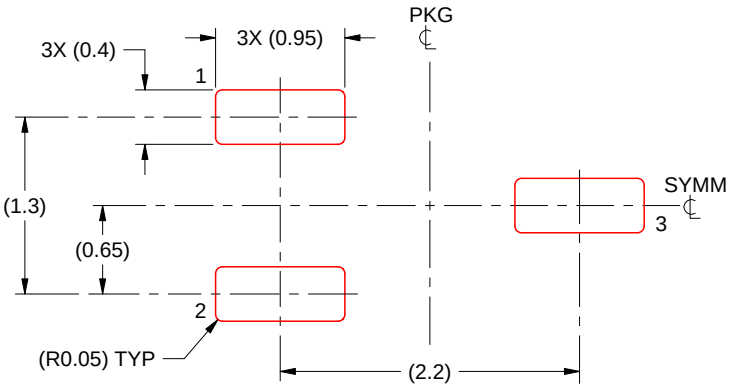


SOLDER MASK DETAILS

4220745/C 06/2021

NOTES: (continued)

3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4220745/C 06/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
6. Board assembly site may have different recommendations for stencil design.

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