

MSP430F673xA、MSP430F672xA 混合信号微控制器

1 器件概述

1.1 特性

- 低电源电压范围：
3.6V 到低至 1.8V
- 超低功耗
 - 激活模式 (AM):
所有系统时钟激活
在 8MHz、3.0V 且闪存程序执行时为
265 μ A/MHz (典型值)
在 8MHz、3.0V 且 RAM 程序执行时为
140 μ A/MHz (典型值)
 - 待机模式 (LPM3):
含晶体的实时时钟 (RTC)、看门狗、电源监视器
可用、完全 RAM 保持、快速唤醒：
2.2V 时为 1.7 μ A，3.0V 时为 2.5 μ A (典型值)
 - 关闭模式 (LPM4):
完全 RAM 保持、电源监视器可用、快速唤醒：
3.0V 时为 1.6 μ A (典型值)
 - 关断 RTC 模式 (LPM3.5):
关断模式，RTC (采用晶振) 工作：
3.0V 时为 1.24 μ A (典型值)
 - 关断模式 (LPM4.5):
3.0V 时为 0.78 μ A (典型值)
- 在 3 μ s (典型值) 内从待机模式唤醒
- 16 位精简指令集计算机 (RISC) 架构，扩展内存，
高达 25MHz 的系统时钟
- 灵活的电源管理系统
 - 内置可编程的低压降稳压器 (LDO)
 - 电源电压监视、监控、和临时限电
 - 由多达 2 个辅助电源供电的系统运行
- 单一时钟系统
 - 针对频率稳定的锁相环 (FLL) 控制环路
 - 低功耗低频内部时钟源 (VLO)
 - 低频修整内部基准源 (REFO)
 - 32kHz 晶体 (XT1)
- 一个具有 3 个捕捉/比较寄存器的 16 位定时器
- 3 个 16 位定时器，每个定时器具有 2 个捕捉/比较
寄存器
- 增强型通用串行通信接口 (eUSCI)
 - eUSCI_A0、eUSCI_A1 和 eUSCI_A2
 - 增强型通用异步收发器 (UART) 支持自动波特
率检测
 - IrDA 编码和解码
 - 同步串行外设接口 (SPI)
 - eUSCI_B0
 - 支持多个从器件寻址的 I²C
 - 同步串行外设接口 (SPI)
- 具有晶振偏移校准和温度补偿功能的受密码保护的
RTC
- 用于备用子系统的独立电压电源
 - 32kHz 低频振荡器 (XT1)
 - 实时时钟
 - 备用存储器 (4 \times 16 位)
- 三个具有差分可编程增益放大器 (PGA) 输入的 24
位 Σ - Δ 模数转换器 (ADC)
- 具有 8 路复用模式下高达 320 段对比度控制 的集成
LCD 驱动器
- 硬件乘法器支持 32 位运算
- 10 位 200ksps ADC
 - 内部基准
 - 采样和保持、自动扫描特性
 - 多达 6 个外部通道和 2 个内部通道，包括温度传
感器
- 3 通道内部直接内存访问 (DMA)
- 串行板上编程，无需外部编程电压
- [器件比较](#) 汇总了可用的产品系列成员
- 采用 100 引脚和 80 引脚 LQFP 封装
- 单相电子电表开发工具 (另请参阅 [工具与软件](#))
 - [EVM430-F6736 - 用于计量的 MSP430F6736
EVM](#)
 - [适用于 MSP430™ MCU 的能量测量设计中心](#)

1.2 应用

- 单相电子式电度表
- 公用事业仪表计量
- 能量监控

1.3 说明

TI MSP 系列超低功耗微控制器种类繁多，各成员器件配备不同的外设集以满足各类应用的需求。此架构与多种低功耗模式配合使用，是延长便携式测量应用电池寿命的最优选择。该器件具有一个强大的 16 位精简指令集 (RISC) CPU，使用 16 位寄存器以及常数发生器，以便获得最高编码效率。DCO 可使器件在不到 3 μ s（典型值）的时间内从低功耗模式唤醒至激活模式。

MSP430F673xA 和 MSP430F672xA 微控制器具有高性能 24 位 Σ - Δ ADC（MSP430F673xA 中有 3 个 ADC，MSP430F672xA 中有 2 个 ADC）、1 个 10 位 ADC、4 个 eUSCI（3 个 eUSCI_A 模块和 1 个 eUSCI_B 模块）、4 个 16 位计时器、1 个硬件乘法器、1 个 DMA 模块、1 个具有报警功能的 RTC 模块、1 个具有集成对比度控制功能的 LCD 驱动器以及 1 个辅助电源系统；100 引脚器件的 I/O 引脚多达 72 个，而 80 引脚器件的 I/O 引脚多达 52 个。

要获得完整的模块说明，请参阅《MSP430F5xx 和 MSP430F6xx 系列用户指南》

器件信息⁽¹⁾

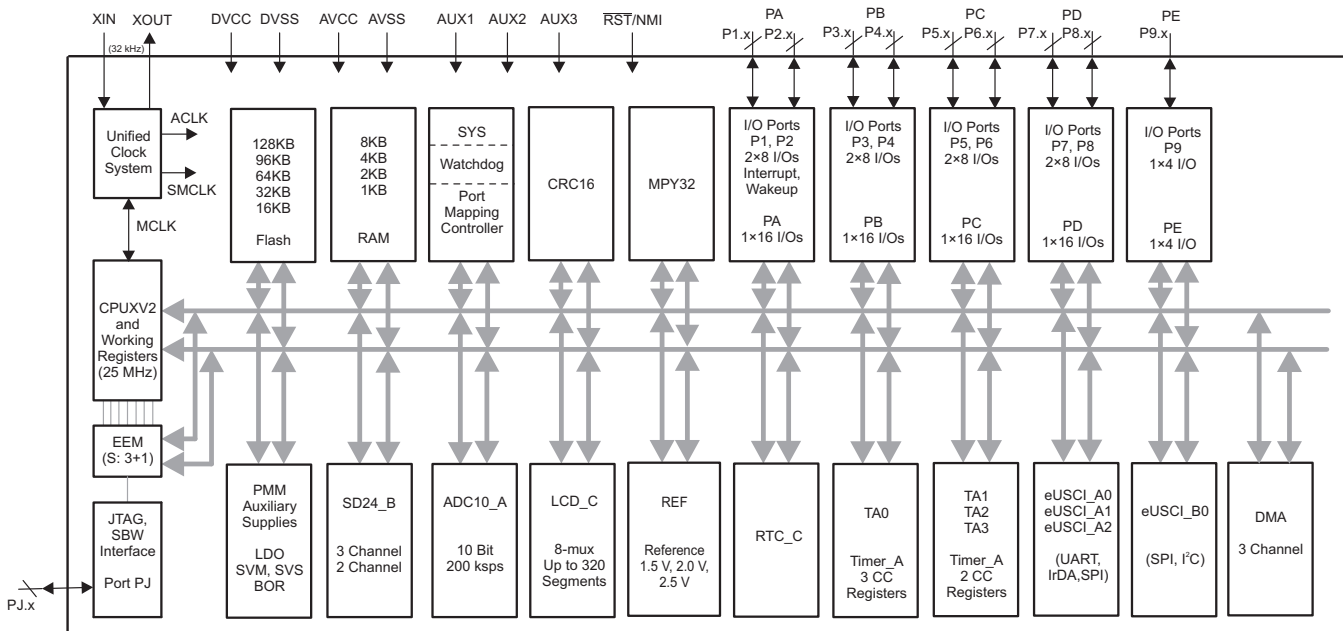
| 器件型号 | 封装 | 封装尺寸 ⁽²⁾ |
|-----------------|------------|---------------------|
| MSP430F6736AIPZ | LQFP (100) | 14mm x 14mm |
| MSP430F6736AIPN | LQFP (80) | 12mm x 12mm |

(1) 要获得最新的产品、封装和订购信息，请参见封装选项附录（节 9），或者访问德州仪器 (TI) 网站 www.ti.com.cn。

(2) 这里显示的尺寸为近似值。要获得包含误差值的封装尺寸，请参见机械数据（节 9）。

1.4 功能框图

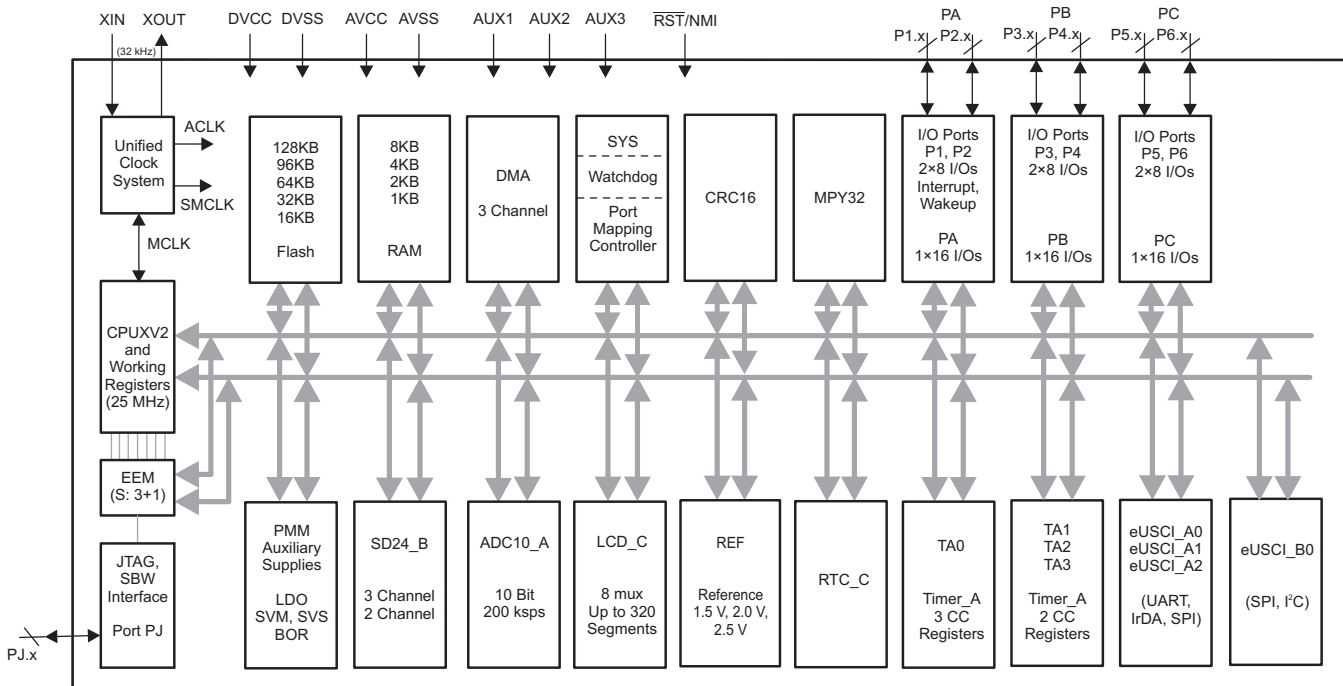
图 1-1 给出了所有采用 PZ 封装的器件型号的功能框图。



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图 1-1. 功能框图 - MSP430F673xAIPZ 和 MSP430F672xAIPZ

图 1-2 给出了所有采用 PN 封装的器件型号的功能框图。



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图 1-2. 功能框图 - MSP430F673xAIPN 和 MSP430F672xAIPN

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2 修订历史记录

| Changes from February 25, 2015 to October 3, 2018 | Page |
|--|---------------------|
| • 在以下位置添加了指向开发工具和设计中心的链接: 特性 | 1 |
| • Added Section 3.1, Related Products | 7 |
| • Added Section 4.5, Buffer Type | 33 |
| • Added typical conditions statements at the beginning of Section 5, Specifications | 34 |
| • Added SD24_B input pins and AUXVCCx pins to exception list on "Voltage applied to pins" parameter, and added SD24_B input pin limits in "Diode current at pins" parameter in Section 5.1, Absolute Maximum Ratings | 34 |
| • Added Section 5.7, Thermal Resistance Characteristics | 39 |
| • Corrected nonvolatile memory type (changed "FRAM" to "flash") in 节 5.8.1, Power Supply Sequencing | 40 |
| • Updated notes (1) and (2) and added note (3) in Table 5-1, Wake-up Times From Low-Power Modes and Reset .. | 40 |
| • Changed the MIN value of the $V_{(DVCC_BOR_hys)}$ parameter from 60 mV to 50 mV in Table 5-12, PMM, Brownout Reset (BOR) | 50 |
| • Replaced f_{Frame} parameter with f_{LCD} , $f_{FRAME,4mux}$, and $f_{FRAME,8mux}$ parameters in Table 5-33, LCD_C Operating Conditions | 62 |
| • Removed ADC10DIV from the formula for the TYP value in the second row for $t_{CONVERT}$ in Table 5-44, 10-Bit ADC, Timing Parameters , because $f_{ADC10CLK}$ is after division | 71 |
| • Updated Test Conditions for all parameters in Table 5-45, 10-Bit ADC, Linearity Parameters : changed from " $(V_{eREF+} - V_{eREF-})_{min} \leq (V_{eREF+} - V_{eREF-})$ " to " $1.4 V \leq (V_{eREF+} - V_{eREF-})$ " in all cases..... | 72 |
| • Added " $C_{VeREF+} = 20 pF$ " to E _I Test Conditions..... | 72 |
| • Changed all instances of "bootloader" to "bootloader" | 79 |
| • Corrected spelling of NMIFG in 表 6-9, System Module Interrupt Vector Registers | 85 |
| • Corrected port number in title of 表 6-21, Port P2 (P2.0 and P2.1) Pin Functions (MSP430F67xxAIPZ Only) | 96 |
| • 将先前的开发工具支持部分替换为 节 8.3 工具与软件 | 144 |
| • 更改了格式并在 节 8.4 文档支持 中添加了内容 | 146 |

3 Device Comparison

Table 3-1 summarizes the available family members.

Table 3-1. Device Comparison⁽¹⁾ ⁽²⁾

| DEVICE | FLASH (KB) | SRAM (KB) | SD24_B CONVERTERS | ADC10_A CHANNELS | Timer_A ⁽³⁾ | eUSCI_A: UART, IrDA, SPI | eUSCI_B: SPI, I ² C | I/Os | PACKAGE |
|-----------------|------------|-----------|-------------------|------------------|------------------------|--------------------------|--------------------------------|------|---------|
| MSP430F6736AIPZ | 128 | 8 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6735AIPZ | 128 | 4 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6734AIPZ | 96 | 4 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6733AIPZ | 64 | 4 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6731AIPZ | 32 | 2 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6730AIPZ | 16 | 1 | 3 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6726AIPZ | 128 | 8 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6725AIPZ | 128 | 4 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6724AIPZ | 96 | 4 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6723AIPZ | 64 | 4 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6721AIPZ | 32 | 2 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6720AIPZ | 16 | 1 | 2 | 6 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 72 | 100 PZ |
| MSP430F6736AIPN | 128 | 8 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6735AIPN | 128 | 4 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6734AIPN | 96 | 4 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6733AIPN | 64 | 4 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6731AIPN | 32 | 2 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6730AIPN | 16 | 1 | 3 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6726AIPN | 128 | 8 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6725AIPN | 128 | 4 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6724AIPN | 96 | 4 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6723AIPN | 64 | 4 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6721AIPN | 32 | 2 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |
| MSP430F6720AIPN | 16 | 1 | 2 | 3 ext, 2 int | 3, 2, 2, 2 | 3 | 1 | 52 | 80 PN |

- (1) For the most current package and ordering information, see the *Package Option Addendum* in [§ 9](#), or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Microcontrollers TI's low-power and high-performance MCUs, with wired and wireless connectivity options, are optimized for a broad range of applications.

Products for MSP430 Ultra-Low-Power Microcontrollers One platform. One ecosystem. Endless possibilities. Enabling the connected world with innovations in ultra-low-power microcontrollers with advanced peripherals for precise sensing and measurement.

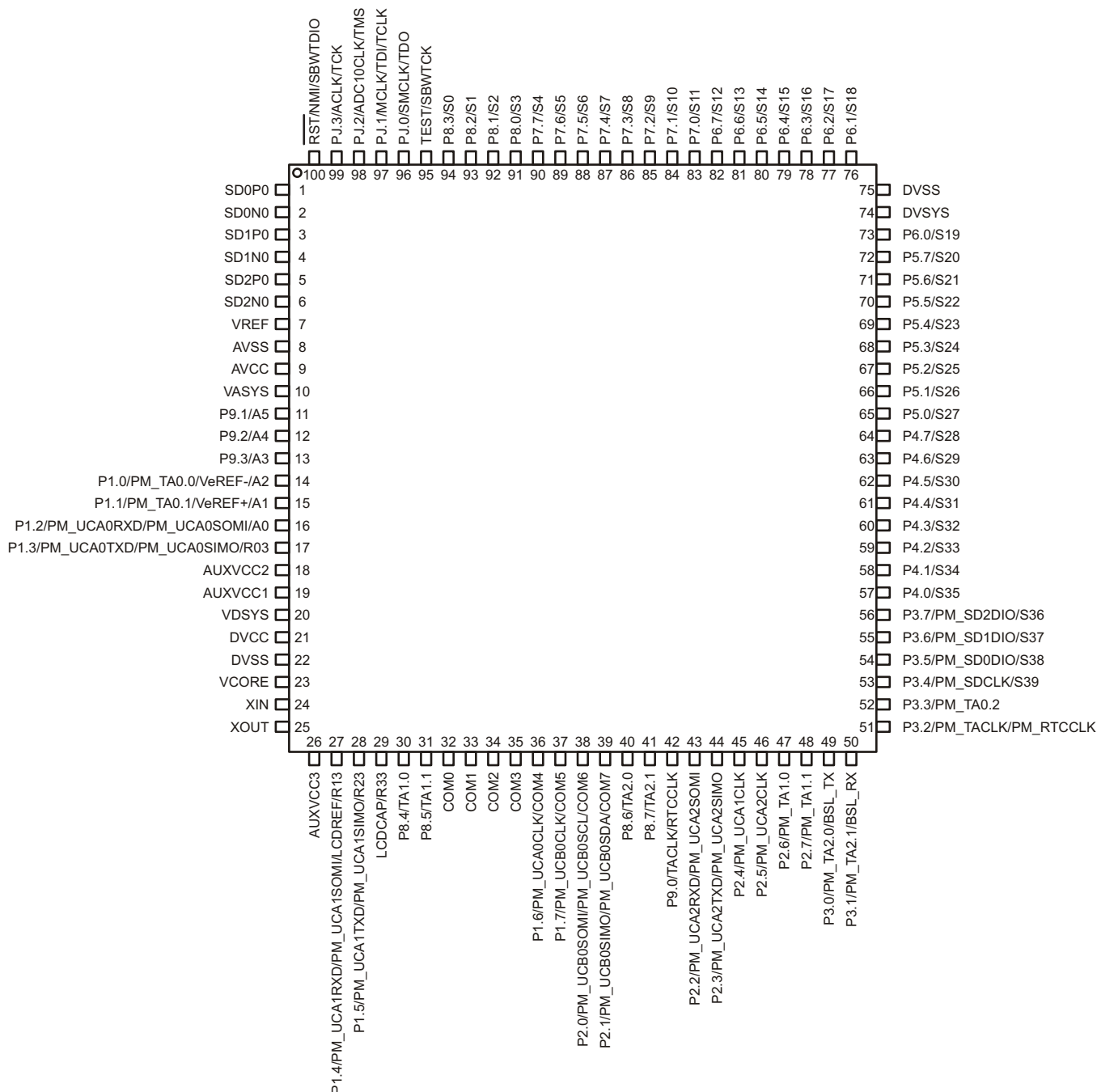
Companion Products for MSP430F6736A Review products that are frequently purchased or used with this product.

Reference Designs for MSP430F6736A The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the 100-pin PZ package. See Table 4-1 for differences between the MSP430F673xA and MSP430F672xA devices in this package.



NOTE: The secondary digital functions on Ports P1, P2, and P3 are fully mappable. This pinout shows the default mapping. See 6.11.6 for details.

NOTE: The pins VDSYS and DVSYS must be connected externally on board for proper device operation.

CAUTION: The LDCAP/R33 pin must be connected to DVSS if not used.

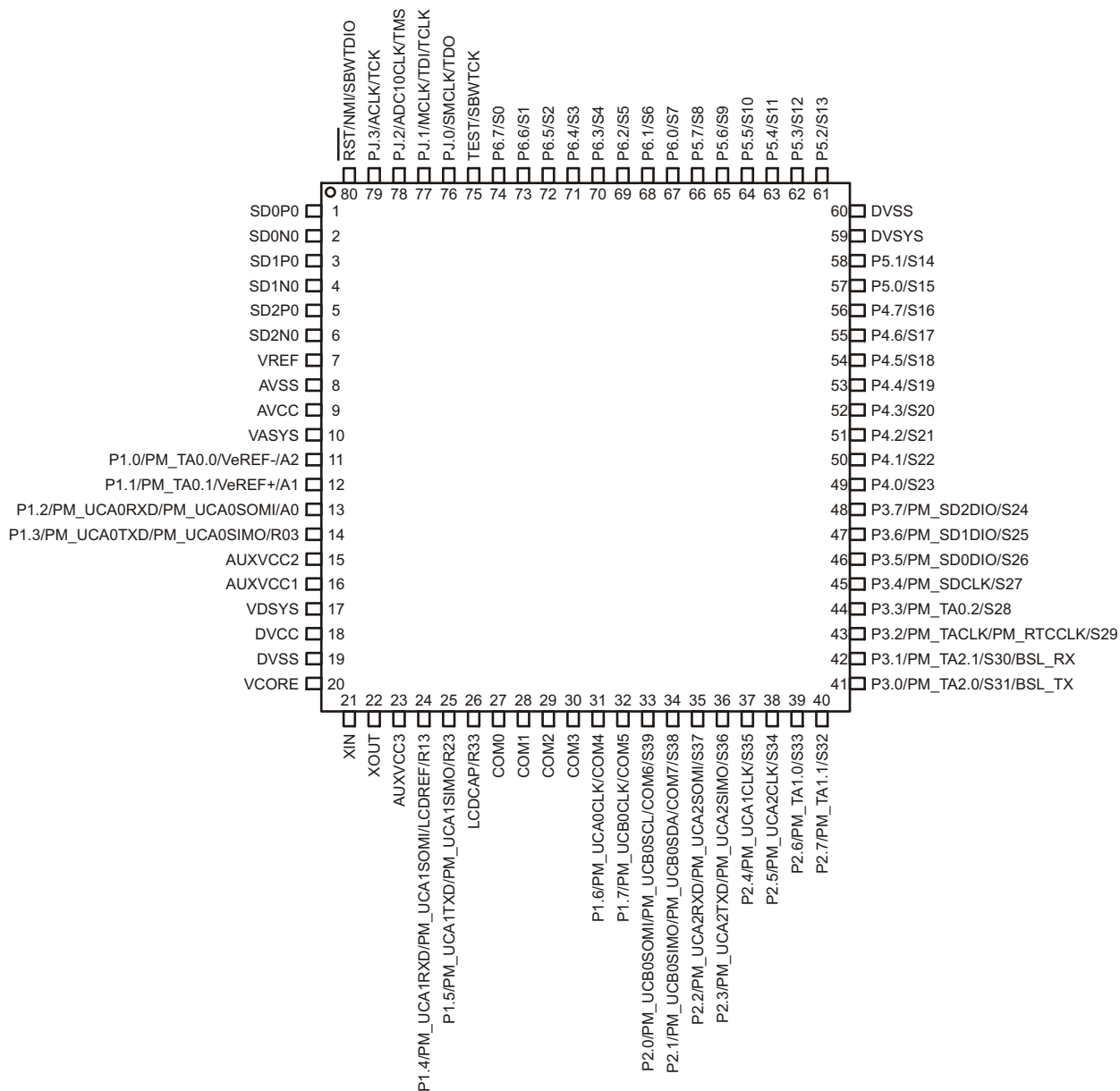
Figure 4-1. 100-Pin PZ Package (Top View)

Table 4-1. Pinout Differences Between MSP430F673xAIPZ and MSP430F672xAIPZ⁽¹⁾

| PIN NUMBER | PIN NAME | |
|------------|--------------------|--------------------|
| | MSP430F673xAIPZ | MSP430F672xAIPZ |
| 1 | SD0P0 | SD0P0 |
| 2 | SD0N0 | SD0N0 |
| 3 | SD1P0 | SD1P0 |
| 4 | SD1N0 | SD1N0 |
| 5 | <i>SD2P0</i> | NC |
| 6 | <i>SD2N0</i> | NC |
| 7 | VREF | VREF |
| 53 | P3.4/PM_SDCLK/S39 | P3.4/PM_SDCLK/S39 |
| 54 | P3.5/PM_SD0DIO/S38 | P3.5/PM_SD0DIO/S38 |
| 55 | P3.6/PM_SD1DIO/S37 | P3.6/PM_SD1DIO/S37 |
| 56 | P3.7/PM_SD2DIO/S36 | P3.7/PM_NONE/S36 |

(1) Signal names that differ between devices are indicated by *italic* typeface.

Figure 4-2 shows the pinout for the 80-pin PN package. See Table 4-2 for differences between the MSP430F673xA and MSP430F672xA devices in this package.



NOTE: The secondary digital functions on Ports P1, P2, and P3 are fully mappable. This pinout shows the default mapping. See § 6.11.6 for details.

NOTE: The pins VDSYS and DVSSYS must be connected externally on board for proper device operation.

CAUTION: The LDCAP/R33 pin must be connected to DVSS if not used.

Figure 4-2. 80-Pin PN Package (Top View)

Table 4-2. Pinout Differences Between MSP430F673xAIPN and MSP430F672xAIPN⁽¹⁾

| PIN NUMBER | PIN NAME | |
|------------|--------------------|--------------------|
| | MSP430F673xAIPN | MSP430F672xAIPN |
| 1 | SD0P0 | SD0P0 |
| 2 | SD0N0 | SD0N0 |
| 3 | SD1P0 | SD1P0 |
| 4 | SD1N0 | SD1N0 |
| 5 | <i>SD2P0</i> | NC |
| 6 | <i>SD2N0</i> | NC |
| 7 | VREF | VREF |
| 45 | P3.4/PM_SDCLK/S27 | P3.4/PM_SDCLK/S27 |
| 46 | P3.5/PM_SD0DIO/S26 | P3.5/PM_SD0DIO/S26 |
| 47 | P3.6/PM_SD1DIO/S25 | P3.6/PM_SD1DIO/S25 |
| 48 | P3.7/PM_SD2DIO/S24 | P3.7/PM_NONE/S24 |

(1) Signal names that differ between devices are indicated by *italic* typeface.

4.2 Pin Attributes

Table 4-3 lists the pin attributes for all device variants in the PZ package. For the PN package, see Table 4-4.

Table 4-3. Pin Attributes, PZ Package

| PIN NO. | SIGNAL NAME ^{(1) (2)} | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|--------------------------------|----------------------------|----------------------------|--------------|--------------------------------------|
| 1 | SD0P0 | I | Analog | AVCC | OFF |
| 2 | SD0N0 | I | Analog | AVCC | OFF |
| 3 | SD1P0 | I | Analog | AVCC | OFF |
| 4 | SD1N0 | I | Analog | AVCC | OFF |
| 5 | SD2P0 | I | Analog | AVCC | OFF |
| 6 | SD2N0 | I | Analog | AVCC | OFF |
| 7 | VREF | I | Analog | – | OFF |
| 8 | AVSS | P | Power | – | N/A |
| 9 | AVCC | P | Power | – | N/A |
| 10 | VASYS | P | Power | – | N/A |
| 11 | P9.1 | I/O | LVC MOS | DVCC | OFF |
| | A5 | I | Analog | AVCC | – |
| 12 | P9.2 | I/O | LVC MOS | DVCC | OFF |
| | A4 | I | Analog | AVCC | – |
| 13 | P9.3 | I/O | LVC MOS | DVCC | OFF |
| | A3 | I | Analog | AVCC | – |
| 14 | P1.0 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA0.0 | I/O | LVC MOS | DVCC | – |
| | VeREF- | I | Power | – | N/A |
| | A2 | I | Analog | AVCC | – |
| 15 | P1.1 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA0.1 | I/O | LVC MOS | DVCC | – |
| | VeREF+ | I | Power | – | N/A |
| | A1 | I | Analog | AVCC | – |
| 16 | P1.2 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA0RXD | I | LVC MOS | DVCC | – |
| | PM_UCA0SOMI | I/O | LVC MOS | DVCC | – |
| | A0 | I | Analog | AVCC | – |
| 17 | P1.3 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA0TXD | O | LVC MOS | DVCC | – |
| | PM_UCA0SIMO | I/O | LVC MOS | DVCC | – |
| | R03 | I/O | Analog | AVCC | – |
| 18 | AUXVCC2 | P | Power | – | N/A |
| 19 | AUXVCC1 | P | Power | – | N/A |
| 20 | VDSYS | P | Power | – | N/A |
| 21 | DVCC | P | Power | – | N/A |
| 22 | DVSS | P | Power | – | N/A |

- (1) For each multiplexed pin, the signal that is listed first in this table is the default after reset.
- (2) To determine the pin mux encodings for each pin, refer to [§ 6.12, Input/Output Diagrams](#).
- (3) Signal Types: I = Input, O = Output, I/O = Input or Output.
- (4) Buffer Types: LVC MOS, Analog, or Power (see [Table 4-7, Buffer Type](#))
- (5) Reset States:
OFF = High-impedance input with pullup or pulldown disabled (if available)
N/A = Not applicable

Table 4-3. Pin Attributes, PZ Package (continued)

| PIN NO. | SIGNAL NAME ^{(1) (2)} | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|--------------------------------|----------------------------|----------------------------|--------------|--------------------------------------|
| 23 | VCORE | P | Power | – | N/A |
| 24 | XIN | I | LVC MOS | DVCC | OFF |
| 25 | XOUT | O | LVC MOS | DVCC | OFF |
| 26 | AUXVCC3 | P | Power | – | N/A |
| 27 | P1.4 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA1RXD | I | LVC MOS | DVCC | – |
| | PM_UCA1SOMI | I/O | LVC MOS | DVCC | – |
| | LCDREF | I | Analog | AVCC | – |
| | R13 | I/O | Analog | AVCC | – |
| 28 | P1.5 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA1TXD | O | LVC MOS | DVCC | – |
| | PM_UCA1SIMO | I/O | LVC MOS | DVCC | – |
| | R23 | I/O | Analog | AVCC | – |
| 29 | LCDCAP | I/O | Analog | AVCC | OFF |
| | R33 | I/O | Analog | AVCC | – |
| 30 | P8.4 | I/O | LVC MOS | DVCC | OFF |
| | TA1.0 | I/O | LVC MOS | DVCC | – |
| 31 | P8.5 | I/O | LVC MOS | DVCC | OFF |
| | TA1.1 | I/O | LVC MOS | DVCC | – |
| 32 | COM0 | O | LVC MOS | DVCC | OFF |
| 33 | COM1 | O | LVC MOS | DVCC | OFF |
| 34 | COM2 | O | LVC MOS | DVCC | OFF |
| 35 | COM3 | O | LVC MOS | DVCC | OFF |
| 36 | P1.6 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA0CLK | I/O | LVC MOS | DVCC | – |
| | COM4 | O | LVC MOS | DVCC | – |
| 37 | P1.7 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCB0CLK | I/O | LVC MOS | DVCC | – |
| | COM5 | O | LVC MOS | DVCC | – |
| 38 | P2.0 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCB0SOMI | I/O | LVC MOS | DVCC | – |
| | PM_UCB0SCL | I/O | LVC MOS | DVCC | – |
| | COM6 | O | LVC MOS | DVCC | – |
| 39 | P2.1 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCB0SIMO | I/O | LVC MOS | DVCC | – |
| | PM_UCB0SDA | I/O | LVC MOS | DVCC | – |
| | COM7 | O | LVC MOS | DVCC | – |
| 40 | P8.6 | I/O | LVC MOS | DVCC | OFF |
| | TA2.0 | I/O | LVC MOS | DVCC | – |
| 41 | P8.7 | I/O | LVC MOS | DVCC | OFF |
| | TA2.1 | I/O | LVC MOS | DVCC | – |
| 42 | P9.0 | I/O | LVC MOS | DVCC | OFF |
| | TACLK | I | LVC MOS | DVCC | – |
| | RTCCLK | O | LVC MOS | DVCC | – |
| 43 | P2.2 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA2RXD | I | LVC MOS | DVCC | – |
| | PM_UCA2SOMI | I/O | LVC MOS | DVCC | – |

Table 4-3. Pin Attributes, PZ Package (continued)

| PIN NO. | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|---|----------------------------|----------------------------|--------------|--------------------------------------|
| 44 | P2.3 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA2TXD | O | LVC MOS | DVCC | – |
| | PM_UCA2SIMO | I/O | LVC MOS | DVCC | – |
| 45 | P2.4 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA1CLK | I/O | LVC MOS | DVCC | – |
| 46 | P2.5 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA2CLK | I/O | LVC MOS | DVCC | – |
| 47 | P2.6 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA1.0 | I/O | LVC MOS | DVCC | – |
| 48 | P2.7 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA1.1 | I/O | LVC MOS | DVCC | – |
| 49 | P3.0 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA2.0 | I/O | LVC MOS | DVCC | – |
| | BSL_TX | O | LVC MOS | DVCC | – |
| 50 | P3.1 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA2.1 | I/O | LVC MOS | DVCC | – |
| | BSL_RX | I | LVC MOS | DVCC | – |
| 51 | P3.2 | I/O | LVC MOS | DVCC | OFF |
| | PM_TACLK | I | LVC MOS | DVCC | – |
| | PM_RTCCLK | O | LVC MOS | DVCC | – |
| 52 | P3.3 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA0.2 | I/O | LVC MOS | DVCC | – |
| 53 | P3.4 | I/O | LVC MOS | DVCC | OFF |
| | PM_SDCLK | I/O | LVC MOS | DVCC | – |
| | S39 | O | LVC MOS | DVCC | – |
| 54 | P3.5 | I/O | LVC MOS | DVCC | OFF |
| | PM_SD0DIO | I/O | Analog | AVCC | – |
| | S38 | O | LVC MOS | DVCC | – |
| 55 | P3.6 | I/O | LVC MOS | DVCC | OFF |
| | PM_SD1DIO | I/O | Analog | AVCC | – |
| | S37 | O | LVC MOS | DVCC | – |
| 56 | P3.7 | I/O | LVC MOS | DVCC | OFF |
| | PM_SD2DIO | I/O | LVC MOS | DVCC | – |
| | S36 | O | LVC MOS | DVCC | – |
| 57 | P4.0 | I/O | LVC MOS | DVCC | OFF |
| | S35 | O | LVC MOS | DVCC | – |
| 58 | P4.1 | I/O | LVC MOS | DVCC | OFF |
| | S34 | O | LVC MOS | DVCC | – |
| 59 | P4.2 | I/O | LVC MOS | DVCC | OFF |
| | S33 | O | LVC MOS | DVCC | – |
| 60 | P4.3 | I/O | LVC MOS | DVCC | OFF |
| | S32 | O | LVC MOS | DVCC | – |
| 61 | P4.4 | I/O | LVC MOS | DVCC | OFF |
| | S31 | O | LVC MOS | DVCC | – |
| 62 | P4.5 | I/O | LVC MOS | DVCC | OFF |
| | S30 | O | LVC MOS | DVCC | – |

Table 4-3. Pin Attributes, PZ Package (continued)

| PIN NO. | SIGNAL NAME ⁽¹⁾ ⁽²⁾ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|---|----------------------------|----------------------------|--------------|--------------------------------------|
| 63 | P4.6 | I/O | LVC MOS | DVCC | OFF |
| | S29 | O | LVC MOS | DVCC | – |
| 64 | P4.7 | I/O | LVC MOS | DVCC | OFF |
| | S28 | O | LVC MOS | DVCC | – |
| 65 | P5.0 | I/O | LVC MOS | DVCC | OFF |
| | S27 | O | LVC MOS | DVCC | – |
| 66 | P5.1 | I/O | LVC MOS | DVCC | OFF |
| | S26 | O | LVC MOS | DVCC | – |
| 67 | P5.2 | I/O | LVC MOS | DVCC | OFF |
| | S25 | O | LVC MOS | DVCC | – |
| 68 | P5.3 | I/O | LVC MOS | DVCC | OFF |
| | S24 | O | LVC MOS | DVCC | – |
| 69 | P5.4 | I/O | LVC MOS | DVCC | OFF |
| | S23 | O | LVC MOS | DVCC | – |
| 70 | P5.5 | I/O | LVC MOS | DVCC | OFF |
| | S22 | O | LVC MOS | DVCC | – |
| 71 | P5.6 | I/O | LVC MOS | DVCC | OFF |
| | S21 | O | LVC MOS | DVCC | – |
| 72 | P5.7 | I/O | LVC MOS | DVCC | OFF |
| | S20 | O | LVC MOS | DVCC | – |
| 73 | P6.0 | I/O | LVC MOS | DVCC | OFF |
| | S19 | O | LVC MOS | DVCC | – |
| 74 | DVSS | P | Power | – | N/A |
| 75 | DVSS | P | Power | – | N/A |
| 76 | P6.1 | I/O | LVC MOS | DVCC | OFF |
| | S18 | O | LVC MOS | DVCC | – |
| 77 | P6.2 | I/O | LVC MOS | DVCC | OFF |
| | S17 | O | LVC MOS | DVCC | – |
| 78 | P6.3 | I/O | LVC MOS | DVCC | OFF |
| | S16 | O | LVC MOS | DVCC | – |
| 79 | P6.4 | I/O | LVC MOS | DVCC | OFF |
| | S15 | O | LVC MOS | DVCC | – |
| 80 | P6.5 | I/O | LVC MOS | DVCC | OFF |
| | S14 | O | LVC MOS | DVCC | – |
| 81 | P6.6 | I/O | LVC MOS | DVCC | OFF |
| | S13 | O | LVC MOS | DVCC | – |
| 82 | P6.7 | I/O | LVC MOS | DVCC | OFF |
| | S12 | O | LVC MOS | DVCC | – |
| 83 | P7.0 | I/O | LVC MOS | DVCC | OFF |
| | S11 | O | LVC MOS | DVCC | – |
| 84 | P7.1 | I/O | LVC MOS | DVCC | OFF |
| | S10 | O | LVC MOS | DVCC | – |
| 85 | P7.2 | I/O | LVC MOS | DVCC | OFF |
| | S9 | O | LVC MOS | DVCC | – |
| 86 | P7.3 | I/O | LVC MOS | DVCC | OFF |
| | S8 | O | LVC MOS | DVCC | – |

Table 4-3. Pin Attributes, PZ Package (continued)

| PIN NO. | SIGNAL NAME ^{(1) (2)} | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|--------------------------------|----------------------------|----------------------------|--------------|--------------------------------------|
| 87 | P7.4 | I/O | LVC MOS | DVCC | OFF |
| | S7 | O | LVC MOS | DVCC | – |
| 88 | P7.5 | I/O | LVC MOS | DVCC | OFF |
| | S6 | O | LVC MOS | DVCC | – |
| 89 | P7.6 | I/O | LVC MOS | DVCC | OFF |
| | S5 | O | LVC MOS | DVCC | – |
| 90 | P7.7 | I/O | LVC MOS | DVCC | OFF |
| | S4 | O | LVC MOS | DVCC | – |
| 91 | P8.0 | I/O | LVC MOS | DVCC | OFF |
| | S3 | O | LVC MOS | DVCC | – |
| 92 | P8.1 | I/O | LVC MOS | DVCC | OFF |
| | S2 | O | LVC MOS | DVCC | – |
| 93 | P8.2 | I/O | LVC MOS | DVCC | OFF |
| | S1 | O | LVC MOS | DVCC | – |
| 94 | P8.3 | I/O | LVC MOS | DVCC | OFF |
| | S0 | O | LVC MOS | DVCC | – |
| 95 | TEST | I | LVC MOS | DVCC | OFF |
| | SBWTCK | I | LVC MOS | DVCC | – |
| 96 | PJ.0 | I/O | LVC MOS | DVCC | OFF |
| | SMCLK | O | LVC MOS | DVCC | – |
| | TDO | O | LVC MOS | DVCC | – |
| 97 | PJ.1 | I/O | LVC MOS | DVCC | OFF |
| | MCLK | O | LVC MOS | DVCC | – |
| | TDI | I | LVC MOS | DVCC | – |
| | TCLK | I | LVC MOS | DVCC | – |
| 98 | PJ.2 | I/O | LVC MOS | DVCC | OFF |
| | ADC10CLK | O | LVC MOS | DVCC | – |
| | TMS | I | LVC MOS | DVCC | – |
| 99 | PJ.3 | I/O | LVC MOS | DVCC | OFF |
| | ACLK | O | LVC MOS | DVCC | – |
| | TCK | I | LVC MOS | DVCC | – |
| 100 | RST | I | LVC MOS | DVCC | PU |
| | NMI | I | LVC MOS | DVCC | – |
| | SBWTDIO | I/O | LVC MOS | DVCC | – |

Table 4-4 lists the pin attributes for all device variants in the PN package. For the PZ package, see Table 4-3.

Table 4-4. Pin Attributes, PN Package

| PIN NO. | SIGNAL NAME ⁽¹⁾ ₍₂₎ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|--|----------------------------|----------------------------|--------------|--------------------------------------|
| 1 | SD0P0 | I | Analog | AVCC | OFF |
| 2 | SD0N0 | I | Analog | AVCC | OFF |
| 3 | SD1P0 | I | Analog | AVCC | OFF |
| 4 | SD1N0 | I | Analog | AVCC | OFF |
| 5 | SD2P0 | I | Analog | AVCC | OFF |
| 6 | SD2N0 | I | Analog | AVCC | OFF |
| 7 | VREF | I | Power | – | N/A |
| 8 | AVSS | P | Power | – | N/A |
| 9 | AVCC | P | Power | – | N/A |
| 10 | VASYS | P | Power | – | N/A |
| 11 | P1.0 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA0.0 | I/O | LVC MOS | DVCC | – |
| | VeREF- | I | Power | – | – |
| | A2 | I | Analog | AVCC | – |
| 12 | P1.1 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA0.1 | I/O | LVC MOS | DVCC | – |
| | VeREF+ | I | Power | – | – |
| | A1 | I | Analog | AVCC | – |
| 13 | P1.2 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA0RXD | I | LVC MOS | DVCC | – |
| | PM_UCA0SOMI | I/O | LVC MOS | DVCC | – |
| | A0 | I | Analog | AVCC | – |
| 14 | P1.3 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA0TXD | O | LVC MOS | DVCC | – |
| | PM_UCA0SIMO | I/O | LVC MOS | DVCC | – |
| | R03 | I/O | Analog | AVCC | – |
| 15 | AUXVCC2 | P | Power | – | N/A |
| 16 | AUXVCC1 | P | Power | – | N/A |
| 17 | VDSYS | P | Power | – | N/A |
| 18 | DVCC | P | Power | – | N/A |
| 19 | DVSS | P | Power | – | N/A |
| 20 | VCORE | P | Power | – | N/A |
| 21 | XIN | I | LVC MOS | DVCC | OFF |
| 22 | XOUT | O | LVC MOS | DVCC | OFF |
| 23 | AUXVCC3 | P | Power | – | N/A |

- (1) For each multiplexed pin, the signal that is listed first in this table is the default after reset.
 (2) To determine the pin mux encodings for each pin, refer to [§ 6.12, Input/Output Diagrams](#).
 (3) Signal Types: I = Input, O = Output, I/O = Input or Output.
 (4) Buffer Types: LVC MOS, Analog, or Power (see [Table 4-7, Buffer Type](#))
 (5) Reset States:
 OFF = High-impedance input with pullup or pulldown disabled (if available)
 N/A = Not applicable

Table 4-4. Pin Attributes, PN Package (continued)

| PIN NO. | SIGNAL NAME ⁽¹⁾ ₍₂₎ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|--|----------------------------|----------------------------|--------------|--------------------------------------|
| 24 | P1.4 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA1RXD | I | LVC MOS | DVCC | – |
| | PM_UCA1SOMI | I/O | LVC MOS | DVCC | – |
| | LCDREF | I | Analog | AVCC | – |
| | R13 | I/O | Analog | AVCC | – |
| 25 | P1.5 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA1TXD | O | LVC MOS | DVCC | – |
| | PM_UCA1SIMO | I/O | LVC MOS | DVCC | – |
| | R23 | I/O | Analog | AVCC | – |
| 26 | LDCAP | I/O | Analog | AVCC | OFF |
| | R33 | I/O | Analog | AVCC | OFF |
| 27 | COM0 | O | LVC MOS | DVCC | OFF |
| 28 | COM1 | O | LVC MOS | DVCC | OFF |
| 29 | COM2 | O | LVC MOS | DVCC | OFF |
| 30 | COM3 | O | LVC MOS | DVCC | OFF |
| 31 | P1.6 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA0CLK | I/O | LVC MOS | DVCC | – |
| | COM4 | O | LVC MOS | DVCC | – |
| 32 | P1.7 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCB0CLK | I/O | LVC MOS | DVCC | – |
| | COM5 | O | LVC MOS | DVCC | – |
| 33 | P2.0 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCB0SOMI | I/O | LVC MOS | DVCC | – |
| | PM_UCB0SCL | I/O | LVC MOS | DVCC | – |
| | COM6 | O | LVC MOS | DVCC | – |
| | S39 | O | LVC MOS | DVCC | – |
| 34 | P2.1 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCB0SIMO | I/O | LVC MOS | DVCC | – |
| | PM_UCB0SDA | I/O | LVC MOS | DVCC | – |
| | COM7 | O | LVC MOS | DVCC | – |
| | S38 | O | LVC MOS | DVCC | – |
| 35 | P2.2 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA2RXD | I | LVC MOS | DVCC | – |
| | PM_UCA2SOMI | I/O | LVC MOS | DVCC | – |
| | S37 | O | LVC MOS | DVCC | – |
| 36 | P2.3 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA2TXD | O | LVC MOS | DVCC | – |
| | PM_UCA2SIMO | I/O | LVC MOS | DVCC | – |
| | S36 | O | LVC MOS | DVCC | – |
| 37 | P2.4 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA1CLK | I/O | LVC MOS | DVCC | – |
| | S35 | O | LVC MOS | DVCC | – |
| 38 | P2.5 | I/O | LVC MOS | DVCC | OFF |
| | PM_UCA2CLK | I/O | LVC MOS | DVCC | – |
| | S34 | O | LVC MOS | DVCC | – |

Table 4-4. Pin Attributes, PN Package (continued)

| PIN NO. | SIGNAL NAME ⁽¹⁾ ₍₂₎ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|--|----------------------------|----------------------------|--------------|--------------------------------------|
| 39 | P2.6 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA1.0 | I/O | LVC MOS | DVCC | – |
| | S33 | O | LVC MOS | DVCC | – |
| 40 | P2.7 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA1.1 | I/O | LVC MOS | DVCC | – |
| | S32 | O | LVC MOS | DVCC | – |
| 41 | P3.0 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA2.0 | I/O | LVC MOS | DVCC | – |
| | S31 | O | LVC MOS | DVCC | – |
| | BSL_TX | O | LVC MOS | DVCC | – |
| 42 | P3.1 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA2.1 | I/O | LVC MOS | DVCC | – |
| | S30 | O | LVC MOS | DVCC | – |
| | BSL_RX | I | LVC MOS | DVCC | – |
| 43 | P3.2 | I/O | LVC MOS | DVCC | OFF |
| | PM_TACLK | I | LVC MOS | DVCC | – |
| | PM_RTCCLK | O | LVC MOS | DVCC | – |
| | S29 | O | LVC MOS | DVCC | – |
| 44 | P3.3 | I/O | LVC MOS | DVCC | OFF |
| | PM_TA0.2 | I/O | LVC MOS | DVCC | – |
| | S28 | O | LVC MOS | DVCC | – |
| 45 | P3.4 | I/O | LVC MOS | DVCC | OFF |
| | PM_SDCLK | I/O | LVC MOS | DVCC | – |
| | S27 | O | LVC MOS | DVCC | – |
| 46 | P3.5 | I/O | LVC MOS | DVCC | OFF |
| | PM_SD0DIO | I/O | LVC MOS | DVCC | – |
| | S26 | O | LVC MOS | DVCC | – |
| 47 | P3.6 | I/O | LVC MOS | DVCC | OFF |
| | PM_SD1DIO | I/O | LVC MOS | DVCC | – |
| | S25 | O | LVC MOS | DVCC | – |
| 48 | P3.7 | I/O | LVC MOS | DVCC | OFF |
| | PM_SD2DIO | I/O | LVC MOS | DVCC | – |
| | S24 | O | LVC MOS | DVCC | – |
| 49 | P4.0 | I/O | LVC MOS | DVCC | OFF |
| | S23 | O | LVC MOS | DVCC | – |
| 50 | P4.1 | I/O | LVC MOS | DVCC | OFF |
| | S22 | O | LVC MOS | DVCC | – |
| 51 | P4.2 | I/O | LVC MOS | DVCC | OFF |
| | S21 | O | LVC MOS | DVCC | – |
| 52 | P4.3 | I/O | LVC MOS | DVCC | OFF |
| | S20 | O | LVC MOS | DVCC | – |
| 53 | P4.4 | I/O | LVC MOS | DVCC | OFF |
| | S19 | O | LVC MOS | DVCC | – |
| 54 | P4.5 | I/O | LVC MOS | DVCC | OFF |
| | S18 | O | LVC MOS | DVCC | – |
| 55 | P4.6 | I/O | LVC MOS | DVCC | OFF |
| | S17 | O | LVC MOS | DVCC | – |

Table 4-4. Pin Attributes, PN Package (continued)

| PIN NO. | SIGNAL NAME ⁽¹⁾ ₍₂₎ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|--|----------------------------|----------------------------|--------------|--------------------------------------|
| 56 | P4.7 | I/O | LVC MOS | DVCC | OFF |
| | S16 | O | LVC MOS | DVCC | – |
| 57 | P5.0 | I/O | LVC MOS | DVCC | OFF |
| | S15 | O | LVC MOS | DVCC | – |
| 58 | P5.1 | I/O | LVC MOS | DVCC | OFF |
| | S14 | O | LVC MOS | DVCC | – |
| 59 | DVSYS | P | Power | – | N/A |
| 60 | DVSS | P | Power | – | N/A |
| 61 | P5.2 | I/O | LVC MOS | DVCC | OFF |
| | S13 | O | LVC MOS | DVCC | – |
| 62 | P5.3 | I/O | LVC MOS | DVCC | OFF |
| | S12 | O | LVC MOS | DVCC | – |
| 63 | P5.4 | I/O | LVC MOS | DVCC | OFF |
| | S11 | O | LVC MOS | DVCC | – |
| 64 | P5.5 | I/O | LVC MOS | DVCC | OFF |
| | S10 | O | LVC MOS | DVCC | – |
| 65 | P5.6 | I/O | LVC MOS | DVCC | OFF |
| | S9 | O | LVC MOS | DVCC | – |
| 66 | P5.7 | I/O | LVC MOS | DVCC | OFF |
| | S8 | O | LVC MOS | DVCC | – |
| 67 | P6.0 | I/O | LVC MOS | DVCC | OFF |
| | S7 | O | LVC MOS | DVCC | – |
| 68 | P6.1 | I/O | LVC MOS | DVCC | OFF |
| | S6 | O | LVC MOS | DVCC | – |
| 69 | P6.2 | I/O | LVC MOS | DVCC | OFF |
| | S5 | O | LVC MOS | DVCC | – |
| 70 | P6.3 | I/O | LVC MOS | DVCC | OFF |
| | S4 | O | LVC MOS | DVCC | – |
| 71 | P6.4 | I/O | LVC MOS | DVCC | OFF |
| | S3 | O | LVC MOS | DVCC | – |
| 72 | P6.5 | I/O | LVC MOS | DVCC | OFF |
| | S2 | O | LVC MOS | DVCC | – |
| 73 | P6.6 | I/O | LVC MOS | DVCC | OFF |
| | S1 | O | LVC MOS | DVCC | – |
| 74 | P6.7 | I/O | LVC MOS | DVCC | OFF |
| | S0 | O | LVC MOS | DVCC | – |
| 75 | TEST | I | LVC MOS | DVCC | OFF |
| | SBWTCK | I | LVC MOS | DVCC | – |
| 76 | PJ.0 | I/O | LVC MOS | DVCC | OFF |
| | SMCLK | O | LVC MOS | DVCC | – |
| | TDO | O | LVC MOS | DVCC | – |
| 77 | PJ.1 | I/O | LVC MOS | DVCC | OFF |
| | MCLK | O | LVC MOS | DVCC | – |
| | TDI | I | LVC MOS | DVCC | – |
| | TCLK | I | LVC MOS | DVCC | – |

Table 4-4. Pin Attributes, PN Package (continued)

| PIN NO. | SIGNAL NAME ⁽¹⁾ ₍₂₎ | SIGNAL TYPE ⁽³⁾ | BUFFER TYPE ⁽⁴⁾ | POWER SOURCE | RESET STATE AFTER BOR ⁽⁵⁾ |
|---------|--|----------------------------|----------------------------|--------------|---|
| 78 | PJ.2 | I/O | LVC MOS | DVCC | OFF |
| | ADC10CLK | O | LVC MOS | DVCC | – |
| | TMS | I | LVC MOS | DVCC | – |
| 79 | PJ.3 | I/O | LVC MOS | DVCC | OFF |
| | ACLK | O | LVC MOS | DVCC | – |
| | TCK | I | LVC MOS | DVCC | – |
| 80 | $\overline{\text{RST}}$ | I/O | LVC MOS | DVCC | PU |
| | NMI | I | LVC MOS | DVCC | – |
| | SBWTDIO | I/O | LVC MOS | DVCC | – |

4.3 Signal Descriptions

Table 4-5 describes the signals for all device variants in the PZ package. See Table 4-6 for signal descriptions in the PN package.

Table 4-5. Signal Descriptions, PZ Package

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE | DESCRIPTION |
|----------|-------------|---------|-------------|---|
| ADC10 | A0 | 16 | I | Analog input A0 for 10-bit ADC |
| | A1 | 15 | I | Analog input A1 for 10-bit ADC |
| | A2 | 14 | I | Analog input A2 for 10-bit ADC |
| | A3 | 13 | I | Analog input A3 for 10-bit ADC |
| | A4 | 12 | I | Analog input A4 for 10-bit ADC |
| | A5 | 11 | I | Analog input A5 for 10-bit ADC |
| | ADC10CLK | 98 | O | ADC10_A clock output |
| | VeREF+ | 15 | I | Positive terminal for the ADC reference voltage for an external applied reference voltage |
| | VeREF- | 14 | I | Negative terminal for the ADC reference voltage for an external applied reference voltage |
| BSL | BSL_RX | 50 | I | Bootloader data receive |
| | BSL_TX | 49 | O | Bootloader data transmit |
| Clock | ACLK | 99 | O | ACLK clock output |
| | MCLK | 97 | O | MCLK clock output |
| | PM_RTCCLK | 51 | O | Default mapping: RTCCLK clock output |
| | RTCCLK | 42 | O | RTCCLK clock output |
| | SMCLK | 96 | O | SMCLK clock output |
| | XIN | 24 | I | Input terminal for crystal oscillator |
| | XOUT | 25 | O | Output terminal for crystal oscillator |
| Debug | SBWTCK | 95 | I | Spy-Bi-Wire input clock |
| | SBWTDIO | 100 | I/O | Spy-Bi-Wire data input/output |
| | TCK | 99 | I | Test clock |
| | TCLK | 97 | I | Test clock input |
| | TDI | 97 | I | Test data input |
| | TDO | 96 | O | Test data output |
| | TEST | 95 | I | Test mode pin – select digital I/O on JTAG pins |
| | TMS | 98 | I | Test mode select |
| GPIO | P1.0 | 14 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.1 | 15 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.2 | 16 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.3 | 17 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.4 | 27 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.5 | 28 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.6 | 36 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.7 | 37 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |

Table 4-5. Signal Descriptions, PZ Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE | DESCRIPTION |
|----------|-------------|---------|-----------------------------|---|
| GPIO | P2.0 | 38 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.1 | 39 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.2 | 43 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.3 | 44 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.4 | 45 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.5 | 46 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.6 | 47 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.7 | 48 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P3.0 | 49 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.1 | 50 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.2 | 51 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.3 | 52 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.4 | 53 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.5 | 54 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.6 | 55 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.7 | 56 | I/O | General-purpose digital I/O with mappable secondary function |
| | P4.0 | 57 | I/O | General-purpose digital I/O |
| | P4.1 | 58 | I/O | General-purpose digital I/O |
| | P4.2 | 59 | I/O | General-purpose digital I/O |
| | P4.3 | 60 | I/O | General-purpose digital I/O |
| | P4.4 | 61 | I/O | General-purpose digital I/O |
| | P4.5 | 62 | I/O | General-purpose digital I/O |
| | P4.6 | 63 | I/O | General-purpose digital I/O |
| | P4.7 | 64 | I/O | General-purpose digital I/O |
| | P5.0 | 65 | I/O | General-purpose digital I/O |
| | P5.1 | 66 | I/O | General-purpose digital I/O |
| | P5.2 | 67 | I/O | General-purpose digital I/O |
| | P5.3 | 68 | I/O | General-purpose digital I/O |
| | P5.4 | 69 | I/O | General-purpose digital I/O |
| | P5.5 | 70 | I/O | General-purpose digital I/O |
| | P5.6 | 71 | I/O | General-purpose digital I/O |
| | P5.7 | 72 | I/O | General-purpose digital I/O |
| | P6.0 | 73 | I/O | General-purpose digital I/O |
| | P6.1 | 76 | I/O | General-purpose digital I/O |
| | P6.2 | 77 | I/O | General-purpose digital I/O |
| P6.3 | 78 | I/O | General-purpose digital I/O | |
| P6.4 | 79 | I/O | General-purpose digital I/O | |
| P6.5 | 80 | I/O | General-purpose digital I/O | |
| P6.6 | 81 | I/O | General-purpose digital I/O | |
| P6.7 | 82 | I/O | General-purpose digital I/O | |

Table 4-5. Signal Descriptions, PZ Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE | DESCRIPTION |
|------------------|-------------|---------|-----------------------------|---|
| GPIO | P7.0 | 83 | I/O | General-purpose digital I/O |
| | P7.1 | 84 | I/O | General-purpose digital I/O |
| | P7.2 | 85 | I/O | General-purpose digital I/O |
| | P7.3 | 86 | I/O | General-purpose digital I/O |
| | P7.4 | 87 | I/O | General-purpose digital I/O |
| | P7.5 | 88 | I/O | General-purpose digital I/O |
| | P7.6 | 89 | I/O | General-purpose digital I/O |
| | P7.7 | 90 | I/O | General-purpose digital I/O |
| | P8.0 | 91 | I/O | General-purpose digital I/O |
| | P8.1 | 92 | I/O | General-purpose digital I/O |
| | P8.2 | 93 | I/O | General-purpose digital I/O |
| | P8.3 | 94 | I/O | General-purpose digital I/O |
| | P8.4 | 30 | I/O | General-purpose digital I/O |
| | P8.5 | 31 | I/O | General-purpose digital I/O |
| | P8.6 | 40 | I/O | General-purpose digital I/O |
| | P8.7 | 41 | I/O | General-purpose digital I/O |
| | P9.0 | 42 | I/O | General-purpose digital I/O |
| | P9.1 | 11 | I/O | General-purpose digital I/O |
| | P9.2 | 12 | I/O | General-purpose digital I/O |
| | P9.3 | 13 | I/O | General-purpose digital I/O |
| PJ.0 | 96 | I/O | General-purpose digital I/O | |
| PJ.1 | 97 | I/O | General-purpose digital I/O | |
| PJ.2 | 98 | I/O | General-purpose digital I/O | |
| PJ.3 | 99 | I/O | General-purpose digital I/O | |
| I ² C | PM_UCB0SCL | 38 | I/O | Default mapping: eUSCI_B0 I ² C clock |
| | PM_UCB0SDA | 39 | I/O | Default mapping: eUSCI_B0 I ² C data |
| LCD | COM0 | 32 | O | LCD common output COM0 for LCD backplane |
| | COM1 | 33 | O | LCD common output COM1 for LCD backplane |
| | COM2 | 34 | O | LCD common output COM2 for LCD backplane |
| | COM3 | 35 | O | LCD common output COM3 for LCD backplane |
| | COM4 | 36 | O | LCD common output COM4 for LCD backplane |
| | COM5 | 37 | O | LCD common output COM5 for LCD backplane |
| | COM6 | 38 | O | LCD common output COM6 for LCD backplane |
| | COM7 | 39 | O | LCD common output COM7 for LCD backplane |
| | LDCAP | 29 | I/O | LCD capacitor connection CAUTION: This pin must be connected to DVSS if not used. |
| | LCDREF | 27 | I | External reference voltage input for regulated LCD voltage |
| | R03 | 17 | I/O | Input/output port of lowest analog LCD voltage (V5) |
| | R13 | 27 | I/O | Input/output port of third most positive analog LCD voltage (V3 or V4) |
| | R23 | 28 | I/O | Input/output port of second most positive analog LCD voltage (V2) |
| | R33 | 29 | I/O | Input/output port of most positive analog LCD voltage (V1) CAUTION: This pin must be connected to DVSS if not used. |

Table 4-5. Signal Descriptions, PZ Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE | DESCRIPTION |
|----------|-------------|---------|------------------------|------------------------|
| LCD | S0 | 94 | O | LCD segment output S0 |
| | S1 | 93 | O | LCD segment output S1 |
| | S2 | 92 | O | LCD segment output S2 |
| | S3 | 91 | O | LCD segment output S3 |
| | S4 | 90 | O | LCD segment output S4 |
| | S5 | 89 | O | LCD segment output S5 |
| | S6 | 88 | O | LCD segment output S6 |
| | S7 | 87 | O | LCD segment output S7 |
| | S8 | 86 | O | LCD segment output S8 |
| | S9 | 85 | O | LCD segment output S9 |
| | S10 | 84 | O | LCD segment output S10 |
| | S11 | 83 | O | LCD segment output S11 |
| | S12 | 82 | O | LCD segment output S12 |
| | S13 | 81 | O | LCD segment output S13 |
| | S14 | 80 | O | LCD segment output S14 |
| | S15 | 79 | O | LCD segment output S15 |
| | S16 | 78 | O | LCD segment output S16 |
| | S17 | 77 | O | LCD segment output S17 |
| | S18 | 76 | O | LCD segment output S18 |
| | S19 | 73 | O | LCD segment output S19 |
| | S20 | 72 | O | LCD segment output S20 |
| | S21 | 71 | O | LCD segment output S21 |
| | S22 | 70 | O | LCD segment output S22 |
| | S23 | 69 | O | LCD segment output S23 |
| | S24 | 68 | O | LCD segment output S24 |
| | S25 | 67 | O | LCD segment output S25 |
| | S26 | 66 | O | LCD segment output S26 |
| | S27 | 65 | O | LCD segment output S27 |
| | S28 | 64 | O | LCD segment output S28 |
| | S29 | 63 | O | LCD segment output S29 |
| | S30 | 62 | O | LCD segment output S30 |
| | S31 | 61 | O | LCD segment output S31 |
| | S32 | 60 | O | LCD segment output S32 |
| | S33 | 59 | O | LCD segment output S33 |
| | S34 | 58 | O | LCD segment output S34 |
| | S35 | 57 | O | LCD segment output S35 |
| | S36 | 56 | O | LCD segment output S36 |
| | S37 | 55 | O | LCD segment output S37 |
| | S38 | 54 | O | LCD segment output S38 |
| S39 | 53 | O | LCD segment output S39 | |

Table 4-5. Signal Descriptions, PZ Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE | DESCRIPTION |
|----------|----------------------|----------|-------------|--|
| Power | AUXVCC1 | 19 | P | Auxiliary power supply AUXVCC1 |
| | AUXVCC2 | 18 | P | Auxiliary power supply AUXVCC2 |
| | AUXVCC3 | 26 | P | Auxiliary power supply AUXVCC3 for back up subsystem |
| | AVCC | 9 | P | Analog power supply |
| | AVSS | 8 | P | Analog ground supply |
| | DVCC | 21 | P | Digital power supply |
| | DVSS | 22 75 | P | Digital ground supply |
| | DVSYN ⁽¹⁾ | 74 | P | Digital power supply for I/Os |
| | VASYS | 10 | P | Analog power supply selected among AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C _{VSYN} (see Table 5-18). |
| | VCORE ⁽²⁾ | 23 | P | Regulated core power supply (internal use only, no external current loading) |
| | VDSYS ⁽¹⁾ | 20 | P | Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C _{VSYN} (see Table 5-18). |
| SD24 | PM_SD0DIO | 54 | I/O | Default mapping: SD24_B converter 0 bit stream data input/output |
| | PM_SD1DIO | 55 | I/O | Default mapping: SD24_B converter 1 bit stream data input/output |
| | PM_SD2DIO | 56 | I/O | Default mapping: SD24_B converter 2 bit stream data input/output (not available on F672xA devices) |
| | PM_SDCLK | 53 | I/O | Default mapping: SD24_B bit stream clock input/output |
| | SD0N0 | 2 | I | SD24_B negative analog input for converter 0 ⁽³⁾ |
| | SD0P0 | 1 | I | SD24_B positive analog input for converter 0 ⁽³⁾ |
| | SD1N0 | 4 | I | SD24_B negative analog input for converter 1 ⁽³⁾ |
| | SD1P0 | 3 | I | SD24_B positive analog input for converter 1 ⁽³⁾ |
| | SD2N0 | 6 | I | SD24_B negative analog input for converter 2 ⁽³⁾ (not available on F672xA devices) |
| | SD2P0 | 5 | I | SD24_B positive analog input for converter 2 ⁽³⁾ (not available on F672xA devices) |
| | VREF | 7 | O | SD24_B external reference voltage |
| SPI | PM_UCA0CLK | 36 | I/O | Default mapping: eUSCI_A0 clock input/output |
| | PM_UCA0SIMO | 17 | I/O | Default mapping: eUSCI_A0 SPI slave in/master out |
| | PM_UCA0SOMI | 16 | I/O | Default mapping: eUSCI_A0 SPI slave out/master in |
| | PM_UCA1CLK | 45 | I/O | Default mapping: eUSCI_A1 clock input/output |
| | PM_UCA1SIMO | 28 | I/O | Default mapping: eUSCI_A1 SPI slave in/master out |
| | PM_UCA1SOMI | 27 | I/O | Default mapping: eUSCI_A1 SPI slave out/master in |
| | PM_UCA2CLK | 46 | I/O | Default mapping: eUSCI_A2 clock input/output |
| | PM_UCA2SIMO | 44 | I/O | Default mapping: eUSCI_A2 SPI slave in/master out |
| | PM_UCA2SOMI | 43 | I/O | Default mapping: eUSCI_A2 SPI slave out/master in |
| | PM_UCB0CLK | 37 | I/O | Default mapping: eUSCI_B0 clock input/output |
| | PM_UCB0SIMO | 39 | I/O | Default mapping: eUSCI_B0 SPI slave in/master out |
| | PM_UCB0SOMI | 38 | I/O | Default mapping: eUSCI_B0 SPI slave out/master in |
| System | NMI | 100 | I | Nonmaskable interrupt input |
| | RST | 100 | I | Reset input active low ⁽⁴⁾ |

- (1) The pins VDSYS and DVSYN must be connected externally on board for proper device operation.
- (2) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.
- (3) TI recommends shorting unused analog input pairs and connect them to analog ground.
- (4) When this pin is configured as reset, the internal pullup resistor is enabled by default.

Table 4-5. Signal Descriptions, PZ Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE | DESCRIPTION |
|----------|-------------|---------|-------------|--|
| Timer_A | PM_TA0.0 | 14 | I/O | Default mapping: Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output |
| | PM_TA0.1 | 15 | I/O | Default mapping: Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output |
| | PM_TA0.2 | 52 | I/O | Default mapping: Timer TA0 capture CCR2: CCI2A input, compare: Out2 output |
| | PM_TA1.0 | 47 | I/O | Default mapping: Timer TA1 capture CCR0: CCI0A input, compare: Out0 output |
| | PM_TA1.1 | 48 | I/O | Default mapping: Timer TA1 capture CCR1: CCI1A input, compare: Out1 output |
| | PM_TA2.0 | 49 | I/O | Default mapping: Timer TA2 capture CCR0: CCI0A input, compare: Out0 output |
| | PM_TA2.1 | 50 | I/O | Default mapping: Timer TA2 capture CCR1: CCI1A input, compare: Out1 output |
| | PM_TACLK | 51 | I | Default mapping: Timer clock input TACLK for TA0, TA1, TA2, TA3 |
| | TA1.0 | 30 | I/O | Timer TA1 CCR0 capture: CCI0A input, compare: Out0 output |
| | TA1.1 | 31 | I/O | Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output |
| | TA2.0 | 40 | I/O | Timer TA2 CCR0 capture: CCI0A input, compare: Out0 output |
| | TA2.1 | 41 | I/O | Timer TA2 CCR1 capture: CCI1A input, compare: Out1 output |
| | TACLK | 42 | I | Timer clock input TACLK for TA0, TA1, TA2, TA3 |
| UART | PM_UCA0RXD | 16 | I | Default mapping: eUSCI_A0 UART receive data |
| | PM_UCA0TXD | 17 | O | Default mapping: eUSCI_A0 UART transmit data |
| | PM_UCA1RXD | 27 | I | Default mapping: eUSCI_A1 UART receive data |
| | PM_UCA1TXD | 28 | O | Default mapping: eUSCI_A1 UART transmit data |
| | PM_UCA2RXD | 43 | I | Default mapping: eUSCI_A2 UART receive data |
| | PM_UCA2TXD | 44 | O | Default mapping: eUSCI_A2 UART transmit data |

Table 4-6 describes the signals for all device variants in the PN package. See Table 4-5 for signal descriptions in the PZ package.

Table 4-6. Signal Descriptions, PN Package

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE ⁽¹⁾ | DESCRIPTION |
|----------|-------------|---------|----------------------------|---|
| ADC10 | A0 | 13 | I | Analog input A0 for 10-bit ADC |
| | A1 | 12 | I | Analog input A1 for 10-bit ADC |
| | A2 | 11 | I | Analog input A2 for 10-bit ADC |
| | ADC10CLK | 78 | O | ADC10_A clock output |
| | VeREF+ | 12 | I | Positive terminal for the ADC reference voltage for an external applied reference voltage |
| | VeREF- | 11 | I | Negative terminal for the ADC reference voltage for an external applied reference voltage |
| BSL | BSL_RX | 42 | I | Bootloader data receive |
| | BSL_TX | 41 | O | Bootloader data transmit |
| Clock | ACLK | 79 | O | ACLK clock output |
| | MCLK | 77 | O | MCLK clock output |
| | PM_RTCCLK | 43 | O | Default mapping: RTCCLK clock output |
| | SMCLK | 76 | O | SMCLK clock output |
| | XIN | 21 | I | Input terminal for crystal oscillator |
| | XOUT | 22 | O | Output terminal for crystal oscillator |
| | Debug | SBWTCK | 75 | I |
| SBWTDIO | | 80 | I/O | Spy-Bi-Wire data input/output |
| TCK | | 79 | I | Test clock |
| TCLK | | 77 | I | Test clock input |
| TDI | | 77 | I | Test data input |
| TDO | | 76 | O | Test data output |
| TEST | | 75 | I | Test mode pin – select digital I/O on JTAG pins |
| TMS | | 78 | I | Test mode select |
| GPIO | P1.0 | 11 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.1 | 12 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.2 | 13 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.3 | 14 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.4 | 24 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.5 | 25 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.6 | 31 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P1.7 | 32 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.0 | 33 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.1 | 34 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.2 | 35 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.3 | 36 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |

(1) I = input, O = output

Table 4-6. Signal Descriptions, PN Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE ⁽¹⁾ | DESCRIPTION |
|------------------|-------------|---------|-----------------------------|---|
| GPIO | P2.4 | 37 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.5 | 38 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.6 | 39 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P2.7 | 40 | I/O | General-purpose digital I/O with port interrupt and mappable secondary function |
| | P3.0 | 41 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.1 | 42 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.2 | 43 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.3 | 44 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.4 | 45 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.5 | 46 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.6 | 47 | I/O | General-purpose digital I/O with mappable secondary function |
| | P3.7 | 48 | I/O | General-purpose digital I/O with mappable secondary function |
| | P4.0 | 49 | I/O | General-purpose digital I/O |
| | P4.1 | 50 | I/O | General-purpose digital I/O |
| | P4.2 | 51 | I/O | General-purpose digital I/O |
| | P4.3 | 52 | I/O | General-purpose digital I/O |
| | P4.4 | 53 | I/O | General-purpose digital I/O |
| | P4.5 | 54 | I/O | General-purpose digital I/O |
| | P4.6 | 55 | I/O | General-purpose digital I/O |
| | P4.7 | 56 | I/O | General-purpose digital I/O |
| | P5.0 | 57 | I/O | General-purpose digital I/O |
| | P5.1 | 58 | I/O | General-purpose digital I/O |
| | P5.2 | 61 | I/O | General-purpose digital I/O |
| | P5.3 | 62 | I/O | General-purpose digital I/O |
| | P5.4 | 63 | I/O | General-purpose digital I/O |
| | P5.5 | 64 | I/O | General-purpose digital I/O |
| | P5.6 | 65 | I/O | General-purpose digital I/O |
| | P5.7 | 66 | I/O | General-purpose digital I/O |
| | P6.0 | 67 | I/O | General-purpose digital I/O |
| | P6.1 | 68 | I/O | General-purpose digital I/O |
| | P6.2 | 69 | I/O | General-purpose digital I/O |
| | P6.3 | 70 | I/O | General-purpose digital I/O |
| | P6.4 | 71 | I/O | General-purpose digital I/O |
| P6.5 | 72 | I/O | General-purpose digital I/O | |
| P6.6 | 73 | I/O | General-purpose digital I/O | |
| P6.7 | 74 | I/O | General-purpose digital I/O | |
| PJ.0 | 76 | I/O | General-purpose digital I/O | |
| PJ.1 | 77 | I/O | General-purpose digital I/O | |
| PJ.2 | 78 | I/O | General-purpose digital I/O | |
| PJ.3 | 79 | I/O | General-purpose digital I/O | |
| I ² C | PM_UCB0SCL | 33 | I/O | Default mapping: eUSCI_B0 I ² C clock |
| | PM_UCB0SDA | 34 | I/O | Default mapping: eUSCI_B0 I ² C data |

Table 4-6. Signal Descriptions, PN Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE ⁽¹⁾ | DESCRIPTION |
|----------|-------------|---------|----------------------------|---|
| LCD | COM0 | 27 | O | LCD common output COM0 for LCD backplane |
| | COM1 | 28 | O | LCD common output COM1 for LCD backplane |
| | COM2 | 29 | O | LCD common output COM2 for LCD backplane |
| | COM3 | 30 | O | LCD common output COM3 for LCD backplane |
| | COM4 | 31 | O | LCD common output COM4 for LCD backplane |
| | COM5 | 32 | O | LCD common output COM5 for LCD backplane |
| | COM6 | 33 | O | LCD common output COM6 for LCD backplane |
| | COM7 | 34 | O | LCD common output COM7 for LCD backplane |
| | LDCAP | 26 | I/O | LCD capacitor connection CAUTION: This pin must be connected to DVSS if not used. |
| | LCDREF | 24 | I | External reference voltage input for regulated LCD voltage |
| | R03 | 14 | I/O | Input/output port of lowest analog LCD voltage (V5) |
| | R13 | 24 | I/O | Input/output port of third most positive analog LCD voltage (V3 or V4) |
| | R23 | 25 | I/O | Input/output port of second most positive analog LCD voltage (V2) |
| | R33 | 26 | I/O | Input/output port of most positive analog LCD voltage (V1) CAUTION: This pin must be connected to DVSS if not used. |
| | S0 | 74 | O | LCD segment output S0 |
| | S1 | 73 | O | LCD segment output S1 |
| | S2 | 72 | O | LCD segment output S2 |
| | S3 | 71 | O | LCD segment output S3 |
| | S4 | 70 | O | LCD segment output S4 |
| | S5 | 69 | O | LCD segment output S5 |
| | S6 | 68 | O | LCD segment output S6 |
| | S7 | 67 | O | LCD segment output S7 |
| | S8 | 66 | O | LCD segment output S8 |
| | S9 | 65 | O | LCD segment output S9 |
| | S10 | 64 | O | LCD segment output S10 |
| | S11 | 63 | O | LCD segment output S11 |
| | S12 | 62 | O | LCD segment output S12 |
| | S13 | 61 | O | LCD segment output S13 |
| | S14 | 58 | O | LCD segment output S14 |
| | S15 | 57 | O | LCD segment output S15 |
| | S16 | 56 | O | LCD segment output S16 |
| | S17 | 55 | O | LCD segment output S17 |
| | S18 | 54 | O | LCD segment output S18 |
| | S19 | 53 | O | LCD segment output S19 |
| | S20 | 52 | O | LCD segment output S20 |
| | S21 | 51 | O | LCD segment output S21 |
| S22 | 50 | O | LCD segment output S22 | |
| S23 | 49 | O | LCD segment output S23 | |
| S24 | 48 | O | LCD segment output S24 | |
| S25 | 47 | O | LCD segment output S25 | |
| S26 | 46 | O | LCD segment output S26 | |

Table 4-6. Signal Descriptions, PN Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE ⁽¹⁾ | DESCRIPTION |
|----------------------|----------------------|---------|--|---|
| LCD | S27 | 45 | O | LCD segment output S27 |
| | S28 | 44 | O | LCD segment output S28 |
| | S29 | 43 | O | LCD segment output S29 |
| | S30 | 42 | O | LCD segment output S30 |
| | S31 | 41 | O | LCD segment output S31 |
| | S32 | 40 | O | LCD segment output S32 |
| | S33 | 39 | O | LCD segment output S33 |
| | S34 | 38 | O | LCD segment output S34 |
| | S35 | 37 | O | LCD segment output S35 |
| | S36 | 36 | O | LCD segment output S36 |
| | S37 | 35 | O | LCD segment output S37 |
| | S38 | 34 | O | LCD segment output S38 |
| | S39 | 33 | O | LCD segment output S39 |
| Power | AUXVCC1 | 16 | P | Auxiliary power supply AUXVCC1 |
| | AUXVCC2 | 15 | P | Auxiliary power supply AUXVCC2 |
| | AUXVCC3 | 23 | P | Auxiliary power supply AUXVCC3 for backup subsystem |
| | AVCC | 9 | P | Analog power supply |
| | AVSS | 8 | P | Analog ground supply |
| | DVCC | 18 | P | Digital power supply |
| | DVSS | 19 | P | Digital ground supply |
| | DVSS | 60 | P | Digital ground supply |
| | DVSY ⁽²⁾ | 59 | P | Digital power supply for I/Os |
| | VASYS | 10 | P | Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C _{VSY} (see Table 5-18). |
| | VCORE ⁽³⁾ | 20 | P | Regulated core power supply (internal use only, no external current loading) |
| VDSYS ⁽²⁾ | 17 | P | Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C _{VSY} (see Table 5-18). | |
| SD24 | PM_SD0DIO | 46 | I/O | Default mapping: SD24_B converter 0 bit stream data input/output |
| | PM_SD1DIO | 47 | I/O | Default mapping: SD24_B converter 1 bit stream data input/output |
| | PM_SD2DIO | 48 | I/O | Default mapping: SD24_B converter 2 bit stream data input/output (not available on F672xA devices) |
| | PM_SDCLK | 45 | I/O | Default mapping: SD24_B bit stream clock input/output |
| | SD0N0 | 2 | I | SD24_B negative analog input for converter 0 ⁽⁴⁾ |
| | SD0P0 | 1 | I | SD24_B positive analog input for converter 0 ⁽⁴⁾ |
| | SD1N0 | 4 | I | SD24_B negative analog input for converter 1 ⁽⁴⁾ |
| | SD1P0 | 3 | I | SD24_B positive analog input for converter 1 ⁽⁴⁾ |
| | SD2N0 | 6 | I | SD24_B negative analog input for converter 2 ⁽⁴⁾ (not available on F672xA devices) |
| | SD2P0 | 5 | I | SD24_B positive analog input for converter 2 ⁽⁴⁾ (not available on F672xA devices) |
| | VREF | 7 | I | SD24_B external reference voltage |

(2) The pins VDSYS and DVSY must be connected externally on board for proper device operation.

(3) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

(4) TI recommends shorting unused analog input pairs and connect them to analog ground.

Table 4-6. Signal Descriptions, PN Package (continued)

| FUNCTION | SIGNAL NAME | PIN NO. | SIGNAL TYPE ⁽¹⁾ | DESCRIPTION |
|----------|-------------|---------|----------------------------|--|
| SPI | PM_UCA0CLK | 31 | I/O | Default mapping: eUSCI_A0 clock input/output |
| | PM_UCA0SIMO | 14 | I/O | Default mapping: eUSCI_A0 SPI slave in/master out |
| | PM_UCA0SOMI | 13 | I/O | Default mapping: eUSCI_A0 SPI slave out/master in |
| | PM_UCA1CLK | 37 | I/O | Default mapping: eUSCI_A1 clock input/output |
| | PM_UCA1SIMO | 25 | I/O | Default mapping: eUSCI_A1 SPI slave in/master out |
| | PM_UCA1SOMI | 24 | I/O | Default mapping: eUSCI_A1 SPI slave out/master in |
| | PM_UCA2CLK | 38 | I/O | Default mapping: eUSCI_A2 clock input/output |
| | PM_UCA2SIMO | 36 | I/O | Default mapping: eUSCI_A2 SPI slave in/master out |
| | PM_UCA2SOMI | 35 | I/O | Default mapping: eUSCI_A2 SPI slave out/master in |
| | PM_UCB0CLK | 32 | I/O | Default mapping: eUSCI_B0 clock input/output |
| | PM_UCB0SIMO | 34 | I/O | Default mapping: eUSCI_B0 SPI slave in/master out |
| | PM_UCB0SOMI | 33 | I/O | Default mapping: eUSCI_B0 SPI slave out/master in |
| System | NMI | 80 | I | Nonmaskable interrupt input |
| | RST | 80 | I/O | Reset input active low ⁽⁵⁾ |
| Timer_A | PM_TA0.0 | 11 | I/O | Default mapping: Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output |
| | PM_TA0.1 | 12 | I/O | Default mapping: Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output |
| | PM_TA0.2 | 44 | I/O | Default mapping: Timer TA0 capture CCR2: CCI2A input, compare: Out2 output |
| | PM_TA1.0 | 39 | I/O | Default mapping: Timer TA1 capture CCR0: CCI0A input, compare: Out0 output |
| | PM_TA1.1 | 40 | I/O | Default mapping: Timer TA1 capture CCR1: CCI1A input, compare: Out1 output |
| | PM_TA2.0 | 41 | I/O | Default mapping: Timer TA2 capture CCR0: CCI0A input, compare: Out0 output |
| | PM_TA2.1 | 42 | I/O | Default mapping: Timer TA2 capture CCR1: CCI1A input, compare: Out1 output |
| | PM_TACLK | 43 | I | Default mapping: Timer clock input TACLK for TA0, TA1, TA2, TA3 |
| UART | PM_UCA0RXD | 13 | I | Default mapping: eUSCI_A0 UART receive data |
| | PM_UCA0TXD | 14 | O | Default mapping: eUSCI_A0 UART transmit data |
| | PM_UCA1RXD | 24 | I | Default mapping: eUSCI_A1 UART receive data |
| | PM_UCA1TXD | 25 | O | Default mapping: eUSCI_A1 UART transmit data |
| | PM_UCA2RXD | 35 | I | Default mapping: eUSCI_A2 UART receive data |
| | PM_UCA2TXD | 36 | O | Default mapping: eUSCI_A2 UART transmit data |

(5) When this pin is configured as reset, the internal pullup resistor is enabled by default.

4.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [§ 6.12](#).

4.5 Buffer Type

[Table 4-7](#) describes the buffer types that are referenced in [Table 4-3](#) and [Table 4-4](#).

Table 4-7. Buffer Type

| BUFFER TYPE (STANDARD) | NOMINAL VOLTAGE | HYSTERESIS | PU OR PD | NOMINAL PU OR PD STRENGTH (μ A) | OUTPUT DRIVE STRENGTH (mA) | OTHER CHARACTERISTICS |
|------------------------|-----------------|---------------|--------------|---|---|--|
| LVC MOS | 3.0 V | Y | Programmable | See § 5.8.4 Digital I/O Ports | See § 5.8.4 Digital I/O Ports | |
| Analog | 3.0 V | N | N/A | N/A | N/A | See analog modules in Section 5, Specifications , for details. |
| Power | 3.0 V | Y with SVS on | N/A | N/A | N/A | |

4.6 Connection of Unused Pins

[Table 4-8](#) lists the correct termination of unused pins.

Table 4-8. Connection of Unused Pins⁽¹⁾

| PIN | POTENTIAL | COMMENT |
|--|-------------------------------------|---|
| AVCC | DV _{CC} | |
| AVSS | DV _{SS} | |
| Px.y | Open | Switched to port function, output direction (PxDIR.n = 1). Px.y represents port x and bit y of port x (for example, P1.0, P1.1, P2.2, PJ.0, PJ.1) |
| XIN | DV _{SS} | For dedicated XIN pins only. XIN pins with shared GPIO functions should be programmed to GPIO and follow Px.y recommendations. |
| XOUT | Open | For dedicated XOUT pins only. XOUT pins with shared GPIO functions should be programmed to GPIO and follow Px.y recommendations. |
| LDCAP | DV _{SS} | |
| RST/NMI | DV _{CC} or V _{CC} | 47-k Ω pullup or internal pullup selected with 10-nF (2.2-nF) pulldown ⁽²⁾ |
| PJ.0/TDO PJ.1/TDI PJ.2/TMS PJ.3/TCK | Open | The JTAG pins are shared with general-purpose I/O function (PJ.x). If not being used, these should be switched to port function, output direction (PJDIR.n = 1). When used as JTAG pins, these pins should remain open. |
| TEST | Open | This pin always has an internal pulldown enabled. |

- (1) Any unused pin with a secondary function that is shared with a general-purpose I/O must follow the Px.y unused pin connection guidelines.
- (2) The pulldown capacitor should not exceed 2.2 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools such as FET interfaces or GANG programmers.

5 Specifications

All graphs in this section are for typical conditions, unless otherwise noted.

Typical (TYP) values are specified at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$, unless otherwise noted.

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|---|---------|----------------|------|
| Voltage applied at DVCC to DVSS | | -0.3 | 4.1 | V |
| Voltage applied to pins ⁽²⁾ | All pins except V _{CORE} ⁽³⁾ , SD24_B input pins (SDxN0, SDxP0) ⁽⁴⁾ , AUXVCC1, AUXVCC2, and AUXVCC3 ⁽⁵⁾ | -0.3 | $V_{CC} + 0.3$ | V |
| Diode current at pins | All pins except SD24_B input pins (SDxN0, SDxP0) | ± 2 | | mA |
| | SD0N0, SD0P0, SD1N0, SD1P0, SD2N0, SD2P0 ⁽⁶⁾ | 2 | | |
| Maximum junction temperature, T _J | | 95 | | °C |
| Storage temperature, T _{stg} ⁽⁷⁾ | | -55 | 105 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to $V_{SS} = V_{DVSS} = V_{AVSS}$.
- (3) V_{CORE} is for internal device use only. No external DC loading or voltage should be applied.
- (4) See [Table 5-35](#) for SD24_B specifications.
- (5) See [Table 5-18](#) for AUX specifications.
- (6) A protection diode is connected to V_{CC} for the SD24_B input pins. No protection diode is connected to V_{SS} .
- (7) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|------------|------|
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ± 1000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ± 250 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as $\pm 1000\text{ V}$ may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as $\pm 250\text{ V}$ may actually have higher performance.

5.3 Recommended Operating Conditions

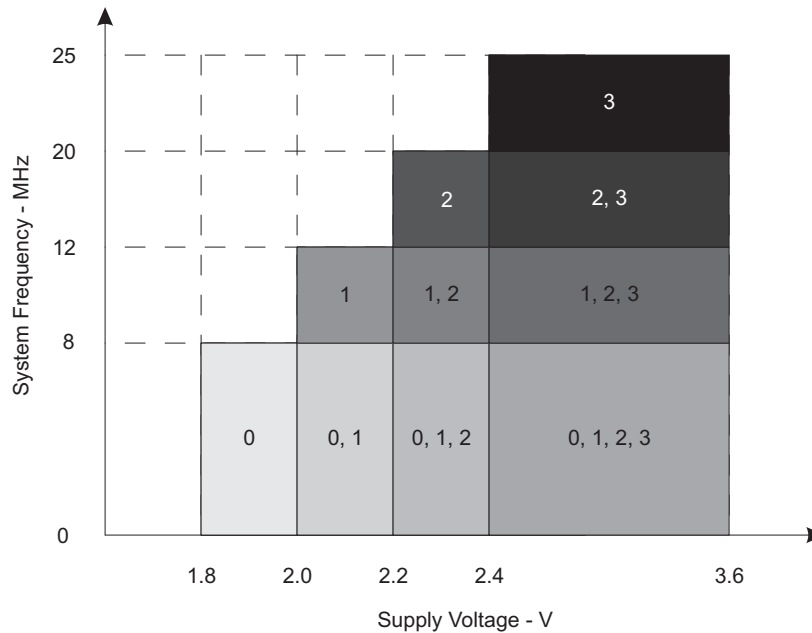
| | | MIN | NOM | MAX | UNIT | |
|--|--|------------------------|-----|-----|------|----|
| V _{CC} | Supply voltage during program execution and flash programming. $V_{(AVCC)} = V_{(DVCC)} = V_{CC}$ ^{(1) (2)} | PMMCOREVx = 0 | 1.8 | 3.6 | V | |
| | | PMMCOREVx = 0, 1 | 2.0 | 3.6 | | |
| | | PMMCOREVx = 0, 1, 2 | 2.2 | 3.6 | | |
| | | PMMCOREVx = 0, 1, 2, 3 | 2.4 | 3.6 | | |
| V _{SS} | Supply voltage $V_{(AVSS)} = V_{(DVSS)} = V_{SS}$ | 0 | | V | | |
| T _A | Operating free-air temperature | I version | | -40 | 85 | °C |
| T _J | Operating junction temperature | I version | | -40 | 85 | °C |
| C _{VCORE} | Recommended capacitor at V _{CORE} ⁽³⁾ | | | 470 | nF | |
| C _{DVCC} / C _{VCORE} | Capacitor ratio of DVCC to V _{CORE} | | | 10 | | |

- (1) TI recommends powering AVCC and DVCC from the same source. A maximum difference of 0.3 V between V(AVCC) and V(DVCC) can be tolerated during power up and operation.
- (2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the [Table 5-14](#) threshold parameters for the exact values and further details.
- (3) A capacitor tolerance of $\pm 20\%$ or better is required.

Recommended Operating Conditions (continued)

| | | MIN | NOM | MAX | UNIT | |
|--------------------------|---|--|-----|-----|------|-----|
| f _{SYSTEM} | Processor frequency (maximum MCLK frequency) ⁽⁴⁾ ⁽⁵⁾ (see Figure 5-1) | PMMCOREVx = 0, 1.8 V ≤ V _{CC} ≤ 3.6 V (default condition) | | 0 | 8.0 | MHz |
| | | PMMCOREVx = 1, 2.0 V ≤ V _{CC} ≤ 3.6 V | | 0 | 12.0 | |
| | | PMMCOREVx = 2, 2.2 V ≤ V _{CC} ≤ 3.6 V | | 0 | 20.0 | |
| | | PMMCOREVx = 3, 2.4 V ≤ V _{CC} ≤ 3.6 V | | 0 | 25.0 | |
| I _{LOAD, DVCCD} | Maximum load current that can be drawn from DVCC for core and IO (I _{LOAD} = I _{CORE} + I _{IO}) | | | 20 | mA | |
| I _{LOAD, AUX1D} | Maximum load current that can be drawn from AUXVCC1 for core and IO (I _{LOAD} = I _{CORE} + I _{IO}) | | | 20 | mA | |
| I _{LOAD, AUX2D} | Maximum load current that can be drawn from AUXVCC2 for core and IO (I _{LOAD} = I _{CORE} + I _{IO}) | | | 20 | mA | |
| I _{LOAD, AVCCA} | Maximum load current that can be drawn from AVCC for analog modules (I _{LOAD} = I _{Modules}) | | | 10 | mA | |
| I _{LOAD, AUX1A} | Maximum load current that can be drawn from AUXVCC1 for analog modules (I _{LOAD} = I _{Modules}) | | | 5 | mA | |
| I _{LOAD, AUX2A} | Maximum load current that can be drawn from AUXVCC2 for analog modules (I _{LOAD} = I _{Modules}) | | | 5 | mA | |

- (4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
- (5) Modules may have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 5-1. Maximum System Frequency

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)⁽¹⁾ ⁽²⁾ ⁽³⁾

| PARAMETER | EXECUTION MEMORY | V_{CC} | PMMCOREVx | FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$) | | | | | | | | UNIT | | |
|-----------------------|------------------|----------|-----------|--|------|-------|------|--------|------|--------|------|------|--------|-----|
| | | | | 1 MHz | | 8 MHz | | 12 MHz | | 20 MHz | | | 25 MHz | |
| | | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | | TYP | MAX |
| $I_{AM, Flash}^{(4)}$ | Flash | 3.0 V | 0 | 0.32 | 0.36 | 2.10 | 2.30 | | | | | | | mA |
| | | | 1 | 0.36 | | 2.39 | | 3.54 | 3.90 | | | | | |
| | | | 2 | 0.39 | | 2.65 | | 3.94 | | 6.54 | 7.23 | | | |
| | | | 3 | 0.42 | | 2.82 | | 4.20 | | 6.96 | | 8.65 | 9.54 | |
| $I_{AM, RAM}^{(5)}$ | RAM | 3.0 V | 0 | 0.20 | 0.22 | 1.10 | 1.22 | | | | | | | mA |
| | | | 1 | 0.22 | | 1.30 | | 1.90 | 2.10 | | | | | |
| | | | 2 | 0.24 | | 1.45 | | 2.15 | | 3.55 | 4.0 | | | |
| | | | 3 | 0.26 | | 1.55 | | 2.30 | | 3.80 | | 4.70 | 5.30 | |

- (1) All inputs are tied to 0 or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Characterized with program executing typical data processing.
 $f_{ACLK} = 32786$ Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
 $XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0$.
- (4) Active mode supply current when program executes in flash at a nominal supply voltage of 3 V.
- (5) Active mode supply current when program executes in RAM at a nominal supply voltage of 3 V.

5.5 Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V_{CC} | PMMCOREVx | TEMPERATURE (T_A) | | | | | | | | UNIT |
|---|----------|-----------|-----------------------|-----|------|------|------|-----|------|------|---------|
| | | | -40°C | | 25°C | | 60°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0,1MHz}$ Low-power mode 0 ^{(3) (4)} | 2.2 V | 0 | 75 | | 78 | 87 | 81 | | 84 | 96 | μA |
| | 3.0 V | 3 | 85 | | 89 | 99 | 93 | | 98 | 110 | |
| I_{LPM2} Low-power mode 2 ^{(5) (4)} | 2.2 V | 0 | 5.9 | | 6.2 | 9 | 6.9 | | 9.4 | 17 | μA |
| | 3.0 V | 3 | 6.9 | | 7.4 | 10 | 8.4 | | 11 | 19 | |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ^{(6) (4)} | 2.2 V | 0 | 1.4 | | 1.7 | | 2.5 | | 4.9 | | μA |
| | | 1 | 1.5 | | 1.9 | | 2.7 | | 5.2 | | |
| | | 2 | 1.7 | | 2.0 | | 2.9 | | 5.5 | | |
| $I_{LPM3,XT1LF}$ Low-power mode 3, crystal mode ^{(6) (4)} | 3.0 V | 0 | 2.2 | | 2.5 | 3.1 | 3.3 | | 5.5 | 12.7 | μA |
| | | 1 | 2.3 | | 2.7 | | 3.5 | | 6.1 | | |
| | | 2 | 2.5 | | 2.9 | | 3.7 | | 6.1 | 14.0 | |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO mode ^{(7) (4)} | 3.0 V | 0 | 1.4 | | 1.7 | 2.2 | 2.4 | | 4.5 | 11.5 | μA |
| | | 1 | 1.5 | | 1.8 | | 2.5 | | 4.7 | | |
| | | 2 | 1.6 | | 1.9 | | 2.7 | | 4.9 | | |
| I_{LPM4} Low-power mode 4 ^{(8) (4)} | 3.0 V | 0 | 1.3 | | 1.6 | 2.0 | 2.3 | | 4.4 | 11.1 | μA |
| | | 1 | 1.4 | | 1.6 | | 2.4 | | 4.5 | | |
| | | 2 | 1.4 | | 1.7 | | 2.5 | | 4.8 | | |
| $I_{LPM4.5}$ Low-power mode 4.5 ⁽¹⁰⁾ | 3.0 V | 0 | 1.4 | | 1.7 | 2.2 | 2.5 | | 4.8 | 12.2 | μA |
| | | 1 | 1.4 | | 1.7 | | 2.5 | | 4.8 | | |
| | | 2 | 1.4 | | 1.7 | | 2.5 | | 4.8 | | |
| $I_{LPM3.5}$ Low-power mode 3.5, RTC active on AUXVCC3 ⁽⁹⁾ | 2.2 V | | 0.65 | | 0.80 | | 0.90 | | 1.30 | | μA |
| | 3.0 V | | 1.16 | | 1.24 | 2.05 | 1.43 | | 1.87 | 2.71 | |
| $I_{LPM4.5}$ Low-power mode 4.5 ⁽¹⁰⁾ | 3.0 V | | 0.70 | | 0.78 | 1.05 | 0.90 | | 1.20 | 1.85 | μA |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Current for watchdog timer clocked by SMCLK included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
- (4) Current for brownout, high-side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM_L) disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.
- (5) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2), f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz, DCO setting = 1-MHz operation, DCO bias generator enabled.
- (6) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0). CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
- (7) Current for watchdog timer clocked by ACLK included. RTC is disabled (RTCHOLD=1). ACLK = VLO. CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = f_{VLO} , f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
- (8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4), f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
- (9) f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC active on AUXVCC3 supply
- (10) f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, PMMREGOFF = 1

5.6 Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)^{(1) (2)}

| PARAMETER | V_{CC} | PMMCOREVx | TEMPERATURE (T_A) | | | | | | | | UNIT |
|---------------------------------|----------|-----------|-----------------------|-----|------|-----|------|------|---------|-----|------|
| | | | -40°C | | 25°C | | 60°C | | 85°C | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| I_{LPM3} LCD, int. bias | 2.2 V | 0 | 2.4 | 2.9 | 3.6 | 3.8 | 5.8 | 12.2 | μ A | | |
| | | 1 | 2.5 | 3.1 | 4.0 | 6.0 | | | | | |
| | | 2 | 2.6 | 3.3 | 3.9 | 4.2 | 6.3 | 13.4 | | | |
| I_{LPM3} LCD, int. bias | 3.0 V | 0 | 2.8 | 3.2 | 3.9 | 4.1 | 6.4 | 13.3 | μ A | | |
| | | 1 | 2.9 | 3.4 | 4.3 | 6.7 | | | | | |
| | | 2 | 3.1 | 3.6 | 4.5 | 7.0 | | | | | |
| | | 3 | 3.1 | 3.6 | 4.5 | 4.5 | 7.0 | 14.7 | | | |
| I_{LPM3} LCD,CP | 2.2 V | 0 | | 3.8 | | | | | μ A | | |
| | | 1 | | 3.9 | | | | | | | |
| | | 2 | | 4.0 | | | | | | | |
| | 3.0 V | 0 | | 4.0 | | | | | | | |
| | | 1 | | 4.1 | | | | | | | |
| | | 2 | | 4.2 | | | | | | | |
| | | 3 | | 4.2 | | | | | | | |

- (1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.
- (2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
- (3) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3), f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
Current for brownout and high-side supervisor (SVSH) normal mode included. Low-side supervisor (SVSL) and low-side monitor (SVM_L) disabled. High-side monitor (SVM_H) disabled. RAM retention enabled.
- (4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ... = 0 and odd segments S1, S3, ... = 1. No LCD panel load.
- (5) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 (V_{LCD} = 3 V, typical), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ... = 0 and odd segments S1, S3, ... = 1. No LCD panel load.

5.7 Thermal Resistance Characteristics

| THERMAL METRIC ^{(1) (2)} | | | VALUE | UNIT |
|-----------------------------------|--|---------------|--------------------|------|
| R _{θJA} | Junction-to-ambient thermal resistance, still air | LQFP 80 (PN) | 46.3 | °C/W |
| | | LQFP 100 (PZ) | 45.6 | |
| R _{θJC(TOP)} | Junction-to-case (top) thermal resistance | LQFP 80 (PN) | 11.5 | °C/W |
| | | LQFP 100 (PZ) | 11.0 | |
| R _{θJC(BOTTOM)} | Junction-to-case (bottom) thermal resistance | LQFP 80 (PN) | N/A ⁽³⁾ | °C/W |
| | | LQFP 100 (PZ) | N/A | |
| R _{θJB} | Junction-to-board thermal resistance | LQFP 80 (PN) | 21.9 | °C/W |
| | | LQFP 100 (PZ) | 23.4 | |
| Ψ _{JT} | Junction-to-package-top thermal characterization parameter | LQFP 80 (PN) | 0.5 | °C/W |
| | | LQFP 100 (PZ) | 0.4 | |
| Ψ _{JB} | Junction-to-board thermal characterization parameter | LQFP 80 (PN) | 21.6 | °C/W |
| | | LQFP 100 (PZ) | 23.0 | |

(1) For more information about traditional and new thermal metrics, see [Semiconductor and IC Package Thermal Metrics](#).

(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R_{θJC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = not applicable

5.8 Timing and Switching Characteristics

5.8.1 Power Supply Sequencing

TI recommends powering AVCC and DVCC pins from the same source. At a minimum, during power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in [Absolute Maximum Ratings](#). Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and flash.

5.8.2 Reset Timing

Table 5-1 lists the device wake-up times.

Table 5-1. Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------|--|---|---|-----|-----|---------------|
| $t_{\text{WAKE-UP-FAST}}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽¹⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1 | $f_{\text{MCLK}} \geq 4 \text{ MHz}$ | 3 | 5 | μs |
| | | | $1 \text{ MHz} < f_{\text{MCLK}} < 4 \text{ MHz}$ | 4 | 6 | |
| $t_{\text{WAKE-UP-SLOW}}$ | Wake-up time from LPM2, LPM3, or LPM4 to active mode ⁽²⁾⁽³⁾ | PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0 | | 150 | 160 | μs |
| $t_{\text{WAKE-UP-LPM4.5}}$ | Wake-up time from LPM4.5 to active mode ⁽⁴⁾ | | | 2 | 3 | ms |
| $t_{\text{WAKE-UP-RESET}}$ | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode ⁽⁴⁾ | | | 2 | 3 | ms |

- (1) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVSL) and low-side monitor (SVM_L). $t_{\text{WAKE-UP-FAST}}$ is possible with SVSL and SVM_L in full performance mode or disabled. For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430x5xx and MSP430x6xx Family User's Guide](#).
- (2) This value represents the time from the wake-up event to the first active edge of MCLK. The wake-up time depends on the performance mode of the low-side supervisor (SVSL) and low-side monitor (SVM_L). $t_{\text{WAKE-UP-SLOW}}$ is set with SVSL and SVM_L in normal mode (low current mode). For specific register settings, see the *Low-Side SVS and SVM Control and Performance Mode Selection* section in the *Power Management Module and Supply Voltage Supervisor* chapter of the [MSP430x5xx and MSP430x6xx Family User's Guide](#).
- (3) The wake-up times from LPM0 and LPM1 to AM are not specified. They are proportional to MCLK cycle time but are not affected by the performance mode settings as for LPM2, LPM3, and LPM4.
- (4) This value represents the time from the wake-up event to the reset vector execution.

5.8.3 Clock Specifications

Table 5-2 lists the characteristics of the crystal oscillator in low-frequency mode.

Table 5-2. Crystal Oscillator, XT1, Low-Frequency Mode⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|----------------------|--|-----------------|-----|--------|-----|------------|---|
| $\Delta I_{DVCC,LF}$ | Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode | 3.0 V | | 0.075 | | μA | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, T _A = 25°C | | | | | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 2, T _A = 25°C | | | | | | |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C | | | 0.290 | | | |
| $f_{XT1,LF0}$ | XT1 oscillator crystal frequency, LF mode | | | 32768 | | Hz | |
| $f_{XT1,LF,SW}$ | XT1 oscillator logic-level square-wave input frequency, LF mode | | 10 | 32.768 | 50 | kHz | |
| OA_{LF} | Oscillation allowance for LF crystals ⁽⁴⁾ | | | 210 | | k Ω | |
| | | | | | | | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 6 pF |
| | XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 1, $f_{XT1,LF} = 32768$ Hz, C _{L,eff} = 12 pF | | | 300 | | | |
| $C_{L,eff}$ | Integrated effective load capacitance, LF mode ⁽⁵⁾ | | | | | pF | |
| | | | | | | | XTS = 0, XCAP _x = 0 ⁽⁶⁾ |
| | | | | | | | XTS = 0, XCAP _x = 1 |
| | | | | | | | XTS = 0, XCAP _x = 2 |
| | XTS = 0, XCAP _x = 3 | | | 12.0 | | | |
| | Duty cycle, LF mode | | | | 30% | 70% | |
| $f_{Fault,LF}$ | Oscillator fault frequency, LF mode ⁽⁷⁾ | | | | 10 | 10000 | |
| $t_{START,LF}$ | Start-up time, LF mode | 3.0 V | | | | ms | |
| | | | | | | | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 0, T _A = 25°C, C _{L,eff} = 6 pF |
| | $f_{OSC} = 32768$ Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVE _x = 3, T _A = 25°C, C _{L,eff} = 12 pF | | | 500 | | | |

- (1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-Trigger Inputs section of this data sheet.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVE_x settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For XT1DRIVE_x = 0, C_{L,eff} ≤ 6 pF
 - For XT1DRIVE_x = 1, 6 pF ≤ C_{L,eff} ≤ 9 pF
 - For XT1DRIVE_x = 2, 6 pF ≤ C_{L,eff} ≤ 10 pF
 - For XT1DRIVE_x = 3, C_{L,eff} ≥ 6 pF
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin). Because the PCB adds additional capacitance, TI recommends verifying the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
- (8) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-3 lists the characteristics of the VLO.

Table 5-3. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at ACLK | 1.8 V to 3.6 V | 6 | 9.4 | 15 | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 4 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 30% | | 70% | |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-4 lists the characteristics of the REFO.

Table 5-4. Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|---------------------------------|-----------------|-----|-------|-------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | 1.8 V to 3.6 V | | 3 | | μA |
| f _{REFO} | REFO frequency calibrated | Measured at ACLK | 1.8 V to 3.6 V | | 32768 | | Hz |
| | REFO absolute tolerance calibrated | Full temperature range | 1.8 V to 3.6 V | | | ±3.5% | |
| | | T _A = 25°C | 3 V | | | ±1.5% | |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at ACLK ⁽¹⁾ | 1.8 V to 3.6 V | | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at ACLK ⁽²⁾ | 1.8 V to 3.6 V | | 1.0 | | %/V |
| | Duty cycle | Measured at ACLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| t _{START} | REFO start-up time | 40%/60% duty cycle | 1.8 V to 3.6 V | | 25 | | μs |

(1) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(85°C – (−40°C))

(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

Table 5-5 lists the DCO frequencies.

Table 5-5. DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-2)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|----------------------|--|--|-----|------|------|-------|
| $f_{DCO(0,0)}$ | DCO frequency (0, 0) ⁽¹⁾ | 0.07 | | 0.20 | MHz | |
| $f_{DCO(0,31)}$ | DCO frequency (0, 31) ⁽¹⁾ | 0.70 | | 1.70 | MHz | |
| $f_{DCO(1,0)}$ | DCO frequency (1, 0) ⁽¹⁾ | 0.15 | | 0.36 | MHz | |
| $f_{DCO(1,31)}$ | DCO frequency (1, 31) ⁽¹⁾ | 1.47 | | 3.45 | MHz | |
| $f_{DCO(2,0)}$ | DCO frequency (2, 0) ⁽¹⁾ | 0.32 | | 0.75 | MHz | |
| $f_{DCO(2,31)}$ | DCO frequency (2, 31) ⁽¹⁾ | 3.17 | | 7.38 | MHz | |
| $f_{DCO(3,0)}$ | DCO frequency (3, 0) ⁽¹⁾ | 0.64 | | 1.51 | MHz | |
| $f_{DCO(3,31)}$ | DCO frequency (3, 31) ⁽¹⁾ | 6.07 | | 14.0 | MHz | |
| $f_{DCO(4,0)}$ | DCO frequency (4, 0) ⁽¹⁾ | 1.3 | | 3.2 | MHz | |
| $f_{DCO(4,31)}$ | DCO frequency (4, 31) ⁽¹⁾ | 12.3 | | 28.2 | MHz | |
| $f_{DCO(5,0)}$ | DCO frequency (5, 0) ⁽¹⁾ | 2.5 | | 6.0 | MHz | |
| $f_{DCO(5,31)}$ | DCO frequency (5, 31) ⁽¹⁾ | 23.7 | | 54.1 | MHz | |
| $f_{DCO(6,0)}$ | DCO frequency (6, 0) ⁽¹⁾ | 4.6 | | 10.7 | MHz | |
| $f_{DCO(6,31)}$ | DCO frequency (6, 31) ⁽¹⁾ | 39.0 | | 88.0 | MHz | |
| $f_{DCO(7,0)}$ | DCO frequency (7, 0) ⁽¹⁾ | 8.5 | | 19.6 | MHz | |
| $f_{DCO(7,31)}$ | DCO frequency (7, 31) ⁽¹⁾ | 60 | | 135 | MHz | |
| $S_{DCORSEL}$ | Frequency step between range DCORSEL and DCORSEL + 1 | $S_{RSEL} = f_{DCO(DCORSEL+1,DCO)} / f_{DCO(DCORSEL,DCO)}$ | | 1.2 | 2.3 | ratio |
| S_{DCO} | Frequency step between tap DCO and DCO + 1 | $S_{DCO} = f_{DCO(DCORSEL,DCO+1)} / f_{DCO(DCORSEL,DCO)}$ | | 1.02 | 1.12 | ratio |
| | Duty cycle | Measured at SMCLK | | 40% | 50% | 60% |
| df_{DCO}/dT | DCO frequency temperature drift | $f_{DCO} = 1 \text{ MHz}$ | | 0.1 | | %/°C |
| df_{DCO}/dV_{CORE} | DCO frequency voltage drift | $f_{DCO} = 1 \text{ MHz}$ | | 1.9 | | %/V |

- (1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO} , should be set to reside within the range of $f_{DCO(n,0),MAX} \leq f_{DCO} \leq f_{DCO(n,31),MIN}$, where $f_{DCO(n,0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

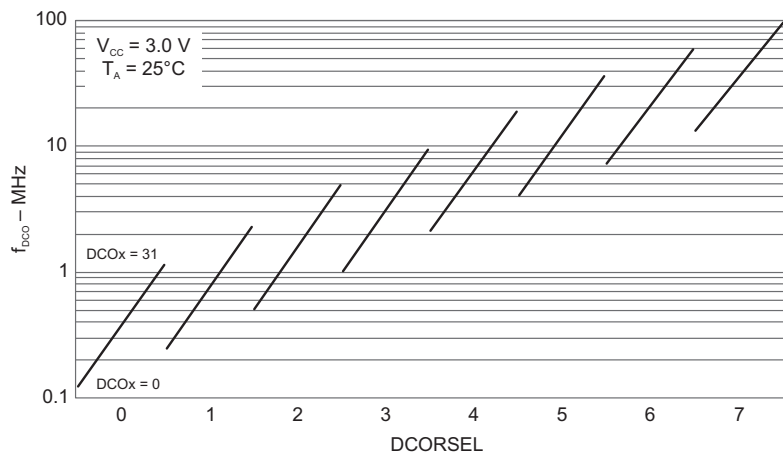


Figure 5-2. Typical DCO Frequency

5.8.4 Digital I/O Ports

Table 5-6 lists the characteristics of the GPIOs.

Table 5-6. Schmitt-Trigger Inputs, General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | | 1.8 V | 0.80 | | 1.40 | V |
| | | | 3 V | 1.50 | | 2.10 | |
| V _{IT-} | Negative-going input threshold voltage | | 1.8 V | 0.45 | | 1.00 | V |
| | | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | | 1.8 V | 0.3 | | 0.85 | V |
| | | | 3 V | 0.4 | | 1.0 | |
| R _{Pull} | Pullup or pulldown resistor ⁽¹⁾ | For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _I | Input capacitance | V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |

(1) Also applies to $\overline{\text{RST}}$ pin when pullup or pulldown resistor is enabled.

Table 5-7 lists the characteristics of the P1 and P2 inputs.

Table 5-7. Inputs, Ports P1 and P2⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--------------------|--|--|-----------------|-----|-----|------|
| t _(int) | External interrupt timing ⁽²⁾ | Port P1, P2: P1.x to P2.x, External trigger pulse duration to set interrupt flag | 2.2 V, 3 V | 20 | | ns |

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.

(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration t_(int) is met. It might be set by trigger signals shorter than t_(int).

Table 5-8 lists the leakage currents of the GPIOs.

Table 5-8. Leakage Current, General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|------------------------|--------------------------------|-----------------------------------|-----------------|-----|-----|------|
| I _{lkg(Px.y)} | High-impedance leakage current | See ⁽¹⁾ ⁽²⁾ | 1.8 V, 3 V | | ±50 | nA |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Table 5-9 lists the output characteristics of the GPIOs in full drive strength mode. Also see Figure 5-3 through Figure 5-6.

Table 5-9. Outputs, General-Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|--|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -3 mA ⁽¹⁾ | 1.8 V | V _{CC} - 0.25 | V _{CC} | V |
| | | I _(OHmax) = -10 mA ⁽¹⁾ | | V _{CC} - 0.60 | V _{CC} | |
| | | I _(OHmax) = -5 mA ⁽¹⁾ | 3 V | V _{CC} - 0.25 | V _{CC} | |
| | | I _(OHmax) = -15 mA ⁽¹⁾ | | V _{CC} - 0.60 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 3 mA ⁽²⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 10 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OLmax) = 5 mA ⁽²⁾ | 3 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OLmax) = 15 mA ⁽³⁾ | | V _{SS} | V _{SS} + 0.60 | |

- (1) The maximum total current, I_(OHmax), for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Section 5.3 for more details.
- (2) The maximum total current, I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
- (3) The maximum total current, I_(OLmax), for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

5.8.4.1 Typical Characteristics, General-Purpose I/O (Full Drive Strength)

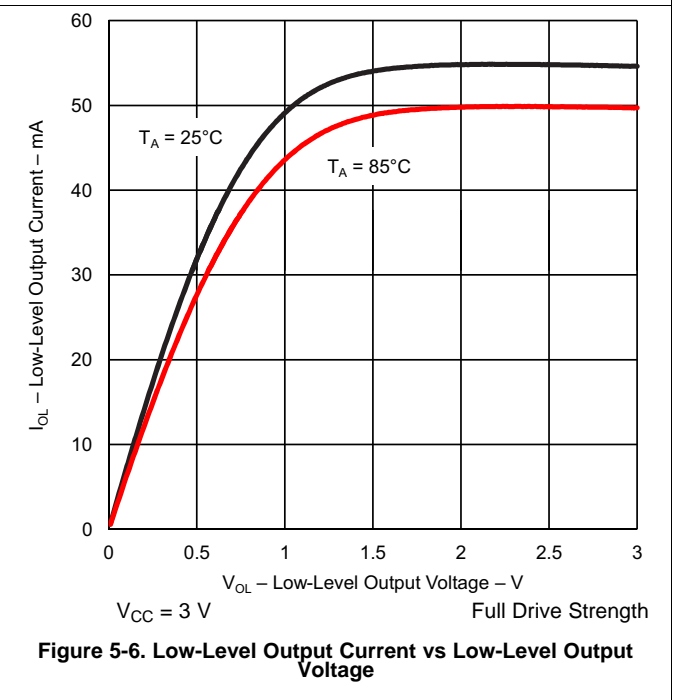
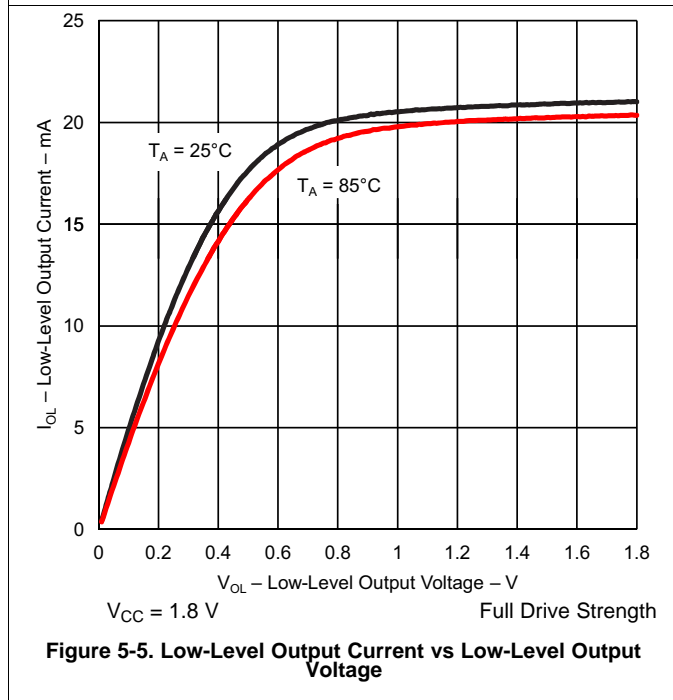
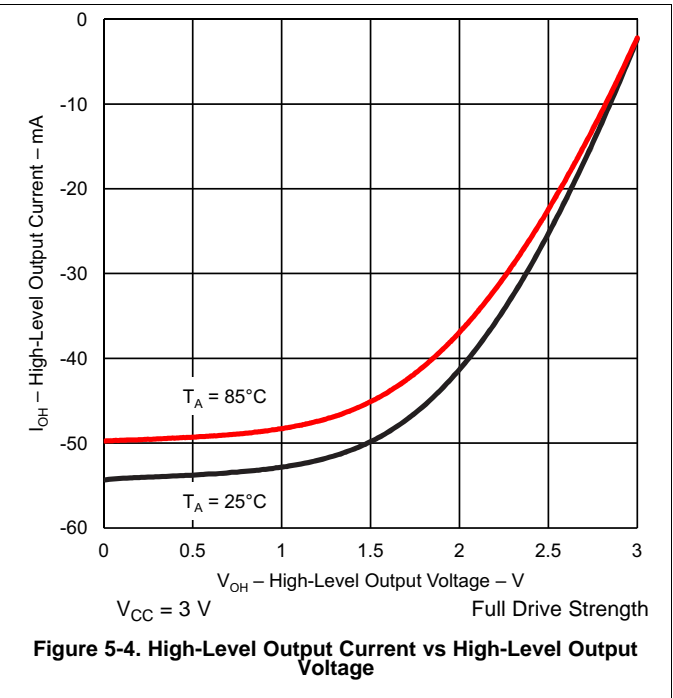
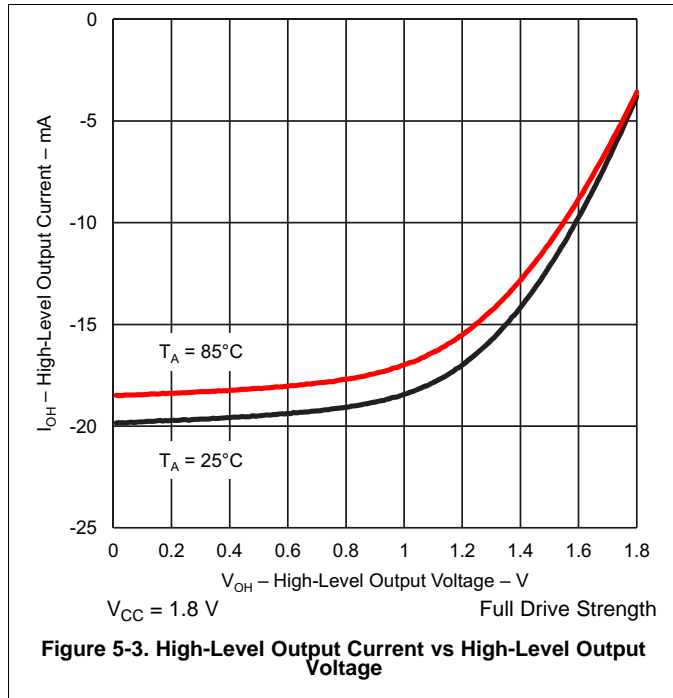


Table 5-10 lists the output characteristics of the GPIOs in reduced drive strength mode. Also see Figure 5-7 through Figure 5-10.

Table 5-10. Outputs, General-Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|---------------------------|---|-----------------|------------------------|------------------------|------|
| V _{OH} | High-level output voltage | I _(OHmax) = -1 mA ⁽²⁾ | 1.8 V | V _{CC} - 0.25 | V _{CC} | V |
| | | I _(OHmax) = -3 mA ⁽²⁾ | | V _{CC} - 0.60 | V _{CC} | |
| | | I _(OHmax) = -2 mA ⁽²⁾ | 3.0 V | V _{CC} - 0.25 | V _{CC} | |
| | | I _(OHmax) = -6 mA ⁽²⁾ | | V _{CC} - 0.60 | V _{CC} | |
| V _{OL} | Low-level output voltage | I _(OLmax) = 1 mA ⁽³⁾ | 1.8 V | V _{SS} | V _{SS} + 0.25 | V |
| | | I _(OLmax) = 3 mA ⁽⁴⁾ | | V _{SS} | V _{SS} + 0.60 | |
| | | I _(OLmax) = 2 mA ⁽³⁾ | 3.0 V | V _{SS} | V _{SS} + 0.25 | |
| | | I _(OLmax) = 6 mA ⁽⁴⁾ | | V _{SS} | V _{SS} + 0.60 | |

(1) Selecting reduced drive strength may reduce EMI.

(2) The maximum total current, I_(OHmax), for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Section 5.3 for more details.

(3) The maximum total current, I_(OLmax), for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.

(4) The maximum total current, I_(OLmax), for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

5.8.4.2 Typical Characteristics, General-Purpose I/O (Reduced Drive Strength)

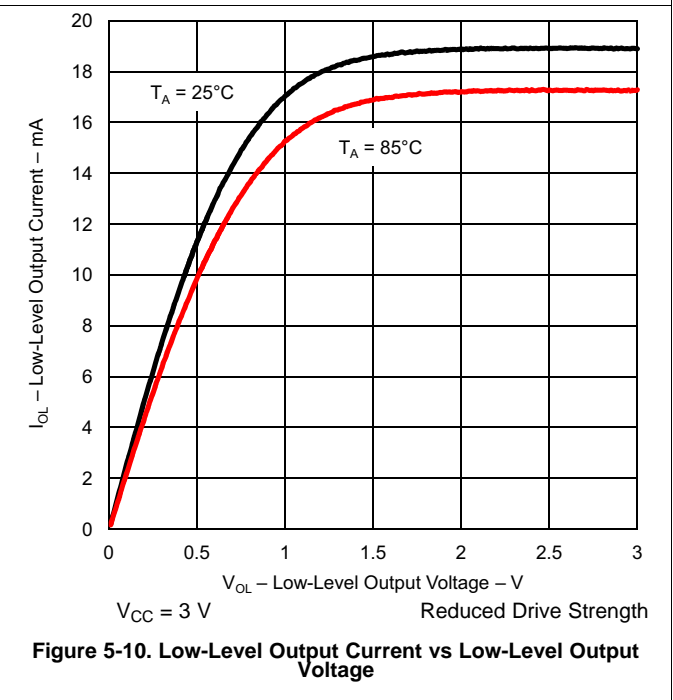
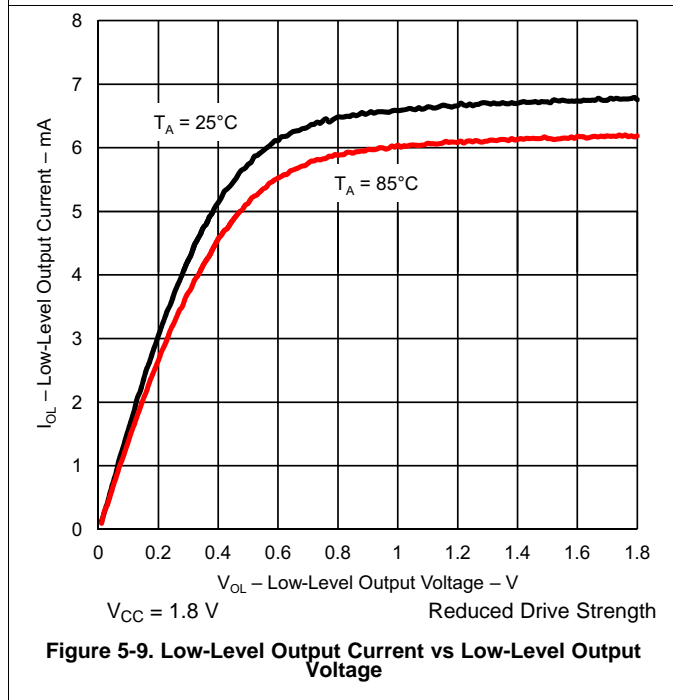
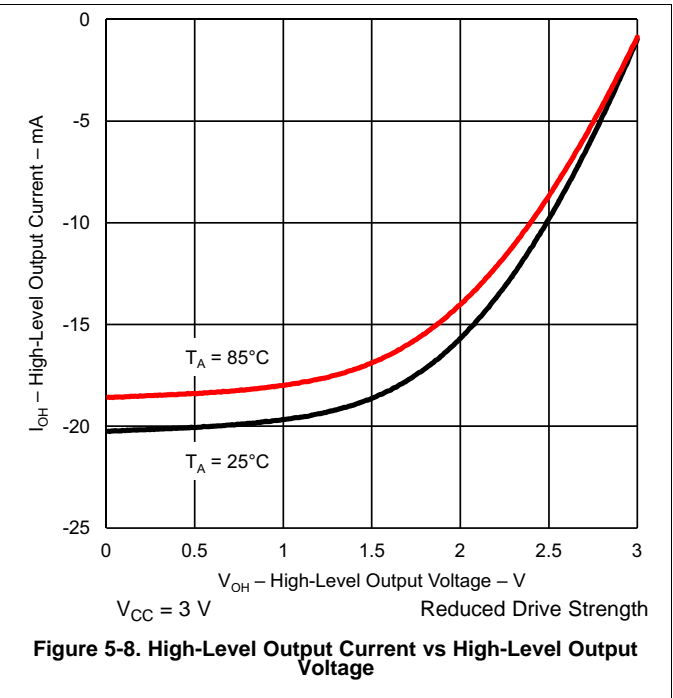
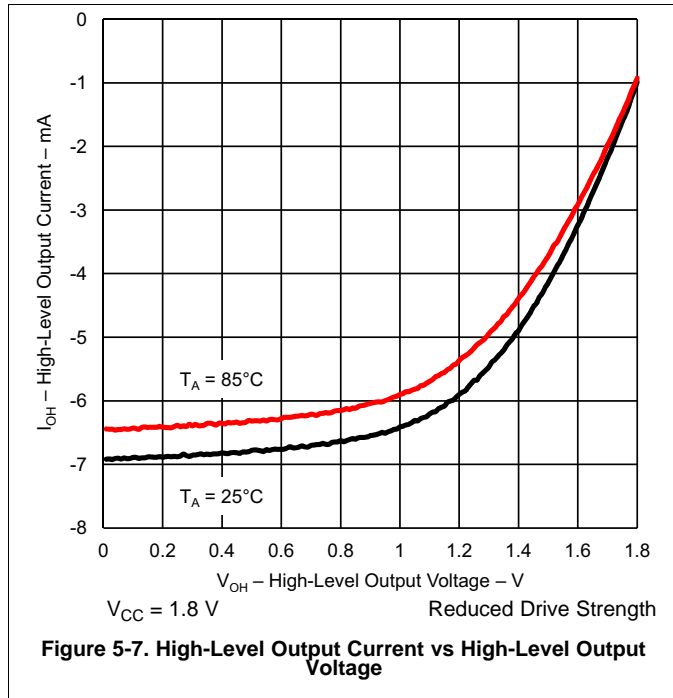


Table 5-11 lists the output frequencies of the GPIOs.

Table 5-11. Output Frequency, General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|-----------------------|-----------------------------------|---|---|-----|-----|------|
| f _{Px,y} | Port output frequency (with load) | See ⁽¹⁾ ⁽²⁾ | V _{CC} = 1.8 V, PMMCOREV _x = 0 | | 16 | MHz |
| | | | V _{CC} = 3 V, PMMCOREV _x = 3 | | 25 | |
| f _{Port_CLK} | Clock output frequency | ACLK, SMCLK, MCLK, C _L = 20 pF ⁽²⁾ | V _{CC} = 1.8 V, PMMCOREV _x = 0 | | 16 | MHz |
| | | | V _{CC} = 3 V, PMMCOREV _x = 3 | | 25 | |

- (1) A resistive divider with $2 \times R1$ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
- (2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

5.8.5 Power-Management Module (PMM)

Table 5-12 lists the characteristics of the BOR.

Table 5-12. PMM, Brownout Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|---------------------------------|------|------|------|------|
| $V_{(DVCC_BOR_IT-)}$ | BOR _H on voltage, DV _{CC} falling level | $ dDV_{CC}/dt < 3 \text{ V/s}$ | | | 1.45 | V |
| $V_{(DVCC_BOR_IT+)}$ | BOR _H off voltage, DV _{CC} rising level | $ dDV_{CC}/dt < 3 \text{ V/s}$ | 0.80 | 1.30 | 1.50 | V |
| $V_{(DVCC_BOR_hys)}$ | BOR _H hysteresis | | 50 | | 250 | mV |
| $t_{\text{RESET}}^{(1)}$ | Pulse duration required at RST/NMI pin to accept a reset | | 2 | | | μs |

(1) Pulse shorter than 2 μs might trigger reset.

Table 5-13 lists the characteristics of the PMM core voltage.

Table 5-13. PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------|--|---|-----|------|-----|------|
| $V_{\text{CORE3(AM)}}$ | Core voltage, active mode, PMMCOREV = 3 | $2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.93 | | V |
| $V_{\text{CORE2(AM)}}$ | Core voltage, active mode, PMMCOREV = 2 | $2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.83 | | V |
| $V_{\text{CORE1(AM)}}$ | Core voltage, active mode, PMMCOREV = 1 | $2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.62 | | V |
| $V_{\text{CORE0(AM)}}$ | Core voltage, active mode, PMMCOREV = 0 | $1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.42 | | V |
| $V_{\text{CORE3(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 3 | $2.4 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.96 | | V |
| $V_{\text{CORE2(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 2 | $2.2 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.94 | | V |
| $V_{\text{CORE1(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 1 | $2.0 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.74 | | V |
| $V_{\text{CORE0(LPM)}}$ | Core voltage, low-current mode, PMMCOREV = 0 | $1.8 \text{ V} \leq DV_{CC} \leq 3.6 \text{ V}$ | | 1.54 | | V |

Table 5-14 lists the characteristics of the high-side SVS.

Table 5-14. PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|---|--|------|------|------|------|
| $I_{(SVSH)}$ | SVS current consumption | SVSHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | | SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 0 | | 200 | | |
| | | SVSHE = 1, DV _{CC} = 3.6 V, SVSHFP = 1 | | 1.5 | | μA |
| $V_{(SVSH_IT-)}$ | SVS _H on voltage level ⁽¹⁾ | SVSHE = 1, SVSHRVL = 0 | 1.60 | 1.65 | 1.70 | V |
| | | SVSHE = 1, SVSHRVL = 1 | 1.77 | 1.84 | 1.90 | |
| | | SVSHE = 1, SVSHRVL = 2 | 1.97 | 2.04 | 2.10 | |
| | | SVSHE = 1, SVSHRVL = 3 | 2.09 | 2.16 | 2.23 | |
| $V_{(SVSH_IT+)}$ | SVS _H off voltage level ⁽¹⁾ | SVSHE = 1, SVSMHRRRL = 0 | 1.68 | 1.74 | 1.80 | V |
| | | SVSHE = 1, SVSMHRRRL = 1 | 1.89 | 1.95 | 2.01 | |
| | | SVSHE = 1, SVSMHRRRL = 2 | 2.08 | 2.14 | 2.21 | |
| | | SVSHE = 1, SVSMHRRRL = 3 | 2.21 | 2.27 | 2.34 | |
| | | SVSHE = 1, SVSMHRRRL = 4 | 2.35 | 2.41 | 2.49 | |
| | | SVSHE = 1, SVSMHRRRL = 5 | 2.65 | 2.72 | 2.80 | |
| | | SVSHE = 1, SVSMHRRRL = 6 | 2.96 | 3.04 | 3.13 | |
| | | SVSHE = 1, SVSMHRRRL = 7 | 2.96 | 3.04 | 3.13 | |
| $t_{pd(SVSH)}$ | SVS _H propagation delay | SVSHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVSHFP = 1 | | 2.5 | | μs |
| | | SVSHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVSHFP = 0 | | 20 | | |
| $t_{(SVSH)}$ | SVS _H on or off delay time | SVSHE = 0 → 1, SVSHFP = 1 | | 12.5 | | μs |
| | | SVSHE = 0 → 1, SVSHFP = 0 | | 100 | | |
| dV _{DVCC} /dt | DV _{CC} rise time | | 0 | | 1000 | V/s |

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. Please refer to the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and use.

Table 5-15 lists the characteristics of the high-side SVM.

Table 5-15. PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---|--|------|------|------|------|
| $I_{(SVMH)}$ | SVM _H current consumption | SVMHE = 0, DV _{CC} = 3.6 V | | 0 | | nA |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 0 | | 200 | | |
| | | SVMHE = 1, DV _{CC} = 3.6 V, SVMHFP = 1 | | 1.5 | | μA |
| $V_{(SVMH)}$ | SVM _H on or off voltage level ⁽¹⁾ | SVMHE = 1, SVSMHRRRL = 0 | 1.68 | 1.74 | 1.80 | V |
| | | SVMHE = 1, SVSMHRRRL = 1 | 1.89 | 1.95 | 2.01 | |
| | | SVMHE = 1, SVSMHRRRL = 2 | 2.08 | 2.14 | 2.21 | |
| | | SVMHE = 1, SVSMHRRRL = 3 | 2.21 | 2.27 | 2.34 | |
| | | SVMHE = 1, SVSMHRRRL = 4 | 2.35 | 2.41 | 2.49 | |
| | | SVMHE = 1, SVSMHRRRL = 5 | 2.65 | 2.72 | 2.80 | |
| | | SVMHE = 1, SVSMHRRRL = 6 | 2.96 | 3.04 | 3.13 | |
| | | SVMHE = 1, SVSMHRRRL = 7 | 2.96 | 3.04 | 3.13 | |
| | | SVMHE = 1, SVMHOVPE = 1 | | 3.79 | | |
| $t_{pd(SVMH)}$ | SVM _H propagation delay | SVMHE = 1, dV _{DVCC} /dt = 10 mV/μs, SVMHFP = 1 | | 2.5 | | μs |
| | | SVMHE = 1, dV _{DVCC} /dt = 1 mV/μs, SVMHFP = 0 | | 20 | | |
| $t_{(SVMH)}$ | SVM _H on or off delay time | SVMHE = 0 → 1, SVMHFP = 1 | | 12.5 | | μs |
| | | SVMHE = 0 → 1, SVMHFP = 0 | | 100 | | |

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. Refer to the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* on recommended settings and use.

Table 5-16 lists the characteristics of the low-side SVS.

Table 5-16. PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|--|-----|------|-----|------|
| $I_{(SVSL)}$ | SVS _L current consumption | SVSLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 0 | | 200 | | |
| | | SVSLE = 1, PMMCOREV = 2, SVSLFP = 1 | | 1.5 | | μA |
| $t_{pd(SVSL)}$ | SVS _L propagation delay | SVSLE = 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVSLFP = 1 | | 2.5 | | μs |
| | | SVSLE = 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVSLFP = 0 | | 20 | | |
| $t_{(SVSL)}$ | SVS _L on or off delay time | SVSLE = 0 → 1, SVSLFP = 1 | | 12.5 | | μs |
| | | SVSLE = 0 → 1, SVSLFP = 0 | | 100 | | |

Table 5-17 lists the characteristics of the low-side SVM.

Table 5-17. PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|--|-----|------|-----|------|
| $I_{(SVML)}$ | SVM _L current consumption | SVMLE = 0, PMMCOREV = 2 | | 0 | | nA |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 0 | | 200 | | |
| | | SVMLE = 1, PMMCOREV = 2, SVMLFP = 1 | | 1.5 | | μA |
| $t_{pd(SVML)}$ | SVM _L propagation delay | SVMLE = 1, $dV_{CORE}/dt = 10 \text{ mV}/\mu\text{s}$, SVMLFP = 1 | | 2.5 | | μs |
| | | SVMLE = 1, $dV_{CORE}/dt = 1 \text{ mV}/\mu\text{s}$, SVMLFP = 0 | | 20 | | |
| $t_{(SVML)}$ | SVM _L on or off delay time | SVMLE = 0 → 1, SVMLFP = 1 | | 12.5 | | μs |
| | | SVMLE = 0 → 1, SVMLFP = 0 | | 100 | | |

5.8.6 Auxiliary Supplies Module

Table 5-18 lists the recommended operating conditions of the auxiliary supplies.

Table 5-18. Auxiliary Supplies, Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------------------|--|------------------|-----|-----|---------|
| V_{CC} | Supply voltage for all supplies at pins DVCC, AVCC, AUX1, AUX2, AUX3 | 1.8 | | 3.6 | V |
| V_{DSYS} | Digital system supply voltage range, $V_{DSYS} = V_{CC} - R_{ON} \times I_{LOAD}$ | PMMCOREVx = 0 | | 3.6 | V |
| | | PMMCOREVx = 1 | 2.0 | 3.6 | |
| | | PMMCOREVx = 2 | 2.2 | 3.6 | |
| | | PMMCOREVx = 3 | 2.4 | 3.6 | |
| V_{ASYS} | Analog system supply voltage range, $V_{ASYS} = V_{CC} - R_{ON} \times I_{LOAD}$ | Refer to modules | | | V |
| C_{VCC} , $C_{AUX1/2}$ | Recommended capacitor at pins DVCC, AVCC, AUX1, AUX2 | 4.7 | | | μ F |
| C_{VSYs} | Recommended capacitor at pins VDSYS and VASYS | 4.7 | | | μ F |
| C_{VCORE} | Recommended capacitance at pin V CORE | 0.47 | | | μ F |
| C_{AUX3} | Recommended capacitor at pin AUX3 | 0.47 | | | μ F |

Table 5-19 lists the current consumption of AUX3.

Table 5-19. Auxiliary Supplies, AUX3 (Backup Subsystem) Currents

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | T_A | MIN | MAX | UNIT |
|-------------------|--------------------------------|----------|-------|-----|------|---------|
| $I_{AUX3,RTCOn}$ | AUX3 current with RTC enabled | 3 V | 25°C | | 0.83 | μ A |
| | | | 85°C | | 0.95 | |
| $I_{AUX3,RTCoFF}$ | AUX3 current with RTC disabled | 3 V | 25°C | | 110 | nA |
| | | | 85°C | | 165 | |

Table 5-20 lists the characteristics of the auxiliary supply monitor.

Table 5-20. Auxiliary Supplies, Auxiliary Supply Monitor

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|--------------------|---|-------------|------|------|------|---------|
| $I_{CC,Monitor}$ | Average supply current for monitoring circuitry drawn from VDSYS (also see Figure 5-11) | 3 V | | | 0.70 | μ A |
| $I_{Meas,Monitor}$ | Average current drawn from monitored supply during measurement cycle (also see Figure 5-12) | | | | 0.11 | μ A |
| $V_{Monitor}$ | Auxiliary supply threshold level | AUXLVLx = 0 | 1.67 | 1.74 | 1.80 | V |
| | | AUXLVLx = 1 | 1.87 | 1.95 | 2.01 | |
| | | AUXLVLx = 2 | 2.06 | 2.14 | 2.21 | |
| | | AUXLVLx = 3 | 2.19 | 2.27 | 2.33 | |
| | | AUXLVLx = 4 | 2.33 | 2.41 | 2.48 | |
| | | AUXLVLx = 5 | 2.63 | 2.72 | 2.79 | |
| | | AUXLVLx = 6 | 2.91 | 3.02 | 3.10 | |
| | | AUXLVLx = 7 | 2.91 | 3.02 | 3.10 | |

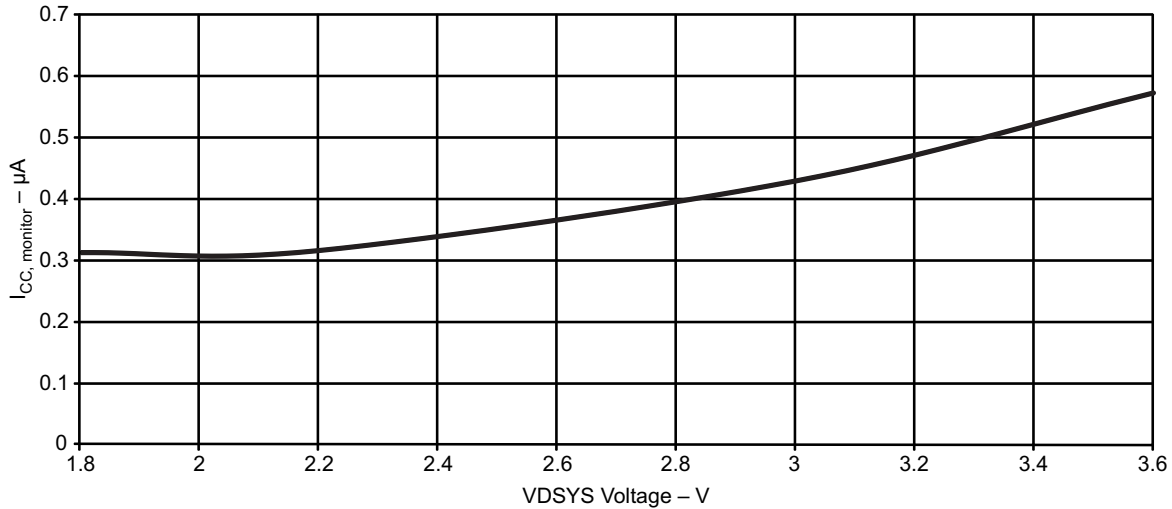


Figure 5-11. VDSYS Voltage vs $I_{CC,Monitor}$

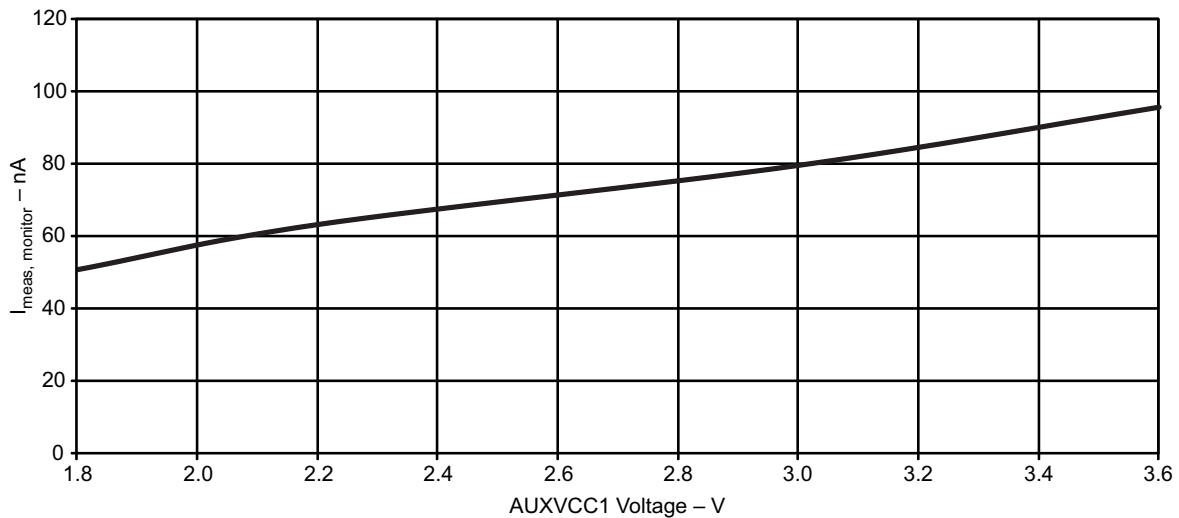


Figure 5-12. AUXVCC1 Voltage vs $I_{Meas,Monitor}$

Table 5-21 lists the AUX switch ON resistance characteristics.

Table 5-21. Auxiliary Supplies, Switch ON-Resistance

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------|---|--|-----|-----|----------|
| $R_{ON,DVCC}$ | ON-resistance of switch between DVCC and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO} = 10 \text{ mA} + 10 \text{ mA} = 20 \text{ mA}$ | | 5 | Ω |
| $R_{ON,DAUX1}$ | ON-resistance of switch between AUX1 and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO} = 10 \text{ mA} + 10 \text{ mA} = 20 \text{ mA}$ | | 5 | Ω |
| $R_{ON,DAUX2}$ | ON-resistance of switch between AUX2 and VDSYS | $I_{LOAD} = I_{CORE} + I_{IO} = 10 \text{ mA} + 10 \text{ mA} = 20 \text{ mA}$ | | 5 | Ω |
| $R_{ON,AVCC}$ | ON-resistance of switch between AVCC and V_{ASYS} | $I_{LOAD} = I_{Modules} = 10 \text{ mA}$ | | 5 | Ω |
| $R_{ON,AAUX1}$ | ON-resistance of switch between AUX1 and V_{ASYS} | $I_{LOAD} = I_{Modules} = 5 \text{ mA}$ | | 20 | Ω |
| $R_{ON,AAUX2}$ | ON-resistance of switch between AUX2 and V_{ASYS} | $I_{LOAD} = I_{Modules} = 5 \text{ mA}$ | | 20 | Ω |

Table 5-22 lists the switching times of the auxiliary supplies.

Table 5-22. Auxiliary Supplies, Switching Time

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|----------------------|---|-----|-----|---------------|
| t_{Switch} | Time from occurrence of trigger (SVM or software) to "new" supply connected to system supplies | | 100 | ns |
| t_{Recover} | "Recovery time" after a switch over takes place; during this time, no further switching takes place | 200 | 450 | μs |

Table 5-23 lists the leakage characteristics of the auxiliary supplies switch.

Table 5-23. Auxiliary Supplies, Switch Leakage

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|---|-----|-----|-----|------|
| $I_{\text{SW,Lkg}}$ | Current into DVCC, AVCC, AUX1 or AUX2 if not selected | Per supply (but not the highest supply) | | 50 | 100 | nA |
| I_{Vmax} | Current drawn from highest supply | | 450 | 730 | | nA |

Table 5-24 lists the characteristics of the auxiliary supplies to the ADC.

Table 5-24. Auxiliary Supplies, Auxiliary Supplies to ADC10_A

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|-------------------------|---|--|-----------------|------|------|------|------------|
| V_3 | Supply voltage divider $V_3 = V_{\text{Supply}} / 3$ | | 1.8 V | 0.58 | 0.60 | 0.62 | V |
| | | | 3.0 V | 0.98 | 1.00 | 1.02 | |
| | | | 3.6 V | 1.18 | 1.20 | 1.22 | |
| R_{V_3} | Load resistance | AUXADCRx = 0 | | | | 18 | k Ω |
| | | AUXADCRx = 1 | | | | 1.5 | |
| | | AUXADCRx = 2 | | | | 0.6 | |
| t_{Sample,V_3} | Sampling time required if V_3 selected | AUXADC = 1, ADC10ON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB | AUXADCRx = 0 | | 1000 | | ns |
| | | | AUXADCRx = 1 | | 1000 | | |
| | | | AUXADCRx = 2 | | 1000 | | |

Table 5-25 lists the characteristics of the charge-limiting resistor.

Table 5-25. Auxiliary Supplies, Charge-Limiting Resistor

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|---------------------|--------------------------|-----------------|-----------------|-----|-----|-----|------------|
| R_{CHARGE} | Charge limiting resistor | CHCx = 1 | 3 V | | | 5 | k Ω |
| | | CHCx = 2 | 3 V | | | 10 | |
| | | CHCx = 3 | 3 V | | | 20 | |

5.8.7 Timer_A Module

Table 5-26 lists the characteristics of the Timer_A.

Table 5-26. Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------|--|-----------------|-----|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10% | 1.8 V, 3 V | | | 25 | MHz |
| t _{TA,cap} | Timer_A capture timing | All capture inputs, Minimum pulse duration required for capture | 1.8 V, 3 V | 20 | | | ns |

5.8.8 eUSCI Module

Table 5-27 lists the supported clock frequencies of the eUSCI in UART mode.

Table 5-27. eUSCI (UART Mode) Clock Frequency

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---------------------|--|---|-----|---------------------|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK or ACLK, External: UCLK, Duty cycle = 50% ± 10% | | f _{SYSTEM} | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in MBaud) | | | 5 | MHz |

Table 5-28 lists the switching characteristics of the eUSCI in UART mode.

Table 5-28. eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|---|-----------------|-----------------|-----|-----|-----|------|
| t _t | UART receive deglitch time ⁽¹⁾ | UCGLITx = 0 | 2 V, 3 V | 10 | 15 | 25 | ns |
| | | UCGLITx = 1 | | 30 | 50 | 85 | |
| | | UCGLITx = 2 | | 50 | 80 | 150 | |
| | | UCGLITx = 3 | | 70 | 120 | 200 | |

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

Table 5-29 lists the supported clock frequencies of the eUSCI in SPI master mode.

Table 5-29. eUSCI (SPI Master Mode) Clock Frequency

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-------------|-----------------------------|--|-----|--------------|------|
| f_{eUSCI} | eUSCI input clock frequency | Internal: SMCLK or ACLK, Duty cycle = 50% \pm 10% | | f_{SYSTEM} | MHz |

Table 5-30 lists the switching characteristics of the eUSCI in SPI master mode.

Table 5-30. eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V_{CC} | MIN | MAX | UNIT |
|----------------|---|--|----------|-----|-----|------|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V, 3 V | 150 | | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V, 3 V | 150 | | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V, 3 V | 200 | | ns |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V, 3 V | 200 | | |
| $t_{STE,ACC}$ | STE access time, STE active to SIMO data out | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V | | 50 | ns |
| | | | 3 V | | 30 | |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V | | 50 | |
| | | | 3 V | | 30 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SIMO high impedance | UCSTEM = 0, UCMODEx = 01 or 10 | 2 V | | 40 | ns |
| | | | 3 V | | 25 | |
| | | UCSTEM = 1, UCMODEx = 01 or 10 | 2 V | | 40 | |
| | | | 3 V | | 25 | |
| $t_{SU,MI}$ | SOMI input data setup time | | 2 V | | 50 | ns |
| | | | 3 V | | 30 | |
| $t_{HD,MI}$ | SOMI input data hold time | | 2 V | | 0 | ns |
| | | | 3 V | | 0 | |
| $t_{VALID,MO}$ | SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, $C_L = 20$ pF | 2 V | | 9 | ns |
| | | | 3 V | | 5 | |
| $t_{HD,MO}$ | SIMO output data hold time ⁽³⁾ | $C_L = 20$ pF | 2 V | | 0 | ns |
| | | | 3 V | | 0 | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$

For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 5-13 and Figure 5-14.

(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 5-13 and Figure 5-14.

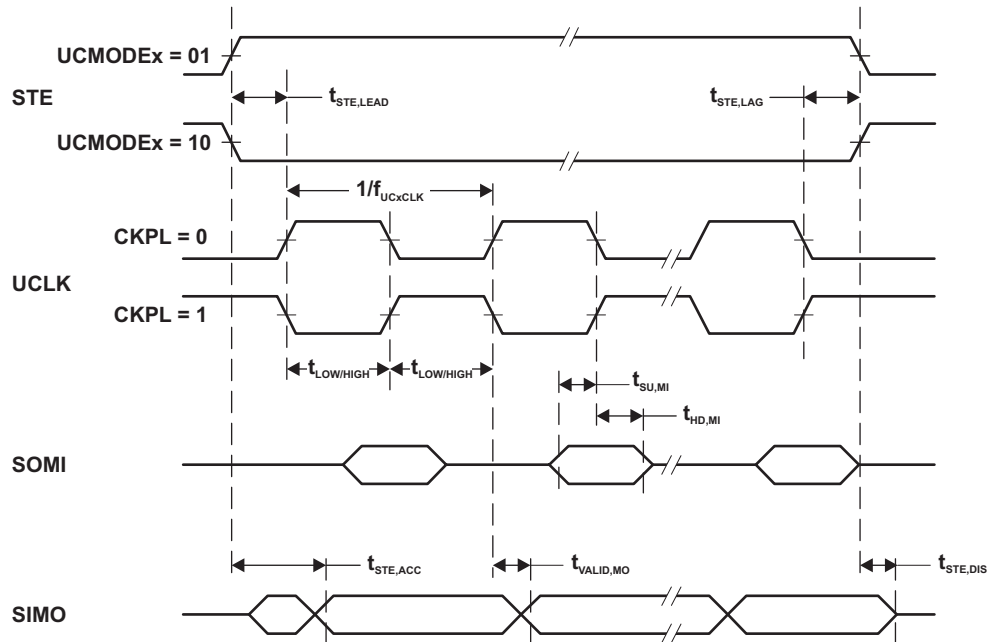


Figure 5-13. BadDriveBacuSPI Master Mode, CKPH = 0

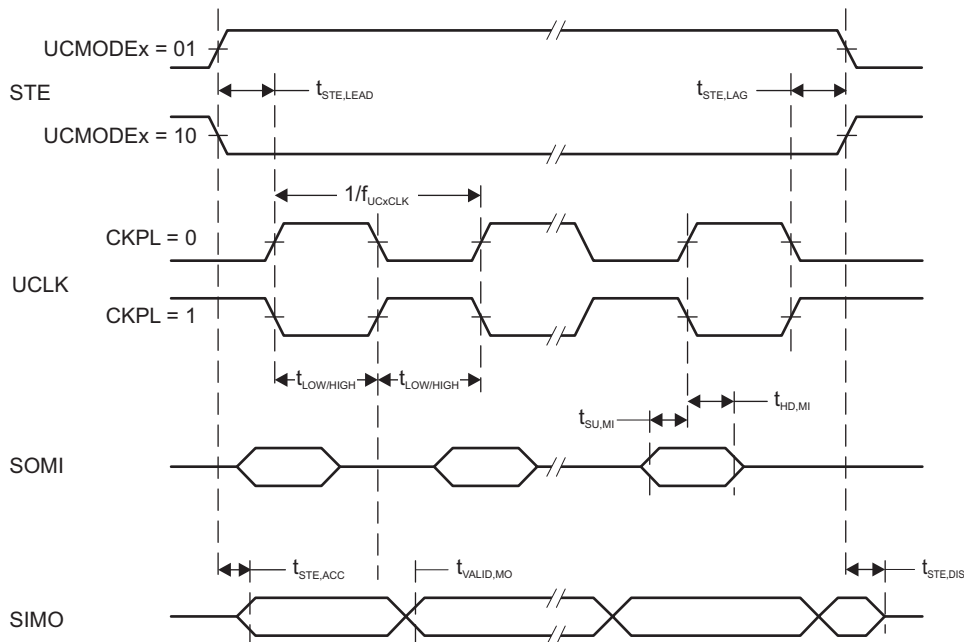


Figure 5-14. SPI Master Mode, CKPH = 1

Table 5-31 lists the switching characteristics of the eUSCI in SPI slave mode.

Table 5-31. eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|--|---|-----------------|-----|-----|------|
| t _{STE,LEAD} STE lead time, STE active to clock | | 2.0 V | 4 | | ns |
| | | 3.0 V | 3 | | |
| t _{STE,LAG} STE lag time, Last clock to STE inactive | | 2.0 V | 0 | | ns |
| | | 3.0 V | 0 | | |
| t _{STE,ACC} STE access time, STE active to SOMI data out | | 2.0 V | | 46 | ns |
| | | 3.0 V | | 24 | |
| t _{STE,DIS} STE disable time, STE inactive to SOMI high impedance | | 2.0 V | | 38 | ns |
| | | 3.0 V | | 25 | |
| t _{SU,SI} SIMO input data setup time | | 2.0 V | 2 | | ns |
| | | 3.0 V | 1 | | |
| t _{HD,SI} SIMO input data hold time | | 2.0 V | 2 | | ns |
| | | 3.0 V | 2 | | |
| t _{VALID,SO} SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF | 2.0 V | | 55 | ns |
| | | 3.0 V | | 32 | |
| t _{HD,SO} SOMI output data hold time ⁽³⁾ | C _L = 20 pF | 2.0 V | 24 | | ns |
| | | 3.0 V | 16 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.
- (2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 5-13 and Figure 5-14.
- (3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 5-15 and Figure 5-16.

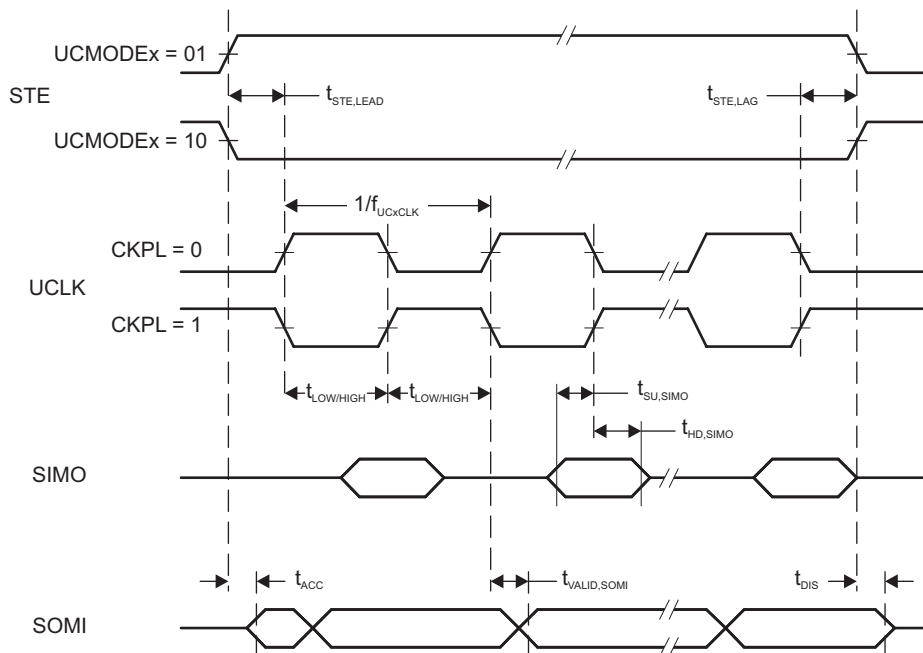


Figure 5-15. SPI Slave Mode, CKPH = 0

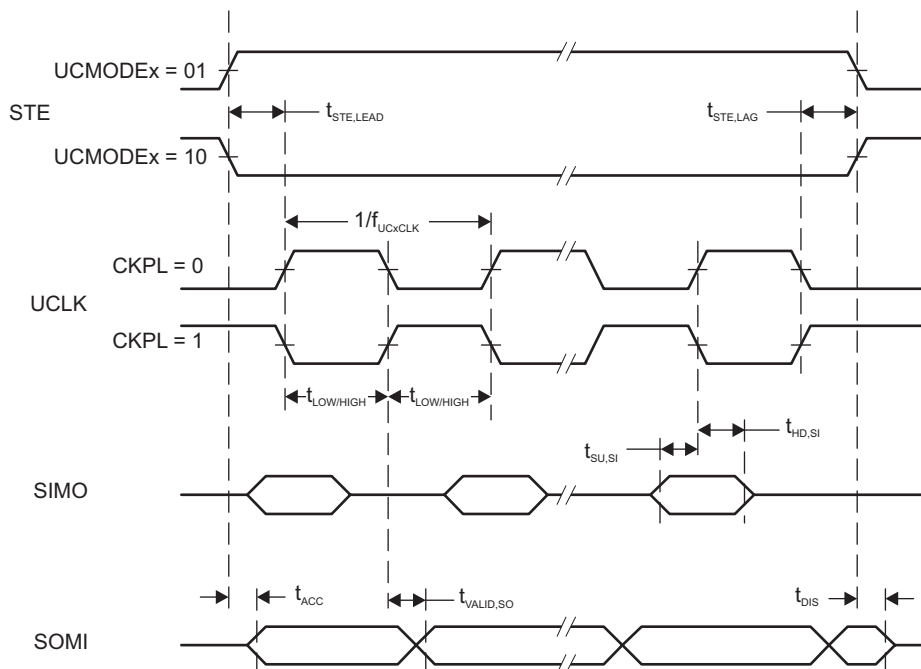


Figure 5-16. SPI Slave Mode, CKPH = 1

Table 5-32 lists the characteristics of the eUSCI in I²C mode.

Table 5-32. eUSCI (I²C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-17)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|---|--|----------|----------------------|------------------------|------|
| f _{eUSCI} | eUSCI input clock frequency | | | | f _{SYSTEM} | MHz |
| f _{SCL} | SCL clock frequency | 2 V, 3 V | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} = 100 kHz f _{SCL} > 100 kHz | 2 V, 3 V | 5.1 1.5 | | μs |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} = 100 kHz f _{SCL} > 100 kHz | 2 V, 3 V | 5.1 1.4 | | μs |
| t _{HD,DAT} | Data hold time | | 2 V, 3 V | 0.4 | | μs |
| t _{SU,DAT} | Data setup time | f _{SCL} = 100 kHz f _{SCL} > 100 kHz | 2 V, 3 V | 5.0 1.3 | | μs |
| t _{SU,STO} | Setup time for STOP | f _{SCL} = 100 kHz f _{SCL} > 100 kHz | 2 V, 3 V | 5.2 1.7 | | μs |
| t _{SP} | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 UCGLITx = 1 UCGLITx = 2 UCGLITx = 3 | 2 V, 3 V | 75 35 30 20 | 220 120 60 35 | ns |
| t _{TIMEOUT} | Clock low time-out | UCCLTOx = 1 UCCLTOx = 2 UCCLTOx = 3 | 2 V, 3 V | 30 33 37 | | ms |

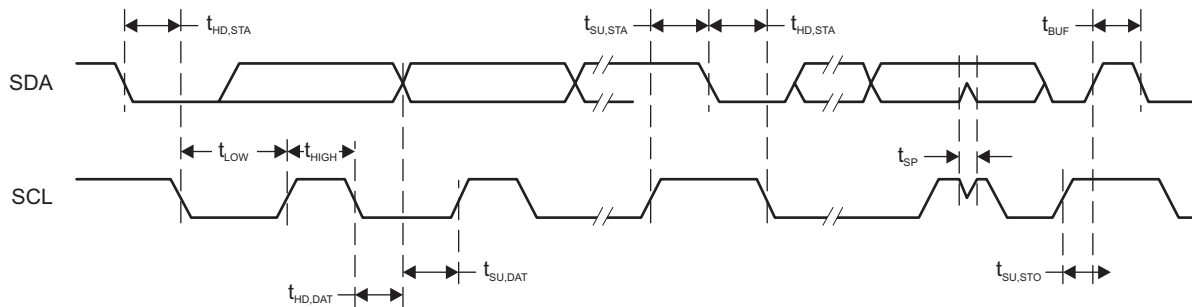


Figure 5-17. I²C Mode Timing

5.8.9 LCD Controller

Table 5-33 lists the operating conditions of the LCD.

Table 5-33. LCD_C Operating Conditions

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT | |
|----------------------------|--|---|-----------|--|---------------|-----|
| $V_{CC,LCD_C,CP\ en,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.6\text{ V}$ | | | 3.6 | V | |
| $V_{CC,LCD_C,CP\ en,3.3}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.3\text{ V}$ | | | 3.6 | V | |
| $V_{CC,LCD_C,int.\ bias}$ | Supply voltage range, internal biasing, charge pump disabled | | | 3.6 | V | |
| $V_{CC,LCD_C,ext.\ bias}$ | Supply voltage range, external biasing, charge pump disabled | | | 3.6 | V | |
| $V_{CC,LCD_C,VLCDEXT}$ | Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled | | | 3.6 | V | |
| $V_{LCDCAP/R33}$ | External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled | | | 3.6 | V | |
| C_{LCDCAP} | Capacitor on LCDCAP when charge pump enabled | | 4.7 | 10 | μF | |
| f_{LCD} | LCD frequency range | $f_{FRAME} = 1/(2 \times \text{mux}) \times f_{LCD}$ with mux = 1 (static) to 8 | | 1024 | Hz | |
| $f_{FRAME,4\text{mux}}$ | LCD frame frequency range | $f_{FRAME,4\text{mux}}(\text{MAX}) = 1/(2 \times 4) \times f_{LCD}(\text{MAX})$ $f_{LCD}(\text{MAX}) = 1/(2 \times 4) \times 1024\text{ Hz}$ | | 128 | Hz | |
| $f_{FRAME,8\text{mux}}$ | LCD frame frequency range | $f_{FRAME,8\text{mux}}(\text{MAX}) = 1/(2 \times 4) \times f_{LCD}(\text{MAX})$ $f_{LCD}(\text{MAX}) = 1/(2 \times 8) \times 1024\text{ Hz}$ | | 64 | Hz | |
| $f_{ACLK,in}$ | ACLK input frequency range | | 30 | 32 | 40 | kHz |
| C_{Panel} | Panel capacitance | | | 10000 | pF | |
| V_{R33} | Analog input voltage at R33 | | 2.4 | $V_{CC} + 0.2$ | V | |
| $V_{R23,1/3\text{bias}}$ | Analog input voltage at R23 | | V_{R13} | $V_{R33} + \frac{2}{3} \times (V_{R33} - V_{R03})$ | V_{R33} | V |
| $V_{R13,1/3\text{bias}}$ | Analog input voltage at R13 with 1/3 biasing | | V_{R03} | $V_{R03} + \frac{1}{3} \times (V_{R33} - V_{R03})$ | V_{R23} | V |
| $V_{R13,1/2\text{bias}}$ | Analog input voltage at R13 with 1/2 biasing | | V_{R03} | $V_{R03} + \frac{1}{2} \times (V_{R33} - V_{R03})$ | V_{R33} | V |
| V_{R03} | Analog input voltage at R03 | | V_{SS} | | V | |
| $V_{LCD}-V_{R03}$ | Voltage difference between V_{LCD} and R03 | | 2.4 | $V_{CC} + 0.2$ | V | |
| $V_{LCDREF/R13}$ | External LCD reference voltage applied at LCDREF/R13 | | 0.8 | 1.2 | 1.5 | V |

Table 5-34 lists the characteristics of the LCD.

Table 5-34. LCD_C Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------|--|--|-----------------|-----------------|-----|-----|------|
| V _{LCD} | LCD voltage | VLCDx = 0000, VLCDEXT = 0 | 2.4 V to 3.6 V | V _{CC} | | | V |
| | | LCDCPEN = 1, VLCDx = 0001 | 2 V to 3.6 V | 2.58 | | | |
| | | LCDCPEN = 1, VLCDx = 0010 | 2 V to 3.6 V | 2.64 | | | |
| | | LCDCPEN = 1, VLCDx = 0011 | 2 V to 3.6 V | 2.71 | | | |
| | | LCDCPEN = 1, VLCDx = 0100 | 2 V to 3.6 V | 2.78 | | | |
| | | LCDCPEN = 1, VLCDx = 0101 | 2 V to 3.6 V | 2.83 | | | |
| | | LCDCPEN = 1, VLCDx = 0110 | 2 V to 3.6 V | 2.90 | | | |
| | | LCDCPEN = 1, VLCDx = 0111 | 2 V to 3.6 V | 2.96 | | | |
| | | LCDCPEN = 1, VLCDx = 1000 | 2 V to 3.6 V | 3.02 | | | |
| | | LCDCPEN = 1, VLCDx = 1001 | 2 V to 3.6 V | 3.07 | | | |
| | | LCDCPEN = 1, VLCDx = 1010 | 2 V to 3.6 V | 3.14 | | | |
| | | LCDCPEN = 1, VLCDx = 1011 | 2 V to 3.6 V | 3.21 | | | |
| | | LCDCPEN = 1, VLCDx = 1100 | 2 V to 3.6 V | 3.27 | | | |
| | | LCDCPEN = 1, VLCDx = 1101 | 2.2 V to 3.6 V | 3.32 | | | |
| LCDCPEN = 1, VLCDx = 1110 | 2.2 V to 3.6 V | 3.38 | | | | | |
| LCDCPEN = 1, VLCDx = 1111 | 2.2 V to 3.6 V | 3.44 | | 3.6 | | | |
| I _{CC,Peak,CP} | Peak supply currents due to charge pump activities | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 400 | | | μA |
| t _{LCD,CP,on} | Time to charge C _{LCD} when discharged | C _{LCD} = 4.7 μF, LCDCPEN = 0→1, VLCDx = 1111 | 2.2 V | 150 | 500 | | ms |
| I _{CP,Load} | Maximum charge pump load current | LCDCPEN = 1, VLCDx = 1111 | 2.2 V | 50 | | | μA |
| R _{LCD,Seg} | LCD driver output impedance, segment lines | LCDCPEN = 1, VLCDx = 1000, I _{LOAD} = ±10 μA | 2.2 V | | | 10 | kΩ |
| R _{LCD,COM} | LCD driver output impedance, common lines | LCDCPEN = 1, VLCDx = 1000, I _{LOAD} = ±10 μA | 2.2 V | | | 10 | kΩ |

5.8.10 SD24_B Module

Table 5-35 lists the power supply and recommended operating conditions of the SD24_B.

Table 5-35. SD24_B Power Supply and Recommended Operating Conditions

| | | MIN | TYP | MAX | UNIT | |
|--------------------|---|---|----------------|-------------------------|-------------------------|-----|
| AV _{CC} | Analog supply voltage | AV _{CC} = DV _{CC} , AV _{SS} = DV _{SS} = 0 V | | 2.4 | 3.6 | V |
| f _{SD} | Modulator clock frequency ⁽¹⁾ | | | 0.03 | 2.3 | MHz |
| V _I | Absolute input voltage range | | | AV _{SS} – 1 | AV _{CC} | V |
| V _{IC} | Common-mode input voltage range | | | AV _{SS} – 1 | AV _{CC} | V |
| V _{ID,FS} | Differential full-scale input voltage | V _{ID} = V _{I,A+} – V _{I,A-} | | -V _{REF} /GAIN | +V _{REF} /GAIN | |
| V _{ID} | Differential input voltage for specified performance ⁽²⁾ | SD24REFS = 1 | SD24GAINx = 1 | ±910 | ±920 | mV |
| | | | SD24GAINx = 2 | ±455 | ±460 | |
| | | | SD24GAINx = 4 | ±227 | ±230 | |
| | | | SD24GAINx = 8 | ±113 | ±115 | |
| | | | SD24GAINx = 16 | ±57 | ±58 | |
| | | | SD24GAINx = 32 | ±28 | ±29 | |
| | | | SD24GAINx = 64 | ±14 | ±14.5 | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| C _{REF} | VREF load capacitance ⁽³⁾ | SD24REFS = 1 | | 100 | | nF |

- (1) Modulator clock frequency: MIN = 32.768 kHz – 10% ≈ 30 kHz. MAX = 32.768 kHz × 64 + 10% ≈ 2.3 MHz
- (2) The full-scale range (FSR) is defined by V_{FS+} = +V_{REF}/GAIN and V_{FS-} = -V_{REF}/GAIN: FSR = V_{FS+} – V_{FS-} = 2 × V_{REF} / GAIN. If V_{REF} is sourced externally, the analog input range should not exceed 80% of V_{FS+} or V_{FS-}; that is, V_{ID} = 0.8 V_{FS-} to 0.8 V_{FS+}. If V_{REF} is sourced internally, the given V_{ID} ranges apply.
- (3) There is no capacitance required on VREF. However, a capacitance of 100 nF is recommended to reduce any reference voltage noise.

Table 5-36 lists the analog input characteristics of the SD24_B.

Table 5-36. SD24_B Analog Input ⁽¹⁾

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | | |
|-----------------|--|---------------------------|-----|-----|-----|------|----------------|---------|
| C _I | Input capacitance | | | | | pF | | |
| | | | | | | | SD24GAINx = 1 | 5 |
| | | | | | | | SD24GAINx = 2 | 5 |
| | | | | | | | SD24GAINx = 4 | 5 |
| | | | | | | | SD24GAINx = 8 | 5 |
| | | | | | | | SD24GAINx = 16 | 5 |
| | SD24GAINx = 32, 64, 128 | 5 | | | | | | |
| Z _I | Input impedance (Pin A+ or A- to AV _{SS}) | f _{SD24} = 1 MHz | 3 V | | | kΩ | | |
| | | | | | | | SD24GAINx = 1 | 200 |
| | | | | | | | SD24GAINx = 8 | 200 |
| | SD24GAINx = 32 | 200 | | | | | | |
| Z _{ID} | Differential input impedance (Pin A+ to pin A-) | f _{SD24} = 1 MHz | 3 V | | | kΩ | | |
| | | | | | | | SD24GAINx = 1 | 300 400 |
| | | | | | | | SD24GAINx = 8 | 400 |
| | SD24GAINx = 32 | 300 400 | | | | | | |

- (1) All parameters pertain to each SD24_B converter.

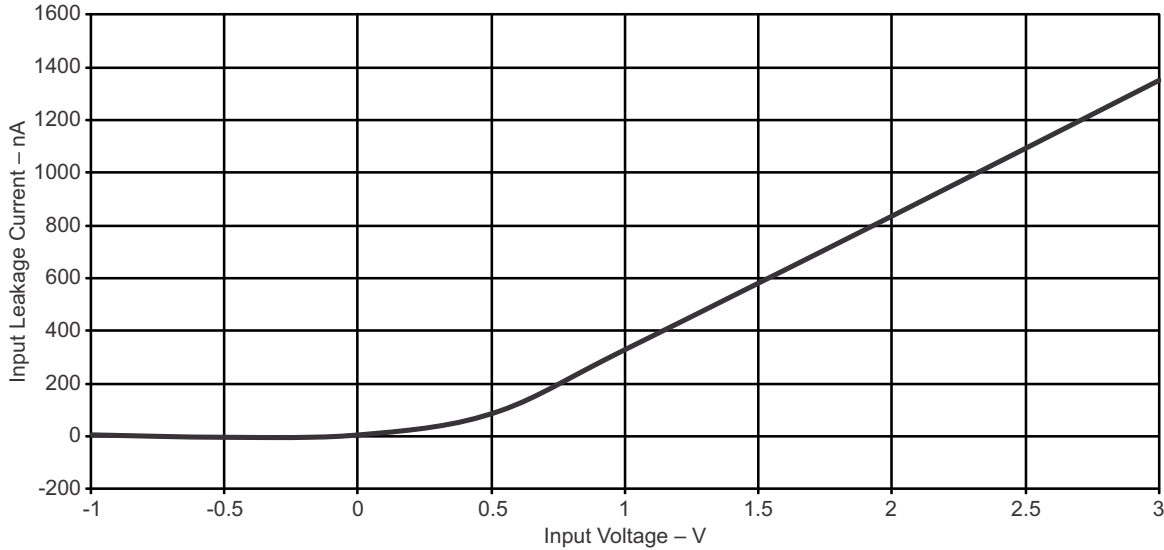


Figure 5-18. Input Leakage Current vs Input Voltage (Modulator OFF)

Table 5-37 lists the supply current of the SD24_B.

Table 5-37. SD24_B Supply Currents

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|-----------------|-----|-----|------|------|
| I _{SD,256} Analog plus digital supply current per converter (reference not included) | f _{SD24} = 1 MHz, SD24OSR = 256 | SD24GAIN: 1 | 3 V | 600 | 675 | μA |
| | | SD24GAIN: 2 | 3 V | 600 | 675 | |
| | | SD24GAIN: 4 | 3 V | 600 | 675 | |
| | | SD24GAIN: 8 | 3 V | 700 | 750 | |
| | | SD24GAIN: 16 | 3 V | 700 | 750 | |
| | | SD24GAIN: 32 | 3 V | 775 | 850 | |
| | | SD24GAIN: 64 | 3 V | 775 | 850 | |
| | | SD24GAIN: 128 | 3 V | 775 | 850 | |
| I _{SD,512} Analog plus digital supply current per converter (reference not included) | f _{SD24} = 2 MHz, SD24OSR = 512 | SD24GAIN: 1 | 3 V | 750 | 800 | μA |
| | | SD24GAIN: 8 | 3 V | 825 | 900 | |
| | | SD24GAIN: 32 | 3 V | 900 | 1000 | |

Table 5-38 lists the performance characteristics of the SD24_B.

Table 5-38. SD24_B Performance

f_{SD24} = 1 MHz, SD24OSRx = 256, SD24REFS = 1

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|-----------------|-----------------|-------|------|------|----------|
| INL Integral nonlinearity, end-point fit | SD24GAIN: 1 | 3 V | -0.01 | | 0.01 | % of FSR |
| | SD24GAIN: 8 | 3 V | -0.01 | | 0.01 | |
| | SD24GAIN: 32 | 3 V | -0.01 | | 0.01 | |
| G _{nom} Nominal gain | SD24GAIN: 1 | 3 V | | 1 | | |
| | SD24GAIN: 2 | 3 V | | 2 | | |
| | SD24GAIN: 4 | 3 V | | 4 | | |
| | SD24GAIN: 8 | 3 V | | 8 | | |
| | SD24GAIN: 16 | 3 V | | 16 | | |
| | SD24GAIN: 32 | 3 V | | 31.7 | | |
| | SD24GAIN: 64 | 3 V | | 63.4 | | |
| SD24GAIN: 128 | 3 V | | 126.8 | | | |

Table 5-38. SD24_B Performance (continued)

$f_{SD24} = 1$ MHz, SD24OSRx = 256, SD24REFS = 1

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------------------|--|---|-----------------|------|------|------|--------|
| E _G | Gain error ⁽¹⁾ | SD24GAIN: 1, with external reference (1.2 V) | 3 V | -1% | | +1% | |
| | | SD24GAIN: 8, with external reference (1.2 V) | 3 V | -2% | | +2% | |
| | | SD24GAIN: 32, with external reference (1.2 V) | 3 V | -2% | | +2% | |
| ΔE _G /ΔT | Gain error temperature coefficient ⁽²⁾ , internal reference | SD24GAIN: 1, 8, or 32 (with internal reference) | 3 V | | | 50 | ppm/°C |
| ΔE _G /ΔV _{CC} | Gain error vs V _{CC} ⁽³⁾ | SD24GAIN: 1 | | | 0.15 | | %V |
| | | SD24GAIN: 8 | | | 0.15 | | |
| | | SD24GAIN: 32 | | | 0.4 | | |
| E _{OS} [V] | Offset error ⁽⁴⁾ | SD24GAIN: 1 (with V _{diff} = 0 V) | 3 V | | | 2.3 | mV |
| | | SD24GAIN: 8 | 3 V | | | 0.73 | |
| | | SD24GAIN: 32 | 3 V | | | 0.18 | |
| E _{OS} [FS] | Offset error ⁽⁴⁾ | SD24GAIN: 1 (with V _{diff} = 0 V) | 3 V | -0.2 | | 0.2 | % FS |
| | | SD24GAIN: 8 | 3 V | -0.5 | | 0.5 | |
| | | SD24GAIN: 32 | 3 V | -0.5 | | 0.5 | |
| ΔE _{OS} /ΔT | Offset error temperature coefficient ⁽⁵⁾ | SD24GAIN: 1 | 3 V | | 1 | | μV/°C |
| | | SD24GAIN: 8 | 3 V | | 0.15 | | |
| | | SD24GAIN: 32 | 3 V | | 0.1 | | |
| ΔE _{OS} /ΔV _{CC} | Offset error vs V _{CC} ⁽⁶⁾ | SD24GAIN: 1 | | | 600 | | μV/V |
| | | SD24GAIN: 8 | | | 100 | | |
| | | SD24GAIN: 32 | | | 50 | | |
| CMRR,DC | Common-mode rejection at DC ⁽⁷⁾ | SD24GAIN: 1 | 3 V | | -110 | | dB |
| | | SD24GAIN: 8 | 3 V | | -110 | | |
| | | SD24GAIN: 32 | 3 V | | -110 | | |

- The gain error E_G specifies the deviation of the actual gain G_{act} from the nominal gain G_{nom}: $E_G = (G_{act} - G_{nom})/G_{nom}$. It covers process, temperature and supply voltage variations.
- The gain error temperature coefficient ΔE_G / ΔT specifies the variation of the gain error E_G over temperature ($E_G(T) = (G_{act}(T) - G_{nom})/G_{nom}$) using the box method (that is, MIN and MAX values):
 $\Delta E_G / \Delta T = (MAX(E_G(T)) - MIN(E_G(T))) / (MAX(T) - MIN(T)) = (MAX(G_{act}(T)) - MIN(G_{act}(T))) / G_{nom} / (MAX(T) - MIN(T))$
with T ranging from -40°C to +85°C.
- The gain error vs V_{CC} coefficient ΔE_G / ΔV_{CC} specifies the variation of the gain error E_G over supply voltage ($E_G(V_{CC}) = (G_{act}(V_{CC}) - G_{nom})/G_{nom}$) using the box method (that is, MIN and MAX values):
 $\Delta E_G / \Delta V_{CC} = (MAX(E_G(V_{CC})) - MIN(E_G(V_{CC}))) / (MAX(V_{CC}) - MIN(V_{CC})) = (MAX(G_{act}(V_{CC})) - MIN(G_{act}(V_{CC}))) / G_{nom} / (MAX(V_{CC}) - MIN(V_{CC}))$
with V_{CC} ranging from 2.4 V to 3.6 V.
- The offset error E_{OS} is measured with shorted inputs in 2s-complement mode with +100% FS = V_{REF} / G and -100% FS = -V_{REF} / G. Conversion between E_{OS} [FS] and E_{OS} [V] is as follows: E_{OS} [FS] = E_{OS} [V] × G / V_{REF}; E_{OS} [V] = E_{OS} [FS] × V_{REF} / G.
- The offset error temperature coefficient ΔE_{OS} / ΔT specifies the variation of the offset error E_{OS} over temperature using the box method (that is, MIN and MAX values):
 $\Delta E_{OS} / \Delta T = (MAX(E_{OS}(T)) - MIN(E_{OS}(T))) / (MAX(T) - MIN(T))$
with T ranging from -40°C to +85°C.
- The offset error vs V_{CC} ΔE_{OS} / ΔV_{CC} specifies the variation of the offset error E_{OS} over supply voltage using the box method (that is, MIN and MAX values):
 $\Delta E_{OS} / \Delta V_{CC} = (MAX(E_{OS}(V_{CC})) - MIN(E_{OS}(V_{CC}))) / (MAX(V_{CC}) - MIN(V_{CC}))$
with V_{CC} ranging from 2.4 V to 3.6 V.
- The DC CMRR specifies the change in the measured differential input voltage value when the common-mode voltage varies:
DC CMRR = -20log(Δ_{MAX}/FSR) with Δ_{MAX} being the difference between the minimum value and the maximum value measured when sweeping the common-mode voltage (for example, calculating with 16-bit FSR = 65536, a maximum change by 1 LSB results in -20log(1/65536) ≈ -96 dB).
The DC CMRR is measured with both inputs connected to the common-mode voltage (that is, no differential input signal is applied), and the common-mode voltage is swept from -1 V to V_{CC}.

Table 5-38. SD24_B Performance (continued)
 $f_{SD24} = 1 \text{ MHz}$, $SD24OSRx = 256$, $SD24REFS = 1$

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------|--|---|-----------------|-----|------|-----|------|
| CMRR,50Hz | Common-mode rejection at 50 Hz ⁽⁸⁾ | SD24GAIN: 1, $f_{CM} = 50 \text{ Hz}$, $V_{CM} = 930 \text{ mV}$ | 3 V | | -110 | | dB |
| | | SD24GAIN: 8, $f_{CM} = 50 \text{ Hz}$, $V_{CM} = 120 \text{ mV}$ | 3 V | | -110 | | |
| | | SD24GAIN: 32, $f_{CM} = 50 \text{ Hz}$, $V_{CM} = 30 \text{ mV}$ | 3 V | | -110 | | |
| AC PSRR,ext | AC power supply rejection ratio, external reference ⁽⁹⁾ | SD24GAIN: 1, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -61 | | dB |
| | | SD24GAIN: 8, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -77 | | |
| | | SD24GAIN: 32, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -79 | | |
| AC PSRR,int | AC power supply rejection ratio, internal reference ⁽⁹⁾ | SD24GAIN: 1, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -61 | | dB |
| | | SD24GAIN: 8, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -77 | | |
| | | SD24GAIN: 32, $V_{CC} = 3 \text{ V} + 50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$, $f_{VCC} = 50 \text{ Hz}$ | | | -79 | | |
| XT | Crosstalk between converters ⁽¹⁰⁾ | Crosstalk source: SD24GAIN: 1, Sine wave with maximum possible V _{pp} , $f_{IN} = 50 \text{ Hz}$ or 100 Hz , Converter under test: SD24GAIN: 1 | 3 V | | -120 | | dB |
| | | Crosstalk source: SD24GAIN: 1, Sine wave with maximum possible V _{pp} , $f_{IN} = 50 \text{ Hz}$ or 100 Hz , Converter under test: SD24GAIN: 8 | 3 V | | -115 | | |
| | | Crosstalk source: SD24GAIN: 1, Sine wave with maximum possible V _{pp} , $f_{IN} = 50 \text{ Hz}$ or 100 Hz , Converter under test: SD24GAIN: 32 | 3 V | | -100 | | |

- (8) The AC CMRR is the difference between a hypothetical signal with the amplitude and frequency of the applied common-mode ripple applied to the inputs of the ADC and the actual common-mode signal spur visible in the FFT spectrum:
 $AC \text{ CMRR} = \text{Error Spur [dBFS]} - 20\log(V_{CM} / 1.2 \text{ V} / G) \text{ [dBFS]}$ with a common-mode signal of $V_{CM} \times \sin(2\pi \times f_{CM} \times t)$ applied to the analog inputs.
The AC CMRR is measured with the both inputs connected to the common-mode signal (that is, no differential input signal is applied). With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).
- (9) The AC PSRR is the difference between a hypothetical signal with the amplitude and frequency of the applied supply voltage ripple applied to the inputs of the ADC and the actual supply ripple spur visible in the FFT spectrum:
 $AC \text{ PSRR} = \text{Error Spur [dBFS]} - 20\log(50 \text{ mV} / 1.2 \text{ V} / G) \text{ [dBFS]}$ with a signal of $50 \text{ mV} \times \sin(2\pi \times f_{VCC} \times t)$ added to V_{CC} .
The AC PSRR is measured with the inputs grounded (that is, no analog input signal is applied).
With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).
SD24GAIN: 1 → Hypothetical signal: $20\log(50 \text{ mV} / 1.2 \text{ V} / 1) = -27.6 \text{ dBFS}$
SD24GAIN: 8 → Hypothetical signal: $20\log(50 \text{ mV} / 1.2 \text{ V} / 8) = -9.5 \text{ dBFS}$
SD24GAIN: 32 → Hypothetical signal: $20\log(50 \text{ mV} / 1.2 \text{ V} / 32) = 2.5 \text{ dBFS}$
- (10) The crosstalk (XT) is specified as the tone level of the signal applied to the crosstalk source seen in the spectrum of the converter under test. It is measured with the inputs of the converter under test being grounded.

Table 5-39 lists the AC performance characteristics of the SD24_B.

Table 5-39. SD24_B AC Performance

$f_{SD24} = 1 \text{ MHz}$, $SD24OSRx = 256$, $SD24REFS = 1$

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------|------------------------------------|-----------------|--------------------------------|-----|-----|-----|------|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN} = 50 \text{ Hz}^{(1)}$ | 3 V | 85 | 87 | dB |
| | | SD24GAIN: 2 | | | 86 | | |
| | | SD24GAIN: 4 | | | 85 | | |
| | | SD24GAIN: 8 | | | 82 | 84 | |
| | | SD24GAIN: 16 | | | 80 | | |
| | | SD24GAIN: 32 | | | 73 | 74 | |
| | | SD24GAIN: 64 | | | 68 | | |
| | | SD24GAIN: 128 | | | 62 | | |
| THD | Total harmonic distortion | SD24GAIN: 1 | $f_{IN} = 50 \text{ Hz}^{(1)}$ | 3 V | 100 | dB | |
| | | SD24GAIN: 8 | | | 90 | | |
| | | SD24GAIN: 32 | | | 80 | | |

(1) The following voltages were applied to the SD24_B inputs:

$$V_{I,A+}(t) = 0 \text{ V} + V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$$

$$V_{I,A-}(t) = 0 \text{ V} - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$$

resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

Table 5-40 lists the AC performance characteristics of the SD24_B.

Table 5-40. SD24_B AC Performance

$f_{SD24} = 2 \text{ MHz}$, $SD24OSRx = 512$, $SD24REFS = 1$

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------|------------------------------------|-----------------|--------------------------------|-----|-----|-----|------|
| SINAD | Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN} = 50 \text{ Hz}^{(1)}$ | 3 V | 87 | dB | |
| | | SD24GAIN: 2 | | | 86 | | |
| | | SD24GAIN: 4 | | | 85 | | |
| | | SD24GAIN: 8 | | | 84 | | |
| | | SD24GAIN: 16 | | | 81 | | |
| | | SD24GAIN: 32 | | | 76 | | |
| | | SD24GAIN: 64 | | | 71 | | |
| | | SD24GAIN: 128 | | | 65 | | |

(1) The following voltages were applied to the SD24_B inputs:

$$V_{I,A+}(t) = 0 \text{ V} + V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$$

$$V_{I,A-}(t) = 0 \text{ V} - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$$

resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

Table 5-41 lists the AC performance characteristics of the SD24_B.

Table 5-41. SD24_B AC Performance

$f_{SD24} = 32$ kHz, $SD24OSRx = 512$, $SD24REFS = 1$

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|-----------------|---------------------------------|-----|-----|-----|------|
| SINAD Signal-to-noise + distortion ratio | SD24GAIN: 1 | $f_{IN} = 12$ Hz ⁽¹⁾ | 3 V | | 89 | dB |
| | SD24GAIN: 2 | | | | 85 | |
| | SD24GAIN: 4 | | | | 84 | |
| | SD24GAIN: 8 | | | | 86 | |
| | SD24GAIN: 16 | | | | 80 | |
| | SD24GAIN: 32 | | | | 76 | |
| | SD24GAIN: 64 | | | | 67 | |
| | SD24GAIN: 128 | | | | 61 | |

(1) The following voltages were applied to the SD24_B inputs:

$$V_{I,A+}(t) = 0 \text{ V} + V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$$

$$V_{I,A-}(t) = 0 \text{ V} - V_{PP} / 2 \times \sin(2\pi \times f_{IN} \times t)$$

resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

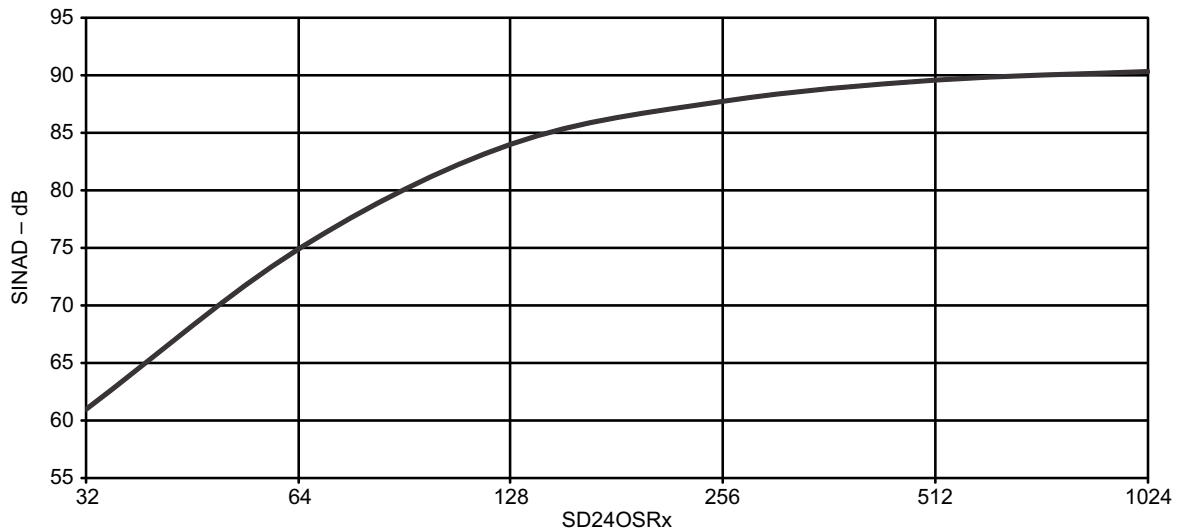


Figure 5-19. SINAD vs OSR
($f_{SD24} = 1$ MHz, $SD24REFS = 1$, $SD24GAIN = 1$)

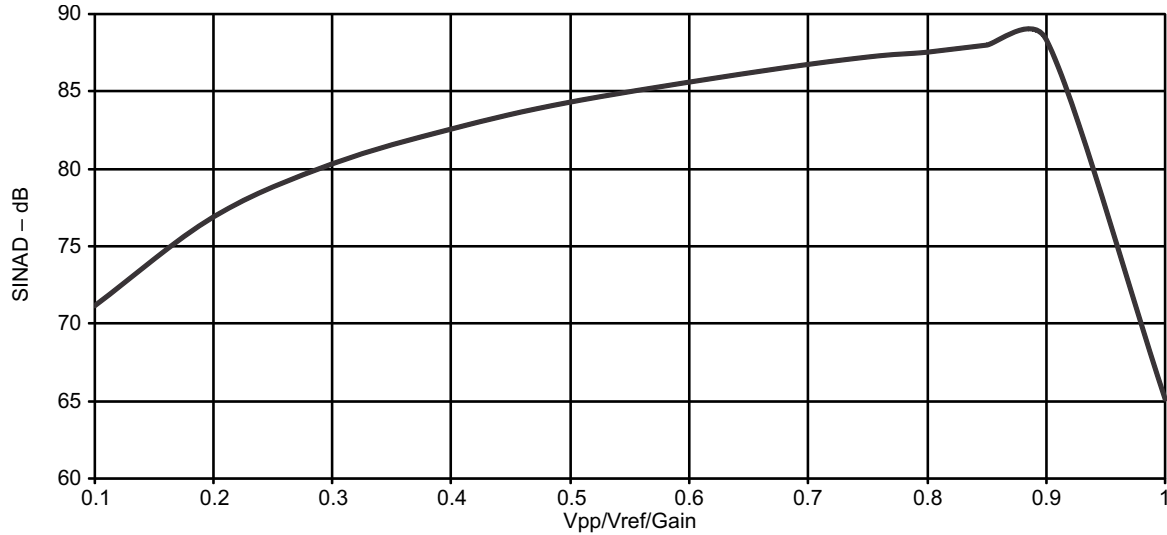


Figure 5-20. SINAD vs V_{PP}

Table 5-42 lists the external reference input requirements of the SD24_B.

Table 5-42. SD24_B External Reference Input

ensure correct input voltage range according to V_{REF}

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP | MAX | UNIT |
|----------------------------|-----------------|----------|-----|------|-----|------|
| $V_{REF(I)}$ Input voltage | SD24REFS = 0 | 3 V | 1.0 | 1.20 | 1.5 | V |
| $I_{REF(I)}$ Input current | SD24REFS = 0 | 3 V | | | 50 | nA |

5.8.11 ADC10_A Module

Table 5-43 lists the input requirements of the ADC.

Table 5-43. 10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---|---|---|-----------------|-----|-----|------------------|------|
| AV _{CC} | Analog supply voltage | AV _{CC} and DV _{CC} are connected together, AV _{SS} and DV _{SS} are connected together, V _(AVSS) = V _(DVSS) = 0 V | | 1.8 | | 3.6 | V |
| V _(Ax) | Analog input voltage range ⁽¹⁾ | All ADC10_A pins | | 0 | | AV _{CC} | V |
| I _{ADC10_A} | Operating supply current into AVCC terminal, REF module and reference buffer off | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00 | 2.2 V | | 70 | 105 | μA |
| | | | 3 V | | 80 | 115 | |
| | Operating supply current into AVCC terminal, REF module on, reference buffer on | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01 | 3 V | | 130 | 185 | |
| | | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VREF = 2.5 V | 3 V | | 108 | 160 | |
| Operating supply current into AVCC terminal, REF module off, reference buffer off | f _{ADC10CLK} = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VREF = 2.5 V | 3 V | | 74 | 105 | | |
| C _I | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad. | 2.2 V | | 3.5 | | pF |
| R _I | Input MUX ON resistance | AV _{CC} > 2 V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 36 | kΩ |
| | | 1.8 V < AV _{CC} < 2 V, 0 V ≤ V _{Ax} ≤ AV _{CC} | | | | 96 | |

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. Two decoupling capacitors, 10 μF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the [MSP430x5xx and MSP430x6xx Family User's Guide](#).

Table 5-44 lists the timing parameters of the ADC.

Table 5-44. 10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|---|-----------------|------|-----------------------------------|-----|------|
| f _{ADC10CLK} | | For specified performance of ADC10_A linearity parameters | 2.2 V, 3 V | 0.45 | 5 | 5.5 | MHz |
| f _{ADC10OSC} | Internal ADC10_A oscillator ⁽¹⁾ | ADC10DIV = 0, f _{ADC10CLK} = f _{ADC10OSC} | 2.2 V, 3 V | 4.4 | 5.0 | 5.6 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode f _{ADC10OSC} = 4 MHz to 5 MHz | 2.2 V, 3 V | 2.4 | | 3.0 | μs |
| | | External f _{ADC10CLK} from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0 | | | 12 × 1 / f _{ADC10CLK} | | |
| t _{ADC10ON} | Turnon settling time of the ADC | See ⁽²⁾ | | | | 100 | ns |
| t _{Sample} | Sampling time | R _S = 1000 Ω, R _I = 96 kΩ, C _I = 3.5 pF ⁽³⁾ | 1.8 V | 3 | | | μs |
| | | R _S = 1000 Ω, R _I = 36 kΩ, C _I = 3.5 pF ⁽³⁾ | 3 V | 1 | | | |

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.

(2) The condition is that the error in a conversion started after t_{ADC10ON} is less than ±0.5 LSB. The reference and input signal are already settled.

(3) Approximately 8 Tau (t) are needed to get an error of less than ±0.5 LSB

Table 5-45 lists the linearity parameters of the ADC.

Table 5-45. 10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------|------------------------------|--|-----------------|-----|------|------|------|
| E _I | Integral linearity error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}) ≤ 1.6 V, C _{VeREF+} = 20 pF | 2.2 V, 3 V | | | ±1.0 | LSB |
| | | 1.6 V < (V _{eREF+} – V _{eREF-}) ≤ V _{AVCC} , C _{VeREF+} = 20 pF | | | | ±1.0 | |
| E _D | Differential linearity error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}), C _{VeREF+} = 20 pF | 2.2 V, 3 V | | | ±1.0 | LSB |
| E _O | Offset error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}), C _{VeREF+} = 20 pF Internal impedance of source R _S < 100 Ω | 2.2 V, 3 V | | | ±1.0 | LSB |
| E _G | Gain error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}), C _{VeREF+} = 20 pF, ADC10SREFX = 11b | 2.2 V, 3 V | | | ±1.0 | LSB |
| E _T | Total unadjusted error | 1.4 V ≤ (V _{eREF+} – V _{eREF-}), C _{VeREF+} = 20 pF, ADC10SREFX = 11b | 2.2 V, 3 V | | ±1.0 | ±2.0 | LSB |

Table 5-46 lists the characteristics of the external reference for the ADC.

Table 5-46. 10-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--|---|--|-----------------|-----|------|------------------|------|
| V _{eREF+} | Positive external reference voltage input | V _{eREF+} > V _{eREF-} ⁽²⁾ | | 1.4 | | AV _{CC} | V |
| V _{eREF-} | Negative external reference voltage input | V _{eREF+} > V _{eREF-} ⁽³⁾ | | 0 | | 1.2 | V |
| (V _{eREF+} – V _{eREF-}) | Differential external reference voltage input | V _{eREF+} > V _{eREF-} ⁽⁴⁾ | | 1.4 | | AV _{CC} | V |
| I _{VeREF+} , I _{VeREF-} | Static input current | 1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x0001, Conversion rate 200 ksps | 2.2 V, 3 V | | ±8.5 | ±26 | μA |
| | | 1.4 V ≤ V _{eREF+} ≤ V _{AVCC} , V _{eREF-} = 0 V, f _{ADC10CLK} = 5 MHz, ADC10SHTX = 0x1000, Conversion rate 20 ksps | 2.2 V, 3 V | | | ±1 | μA |
| C _{VeREF+/-} | Capacitance at VeREF+ or VeREF- terminal | See ⁽⁵⁾ | | 10 | | | μF |

- The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
- The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
- The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
- The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
- Two decoupling capacitors, 10 μF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the [MSP430x5xx and MSP430x6xx Family User's Guide](#).

5.8.12 REF Module

Table 5-47 lists the characteristics of the built-in reference.

Table 5-47. REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|--|---|-----------------|-------|-------|-------|--------|
| V _{REF+} | Positive built-in reference voltage | REFVSEL = {2} for 2.5 V, REFON = 1 | 3 V | 2.47 | 2.51 | 2.55 | V |
| | | REFVSEL = {1} for 2.0 V, REFON = 1 | 3 V | 1.95 | 1.99 | 2.03 | |
| | | REFVSEL = {0} for 1.5 V, REFON = 1 | 2.2 V, 3 V | 1.46 | 1.50 | 1.54 | |
| AV _{CC(min)} | AV _{CC} minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.5 V | | 1.8 | | | V |
| | | REFVSEL = {1} for 2.0 V | | 2.2 | | | |
| | | REFVSEL = {2} for 2.5 V | | 2.7 | | | |
| I _{REF+} | Operating supply current into AV _{CC} terminal ⁽¹⁾ | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V | 3 V | | 23 | 30 | μA |
| | | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V | | | 21 | 27 | |
| | | f _{ADC10CLK} = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V | | | 19 | 25 | |
| TC _{REF+} | Temperature coefficient of built-in reference ⁽²⁾ | REFVSEL = {0, 1, 2}, REFON = 1 | | | 10 | 50 | ppm/°C |
| I _{SENSOR} | Operating supply current into AV _{CC} terminal | REFON = 1, ADC10ON = 1, INCH = 0Ah, T _A = 30°C | 2.2 V | | 145 | 220 | μA |
| | | | 3 V | | 170 | 245 | |
| V _{SENSOR} | See ⁽³⁾ | REFON = 1, ADC10ON = 1, INCH = 0Ah, T _A = 30°C | 2.2 V | | 780 | | mV |
| | | | 3 V | | 780 | | |
| V _{MID} | AV _{CC} divider at channel 11 | ADC10ON = 1, INCH = 0Bh, V _{MID} ≈ 0.5 × V _{AVCC} | 2.2 V | 1.08 | 1.1 | 1.12 | V |
| | | | 3 V | 1.48 | 1.5 | 1.52 | |
| t _{SENSOR(sample)} | Sample time required if channel 10 is selected ⁽⁴⁾ | REFON = 1, ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB | | 30 | | | μs |
| t _{VMID(sample)} | Sample time required if channel 11 is selected ⁽⁵⁾ | ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB | | 1 | | | μs |
| PSRR _{DC} | Power supply rejection ratio (DC) | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1 | | | 120 | 300 | μV/V |
| PSRR _{AC} | Power supply rejection ratio (AC) | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , T _A = 25°C, f = 1 kHz, ΔV _{pp} = 100 mV, REFVSEL = {0, 1, 2}, REFON = 1 | | | 1 | | mV/V |
| t _{SETTLE} | Settling time of reference voltage ⁽⁶⁾ | AV _{CC} = AV _{CC(min)} to AV _{CC(max)} , REFVSEL = {0, 1, 2}, REFON = 0 → 1 | | | 75 | | μs |
| V _{SD24REF} | SD24_B internal reference voltage | SD24REFS = 1 | 3 V | 1.137 | 1.151 | 1.165 | V |
| t _{ON} | SD24_B internal reference turnon time ⁽⁷⁾ | SD24REFS = 0 → 1, C _{REF} = 100 nF | 3 V | | 200 | | μs |

- (1) The internal reference current is supplied by terminal AV_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
- (2) Calculated using the box method: (MAX(−40°C to 85°C) – MIN(−40°C to 85°C)) / MIN(−40°C to 85°C)/(85°C – (−40°C)).
- (3) The temperature sensor offset can be significant. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.
- (4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.
- (5) The on-time t_{VMID(on)} is included in the sampling time t_{VMID(sample)}; no additional on time is needed.
- (6) The condition is that the error in a conversion started after t_{REFON} is ≤ 1 LSB.
- (7) The condition is that SD24_B conversion started after t_{ON} should ensure specified SINAD values for the selected Gain, OSR, and f_{SD24}.

5.8.13 Flash

Table 5-48 lists the characteristics of the flash memory.

Table 5-48. Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | T _J | MIN | TYP | MAX | UNIT |
|---|--|----------------|-----------------|-----------------|-----|--------|
| DV _{CC(PGM/ERASE)} | Program and erase supply voltage | | 1.8 | | 3.6 | V |
| I _{PGM} | Average supply current from DVCC during program | | | 3 | 5 | mA |
| I _{ERASE} | Average supply current from DVCC during erase | | | 6 | 11 | mA |
| I _{MERASE} , I _{BANK} | Average supply current from DVCC during mass erase or bank erase | | | 6 | 11 | mA |
| t _{CPT} | Cumulative program time ⁽¹⁾ | | | | 16 | ms |
| | Program and erase endurance | | 10 ⁴ | 10 ⁵ | | cycles |
| t _{Retention} | Data retention duration | 25°C | 100 | | | years |
| t _{Word} | Word or byte program time ⁽²⁾ | | 64 | | 85 | μs |
| t _{Block, 0} | Block program time for first byte or word ⁽²⁾ | | 49 | | 65 | μs |
| t _{Block, 1–(N–1)} | Block program time for each additional byte or word, except for last byte or word ⁽²⁾ | | 37 | | 49 | μs |
| t _{Block, N} | Block program time for last byte or word ⁽²⁾ | | 55 | | 73 | μs |
| t _{Erase} | Erase time for segment erase, mass erase, and bank erase when available ⁽²⁾ | | 23 | | 32 | ms |
| f _{MCLK,MGR} | MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1) | | 0 | | 1 | MHz |

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming modes: individual word or byte write and block write.

(2) These values are hardwired into the state machine of the flash controller.

5.8.14 Emulation and Debug

Table 5-49 lists the characteristics of the JTAG and Spy-Bi-Wire interface.

Table 5-49. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2.2 V, 3 V | 0 | | 20 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse duration | 2.2 V, 3 V | 0.025 | | 15 | μs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2.2 V, 3 V | | | 1 | μs |
| t _{SBW,Rst} | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | μs |
| f _{TCK} | TCK input frequency for 4-wire JTAG ⁽²⁾ | 2.2 V | 0 | | 5 | MHz |
| | | 3 V | 0 | | 10 | |
| R _{internal} | Internal pulldown resistance on TEST | 2.2 V, 3 V | 45 | 60 | 80 | kΩ |

(1) Tools that access the Spy-Bi-Wire interface must wait for the minimum t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 Overview

The MSP430F673xA and MSP430F673xA microcontrollers feature three high-performance 24-bit sigma-delta ADCs, a 10-bit ADC, four enhanced universal serial communication interfaces (three eUSCI_A modules and one eUSCI_B module), four 16-bit timers, a hardware multiplier, a DMA module, an RTC module with alarm capabilities, a segment LCD driver with integrated contrast control, an auxiliary supply system, and up to 72 I/O pins in the 100-pin devices and 52 I/O pins in the 80-pin devices.

6.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see [图 6-1](#)).

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

| | |
|--------------------------|-----------|
| Program Counter | PC/R0 |
| Stack Pointer | SP/R1 |
| Status Register | SR/CG1/R2 |
| Constant Generator | CG2/R3 |
| General-Purpose Register | R4 |
| General-Purpose Register | R5 |
| General-Purpose Register | R6 |
| General-Purpose Register | R7 |
| General-Purpose Register | R8 |
| General-Purpose Register | R9 |
| General-Purpose Register | R10 |
| General-Purpose Register | R11 |
| General-Purpose Register | R12 |
| General-Purpose Register | R13 |
| General-Purpose Register | R14 |
| General-Purpose Register | R15 |

图 6-1. Integrated CPU Registers

6.3 Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. 表 6-1 lists examples of the three types of instruction formats. 表 6-2 lists the address modes.

表 6-1. Instruction Word Formats

| INSTRUCTION WORD FORMAT | EXAMPLE | OPERATION |
|---|-----------|---|
| Dual operands, source-destination | ADD R4,R5 | $R4 + R5 \rightarrow R5$ |
| Single operands, destination only | CALL R8 | $PC \rightarrow (TOS), R8 \rightarrow PC$ |
| Relative jump, conditional or unconditional | JNE | Jump-on-equal bit = 0 |

表 6-2. Address Mode Descriptions

| ADDRESS MODE | S ⁽¹⁾ | D ⁽¹⁾ | SYNTAX | EXAMPLE | OPERATION |
|------------------------|------------------|------------------|--------------------|------------------|---|
| Register | + | + | MOV Rs,Rd | MOV R10,R11 | $R10 \rightarrow R11$ |
| Indexed | + | + | MOV X(Rn),Y(Rm) | MOV 2(R5),6(R6) | $M(2+R5) \rightarrow M(6+R6)$ |
| Symbolic (PC relative) | + | + | MOV EDE,TONI | | $M(EDE) \rightarrow M(TONI)$ |
| Absolute | + | + | MOV & MEM, & TCDAT | | $M(MEM) \rightarrow M(TCDAT)$ |
| Indirect | + | | MOV @Rn,Y(Rm) | MOV @R10,Tab(R6) | $M(R10) \rightarrow M(Tab+R6)$ |
| Indirect autoincrement | + | | MOV @Rn+,Rm | MOV @R10+,R11 | $M(R10) \rightarrow R11$ $R10 + 2 \rightarrow R10$ |
| Immediate | + | | MOV #X,TONI | MOV #45,TONI | $\#45 \rightarrow M(TONI)$ |

(1) S = source, D = destination

6.4 Operating Modes

The MSP430F673xA and MSP430F673xA microcontrollers have one active mode and seven software-selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

Software can configure the following operating modes:

- Active mode (AM)
 - All clocks are active
- Low-power mode 0 (LPM0)
 - CPU is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
 - FLL loop control remains active
- Low-power mode 1 (LPM1)
 - CPU is disabled
 - FLL loop control is disabled
 - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
 - CPU is disabled
 - MCLK and FLL loop control and DCOCLK are disabled
 - DC generator of the DCO remains enabled
 - ACLK remains active
- Low-power mode 3 (LPM3)
 - CPU is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - ACLK remains active
- Low-power mode 4 (LPM4)
 - CPU is disabled
 - ACLK is disabled
 - MCLK, FLL loop control, and DCOCLK are disabled
 - DC generator of the DCO is disabled
 - Crystal oscillator is stopped
 - Complete data retention
- Low-power mode 3.5 (LPM3.5)
 - Internal regulator disabled
 - No RAM retention, Backup RAM retained
 - I/O pad state retention
 - RTC clocked by low-frequency oscillator
 - Wake-up input from $\overline{\text{RST/NMI}}$, RTC_C events, Ports P1 and P2
- Low-power mode 4.5 (LPM4.5)
 - Internal regulator disabled
 - No RAM retention, Backup RAM retained
 - RTC is disabled
 - I/O pad state retention
 - Wake-up input from $\overline{\text{RST/NMI}}$, Ports P1 and P2

6.5 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h (see [Table 6-3](#)). The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

表 6-3. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|--|------------------|--------------|-------------|
| System Reset Power-Up External Reset Watchdog Time-out, Key Violation Flash Memory Key Violation | WDTIFG, KEYV (SYSRSTIV) ^{(1) (2)} | Reset | 0FFFEh | 63, highest |
| System NMI PMM Vacant Memory Access JTAG Mailbox | SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) ^{(1) (3)} | (Non)maskable | 0FFFCh | 62 |
| User NMI NMI Oscillator Fault Flash Memory Access Violation Supply Switch | NMIIFG, OFIFG, ACCVIFG, AUXSWNMIFG (SYSUNIV) ^{(1) (3)} | (Non)maskable | 0FFFAh | 61 |
| Watchdog Timer_A Interval Timer Mode | WDTIFG | Maskable | 0FFF8h | 60 |
| eUSCI_A0 Receive or Transmit | UCA0RXIFG, UCA0TXIFG (UCA0IV) ^{(1) (4)} | Maskable | 0FFF6h | 59 |
| eUSCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG (UCB0IV) ^{(1) (4)} | Maskable | 0FFF4h | 58 |
| ADC10_A | ADC10IFG0, ADC10INIFG, ADC10LOIFG, ADC10HIIFG, ADC10TOVIFG, ADC10OVIFG (ADC10IV) ^{(1) (4)} | Maskable | 0FFF2h | 57 |
| SD24_B | SD24_B Interrupt Flags (SD24IV) ^{(1) (4)} | Maskable | 0FFF0h | 56 |
| Timer TA0 | TA0CCR0 CCIFG0 ⁽⁴⁾ | Maskable | 0FFEEh | 55 |
| Timer TA0 | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV) ^{(1) (4)} | Maskable | 0FFECCh | 54 |
| eUSCI_A1 Receive or Transmit | UCA1RXIFG, UCA1TXIFG (UCA1IV) ^{(1) (4)} | Maskable | 0FFEAh | 53 |
| eUSCI_A2 Receive or Transmit | UCA2RXIFG, UCA2TXIFG (UCA2IV) ^{(1) (4)} | Maskable | 0FFE8h | 52 |
| Auxiliary Supplies | Auxiliary Supplies Interrupt Flags (AUXIV) ^{(1) (4)} | Maskable | 0FFE6h | 51 |
| DMA | DMA0IFG, DMA1IFG, DMA2IFG (DMAIV) ^{(1) (4)} | Maskable | 0FFE4h | 50 |
| Timer TA1 | TA1CCR0 CCIFG0 ⁽⁴⁾ | Maskable | 0FFE2h | 49 |
| Timer TA1 | TA1CCR1 CCIFG1, TA1IFG (TA1IV) ^{(1) (4)} | Maskable | 0FFE0h | 48 |
| I/O Port P1 | P1IFG.0 to P1IFG.7 (P1IV) ^{(1) (4)} | Maskable | 0FFDEh | 47 |
| Timer TA2 | TA2CCR0 CCIFG0 ⁽⁴⁾ | Maskable | 0FFDCCh | 46 |
| Timer TA2 | TA2CCR1 CCIFG1, TA2IFG (TA2IV) ^{(1) (4)} | Maskable | 0FFDAh | 45 |
| I/O Port P2 | P2IFG.0 to P2IFG.7 (P2IV) ^{(1) (4)} | Maskable | 0FFD8h | 44 |
| Timer TA3 | TA3CCR0 CCIFG0 ⁽⁴⁾ | Maskable | 0FFD6h | 43 |
| Timer TA3 | TA3CCR1 CCIFG1, TA3IFG (TA3IV) ^{(1) (4)} | Maskable | 0FFD4h | 42 |
| LCD_C | LCD_C Interrupt Flags (LCDCIV) ^{(1) (4)} | Maskable | 0FFD2h | 41 |
| RTC_C | RTCOIFG, RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV) ^{(1) (4)} | Maskable | 0FFD0h | 40 |

(1) Multiple source flags

(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.

(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.

(4) Interrupt flags are located in the module.

表 6-3. Interrupt Sources, Flags, and Vectors (continued)

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|------------------|-------------------------|------------------|--------------|-----------|
| Reserved | Reserved ⁽⁵⁾ | | 0FFCEh | 39 |
| | | | ⋮ | ⋮ |
| | | | 0FF80h | 0, lowest |

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, TI recommends reserving these locations.

6.6 Bootloader (BSL)

The BSL lets users program the flash memory or RAM using various serial interfaces. Access to the device memory through the BSL is protected by a user-defined password. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ and $\text{TEST}/\text{SBWTCK}$ pins. For complete description of the features of the BSL and its implementation, see the [MSP430™ Flash Device Bootloader \(BSL\) User's Guide](#). 表 6-4 lists the BSL pin requirements.

表 6-4. UART BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|---|-----------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | Entry sequence signal |
| $\text{TEST}/\text{SBWTCK}$ | Entry sequence signal |
| P3.0 | Data transmit |
| P3.1 | Data receive |
| DVCC | Power supply |
| DVSS | Ground supply |

6.7 JTAG Operation

6.7.1 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The $\text{TEST}/\text{SBWTCK}$ pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ is required to interface with MSP430 development tools and device programmers. 表 6-5 lists the JTAG pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#) and [MSP430 Programming With the JTAG Interface](#).

表 6-5. JTAG Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|---|-----------|----------------------------|
| PJ.3/ACLK/TCK | IN | JTAG clock input |
| PJ.2/ADC10CLK/TMS | IN | JTAG state control |
| PJ.1/MCLK/TDI/TCLK | IN | JTAG data input/TCLK input |
| PJ.0/SMCLK/TDO | OUT | JTAG data output |
| $\text{TEST}/\text{SBWTCK}$ | IN | Enable JTAG pins |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | IN | External reset |
| DVCC | | Power supply |
| DVSS | | Ground supply |

6.7.2 Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 6-6 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the [MSP430 Hardware Tools User's Guide](#) and [MSP430 Programming With the JTAG Interface](#).

表 6-6. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | FUNCTION |
|-------------------------------------|-----------|-------------------------------|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| $\overline{\text{RST}}$ /NMI/SBWDIO | IN, OUT | Spy-Bi-Wire data input/output |
| DVCC | | Power supply |
| DVSS | | Ground supply |

6.8 Flash Memory

The flash memory can be programmed through the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

6.9 RAM

The RAM is made up of n sectors. Each sector can be completely powered down to save leakage; however, all data are lost. Features of the RAM include:

- RAM has n sectors of 2 kbytes each.
- Each sector 0 to n can be completely disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

6.10 Backup RAM

The backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5. This backup RAM is part of the Backup subsystem that operates on dedicated power supply AUXVCC3. 8 bytes of backup RAM are available in this device. The backup RAM can be word-wise accessed through the registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3. The backup RAM registers cannot be accessed by the CPU when the high-side SVS is disabled by software.

6.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. The peripherals can be handled using all instructions. For complete module descriptions, see the [MSP430x5xx and MSP430x6xx Family User's Guide](#).

6.11.1 Oscillator and System Clock

The Unified Clock System (UCS) module includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), and an integrated internal digitally controlled oscillator (DCO). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency-locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turn-on clock source and stabilizes in 3 μ s (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, the internal low-frequency oscillator (VLO), or the trimmed low-frequency oscillator (REFO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

6.11.2 Power-Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM are available on the primary supply and the core supply.

6.11.3 Auxiliary Supply System

The auxiliary supply system provides the possibility to operate the device from auxiliary supplies when the primary supply fails. There are two auxiliary supplies (AUXVCC1 and AUXVCC2) are supported. This module supports automatic and manual switching from primary supply to auxiliary supplies while maintaining full functionality. It allows threshold based monitoring of primary and auxiliary supplies. The device can be started from primary supply or AUXVCC1, whichever is higher. Auxiliary supply system enables internal monitoring of voltage levels on primary and auxiliary supplies using ADC10_A. Also this module implements simple charger for backup supplies.

6.11.4 Backup Subsystem

The Backup subsystem operates on a dedicated power supply AUXVCC3. This subsystem includes low-frequency oscillator (XT1), RTC module, and backup RAM. The functionality of the Backup subsystem is retained during LPM3.5. The Backup subsystem module registers cannot be accessed by CPU when the high-side SVS is disabled by the user. It is necessary to keep the high-side SVS enabled with SVSHMD = 1 and SVSMHACE = 0 to turn off the low-frequency oscillator (XT1) in LPM4.

6.11.5 Digital I/O

Up to nine 8-bit I/O ports are implemented. For 100-pin options, Ports P1 to P8 are complete, and P9 is reduced to 4-bit I/O. For 80-pin options, Ports P1 to P6 are complete, and P7 to P9 are completely removed. Port PJ contains four individual I/O pins, common to all devices. All I/O bits are individually programmable.

- Any combination of input, output and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Programmable drive strength on all ports.
- Edge-selectable interrupt and LPM3.5, LPM4.5 wake-up input capability available for all bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P9) or word-wise in pairs (PA through PE).

6.11.6 Port Mapping Controller

The port mapping controller allows flexible and reconfigurable mapping of digital functions to P1, P2, and P3 (see 表 6-7). 表 6-8 lists the default settings for all pins that support port mapping.

表 6-7. Port Mapping Mnemonics and Functions

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|-------|-----------------|--|------------------------------|
| 0 | PM_NONE | None | DVSS |
| 1 | PM_UCA0RXD | eUSCI_A0 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA0SOMI | eUSCI_A0 SPI slave out master in (direction controlled by eUSCI) | |
| 2 | PM_UCA0TXD | eUSCI_A0 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA0SIMO | eUSCI_A0 SPI slave in master out (direction controlled by eUSCI) | |
| 3 | PM_UCA0CLK | eUSCI_A0 clock input/output (direction controlled by eUSCI) | |
| 4 | PM_UCA0STE | eUSCI_A0 SPI slave transmit enable (direction controlled by eUSCI) | |
| 5 | PM_UCA1RXD | eUSCI_A1 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA1SOMI | eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |
| 6 | PM_UCA1TXD | eUSCI_A1 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA1SIMO | eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| 7 | PM_UCA1CLK | eUSCI_A1 clock input/output (direction controlled by eUSCI) | |
| 8 | PM_UCA1STE | eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI) | |
| 9 | PM_UCA2RXD | eUSCI_A2 UART RXD (direction controlled by eUSCI – Input) | |
| | PM_UCA2SOMI | eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| 10 | PM_UCA2TXD | eUSCI_A2 UART TXD (direction controlled by eUSCI – Output) | |
| | PM_UCA2SIMO | eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| 11 | PM_UCA2CLK | eUSCI_A2 clock input/output (direction controlled by eUSCI) | |
| 12 | PM_UCA2STE | eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI) | |
| 13 | PM_UCB0SIMO | eUSCI_B0 SPI slave in master out (direction controlled by eUSCI) | |
| | PM_UCB0SDA | eUSCI_B0 I2C data (open drain and direction controlled by eUSCI) | |
| 14 | PM_UCB0SOMI | eUSCI_B0 SPI slave out master in (direction controlled by eUSCI) | |
| | PM_UCB0SCL | eUSCI_B0 I2C clock (open drain and direction controlled by eUSCI) | |
| 15 | PM_UCB0CLK | eUSCI_B0 clock input/output (direction controlled by eUSCI) | |
| 16 | PM_UCB0STE | eUSCI_B0 SPI slave transmit enable (direction controlled by eUSCI) | |
| 17 | PM_TA0.0 | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| 18 | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| 19 | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| 20 | PM_TA1.0 | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| 21 | PM_TA1.1 | TA1 CCR1 capture input CCI1A | TA1 CCR1 compare output Out1 |

表 6-7. Port Mapping Mnemonics and Functions (continued)

| VALUE | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|--------------------------|-----------------|--|------------------------------|
| 22 | PM_TA2.0 | TA2 CCR0 capture input CCI0A | TA2 CCR0 compare output Out0 |
| 23 | PM_TA2.1 | TA2 CCR1 capture input CCI1A | TA2 CCR1 compare output Out1 |
| 24 | PM_TA3.0 | TA3 CCR0 capture input CCI0A | TA3 CCR0 compare output Out0 |
| 25 | PM_TA3.1 | TA3 CCR1 capture input CCI1A | TA3 CCR1 compare output Out1 |
| 26 | PM_TACLK | Timer_A clock input to TA0, TA1, TA2, TA3 | None |
| | PM_RTCCLK | None | RTC_C clock output |
| 27 | PM_SDCLK | SD24_B bit stream clock input/output (direction controlled by SD24_B) | |
| 28 | PM_SD0DIO | SD24_B converter 0 bit stream data input/output (direction controlled by SD24_B) | |
| 29 | PM_SD1DIO | SD24_B converter 1 bit stream data input/output (direction controlled by SD24_B) | |
| 30 | PM_SD2DIO | SD24_B converter 2 bit stream data input/output (direction controlled by SD24_B) | |
| 31 (0FFh) ⁽¹⁾ | PM_ANALOG | Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals. | |

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide, and the upper bits are ignored, which results in a read value of 31.

表 6-8. Default Mapping

| PIN NAME | | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|--|--|----------------------------|--|------------------------------|
| PZ | PN | | | |
| P1.0/PM_TA0.0/ VeREF-/A2 | P1.0/PM_TA0.0/ VeREF-/A2 | PM_TA0.0 | TA0 CCR0 capture input CCI0A | TA0 CCR0 compare output Out0 |
| P1.1/PM_TA0.1/ VeREF+/A1 | P1.1/PM_TA0.1/ VeREF+/A1 | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0 | P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0 | PM_UCA0RXD, PM_UCA0SOMI | eUSCI_A0 UART RXD (direction controlled by eUSCI – input), eUSCI_A0 SPI slave out master in (direction controlled by eUSCI) | |
| P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03 | P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03 | PM_UCA0TXD, PM_UCA0SIMO | eUSCI_A0 UART TXD (direction controlled by eUSCI – output), eUSCI_A0 SPI slave in master out (direction controlled by eUSCI) | |
| P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13 | P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13 | PM_UCA1RXD, PM_UCA1SOMI | eUSCI_A1 UART RXD (direction controlled by eUSCI – input), eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |
| P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23 | P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23 | PM_UCA1TXD, PM_UCA1SIMO | eUSCI_A1 UART TXD (direction controlled by eUSCI – output), eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| P1.6/PM_UCA0CLK/ COM4 | P1.6/PM_UCA0CLK/ COM4 | PM_UCA0CLK | eUSCI_A0 clock input/output (direction controlled by eUSCI) | |
| P1.7/PM_UCB0CLK/ COM5 | P1.7/PM_UCB0CLK/ COM5 | PM_UCB0CLK | eUSCI_B0 clock input/output (direction controlled by eUSCI) | |
| P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6 | P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6/S39 | PM_UCB0SOMI, PM_UCB0SCL | eUSCI_B0 SPI slave out master in (direction controlled by eUSCI), eUSCI_B0 I2C clock (open drain and direction controlled by eUSCI) | |
| P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7 | P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7/S38 | PM_UCB0SIMO, PM_UCB0SDA | eUSCI_B0 SPI slave in master out (direction controlled by eUSCI), eUSCI_B0 I2C data (open drain and direction controlled by eUSCI) | |
| P2.2/PM_UCA2RXD/ PM_UCA2SOMI | P2.2/PM_UCA2RXD/ PM_UCA2SOMI/S37 | PM_UCA2RXD, PM_UCA2SOMI | eUSCI_A2 UART RXD (direction controlled by eUSCI – input), eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| P2.3/PM_UCA2TXD/ PM_UCA2SIMO | P2.3/PM_UCA2TXD/ PM_UCA2SIMO/S36 | PM_UCA2TXD, PM_UCA2SIMO | eUSCI_A2 UART TXD (direction controlled by eUSCI – output), eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| P2.4/PM_UCA1CLK | P2.4/PM_UCA1CLK/S35 | PM_UCA1CLK | eUSCI_A1 clock input/output (direction controlled by eUSCI) | |

表 6-8. Default Mapping (continued)

| PIN NAME | | PxMAPy MNEMONIC | INPUT PIN FUNCTION | OUTPUT PIN FUNCTION |
|----------------------------|--------------------------------|-----------------------|---|------------------------------|
| PZ | PN | | | |
| P2.5/PM_UCA2CLK | P2.5/PM_UCA2CLK/S34 | PM_UCA2CLK | eUSCI_A2 clock input/output (direction controlled by eUSCI) | |
| P2.6/PM_TA1.0 | P2.6/PM_TA1.0/S33 | PM_TA1.0 | TA1 CCR0 capture input CCI0A | TA1 CCR0 compare output Out0 |
| P2.7/PM_TA1.1 | P2.7/PM_TA1.1/S32 | PM_TA1.1 | TA1 CCR1 capture input CCI1A | TA1 CCR1 compare output Out1 |
| P3.0/PM_TA2.0 | P3.0/PM_TA2.0/S31 | PM_TA2.0 | TA2 CCR0 capture input CCI0A | TA2 CCR0 compare output Out0 |
| P3.1/PM_TA2.1 | P3.1/PM_TA2.1/S30 | PM_TA2.1 | TA2 CCR1 capture input CCI1A | TA2 CCR1 compare output Out1 |
| P3.2/PM_TACLK/ PM_RTCLK | P3.2/PM_TACLK/ PM_RTCLK/S29 | PM_TACLK, PM_RTCLK | Timer_A clock input to TA0, TA1, TA2, TA3 | RTC_C clock output |
| P3.3/PM_TA0.2 | P3.3/PM_TA0.2/S28 | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| P3.4/PM_SDCLK/S39 | P3.4/PM_SDCLK/S27 | PM_SDCLK | SD24_B bit stream clock input/output (direction controlled by SD24_B) | |
| P3.5/PM_SD0DIO/S38 | P3.5/PM_SD0DIO/S26 | PM_SD0DIO | SD24_B converter 0 bit stream data input/output (direction controlled by SD24_B) | |
| P3.6/PM_SD1DIO/S37 | P3.6/PM_SD1DIO/S25 | PM_SD1DIO | SD24_B converter 1 bit stream data input/output (direction controlled by SD24_B) | |
| P3.7/PM_SD2DIO/S36 | P3.7/PM_SD2DIO/S24 | PM_SD2DIO | SD24_B converter 2 bit stream data input/output (direction controlled by SD24_B) | |

6.11.7 System Module (SYS)

The SYS module handles many of the system functions within the device. These include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators (see 表 6-9), bootloader entry mechanisms, and configuration management (device descriptors). It also includes a data exchange mechanism through JTAG called a JTAG mailbox that can be used in the application.

表 6-9. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---------------------------|--------------------------------|--------------|--------|----------|
| SYSRSTIV, System Reset | No interrupt pending | 019Eh | 00h | |
| | Brownout (BOR) | | 02h | Highest |
| | RST/NMI (POR) | | 04h | |
| | DoBOR (BOR) | | 06h | |
| | Wakeup from LPMx.5 (BOR) | | 08h | |
| | Security violation (BOR) | | 0Ah | |
| | SVSL (POR) | | 0Ch | |
| | SVSH (POR) | | 0Eh | |
| | SVML_OVP (POR) | | 10h | |
| | SVMH_OVP (POR) | | 12h | |
| | DoPOR (POR) | | 14h | |
| | WDT time-out (PUC) | | 16h | |
| | WDT key violation (PUC) | | 18h | |
| | KEYV flash key violation (PUC) | | 1Ah | |
| | Reserved | | 1Ch | |
| | Peripheral area fetch (PUC) | | 1Eh | |
| | PMM key violation (PUC) | | 20h | |
| Reserved | 22h to 3Eh | Lowest | | |

表 6-9. System Module Interrupt Vector Registers (continued)

| INTERRUPT VECTOR REGISTER | INTERRUPT EVENT | WORD ADDRESS | OFFSET | PRIORITY |
|---------------------------|----------------------|--------------|----------------------|----------|
| SYSSNIV, System NMI | No interrupt pending | 019Ch | 00h | |
| | SVMLIFG | | 02h | Highest |
| | SVMHIFG | | 04h | |
| | DLYLIFG | | 06h | |
| | DLYHIFG | | 08h | |
| | VMAIFG | | 0Ah | |
| | JMBINIFG | | 0Ch | |
| | JMBOUTIFG | | 0Eh | |
| | VLRIFG | | 10h | |
| | VLRHIFG | | 12h | |
| | Reserved | | 14h to 1Eh | Lowest |
| | SYSUNIV, User NMI | | No interrupt pending | 019Ah |
| NMIIFG | | 02h | Highest | |
| OFIFG | | 04h | | |
| ACCVIFG | | 06h | | |
| AUXSWNMIFG | | 08h | | |
| Reserved | | 0Ah to 1Eh | Lowest | |

6.11.8 Watchdog Timer (WDT_A)

The primary function of the WDT_A module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the timer can be configured as an interval timer and can generate interrupts at selected time intervals.

6.11.9 DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral. 表 6-10 lists the available DMA triggers.

表 6-10. DMA Trigger Assignments⁽¹⁾

| TRIGGER | CHANNEL | | |
|---------|---------------|---|---|
| | 0 | 1 | 2 |
| 0 | DMAREQ | | |
| 1 | TA0CCR0 CCIFG | | |
| 2 | TA0CCR2 CCIFG | | |
| 3 | TA1CCR0 CCIFG | | |
| 4 | Reserved | | |
| 5 | TA2CCR0 CCIFG | | |
| 6 | Reserved | | |
| 7 | TA3CCR0 CCIFG | | |
| 8 | Reserved | | |
| 9 | Reserved | | |

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

表 6-10. DMA Trigger Assignments⁽¹⁾ (continued)

| TRIGGER | CHANNEL | | |
|---------|------------|---------|---------|
| | 0 | 1 | 2 |
| 10 | Reserved | | |
| 11 | Reserved | | |
| 12 | Reserved | | |
| 13 | SD24IFG | | |
| 14 | Reserved | | |
| 15 | Reserved | | |
| 16 | UCA0RXIFG | | |
| 17 | UCA0TXIFG | | |
| 18 | UCA1RXIFG | | |
| 19 | UCA1TXIFG | | |
| 20 | UCA2RXIFG | | |
| 21 | UCA2TXIFG | | |
| 22 | UCB0RXIFG0 | | |
| 23 | UCB0TXIFG0 | | |
| 24 | ADC10IFG0 | | |
| 25 | Reserved | | |
| 26 | Reserved | | |
| 27 | Reserved | | |
| 28 | Reserved | | |
| 29 | MPY ready | | |
| 30 | DMA2IFG | DMA0IFG | DMA1IFG |
| 31 | Reserved | | |

6.11.10 CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

6.11.11 Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-, 24-, 16-, and 8-bit operands. The module supports signed and unsigned multiplication as well as signed and unsigned multiply-and-accumulate operations.

6.11.12 Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3- or 4-pin) and I²C, and asynchronous communication protocols such as UART, enhanced UART with automatic baud-rate detection, and IrDA.

The eUSCI_An module supports for SPI (3- or 4-pin), UART, enhanced UART, or IrDA.

The eUSCI_Bn module supports for SPI (3- or 4-pin) or I²C.

Three eUSCI_A and one eUSCI_B module are implemented.

6.11.13 ADC10_A

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion results buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

6.11.14 SD24_B

The SD24_B module integrates up to three independent 24-bit sigma-delta analog-to-digital converters. Each converter is designed with a fully differential analog input pair and programmable gain amplifier input stage. The converters are based on second-order over-sampling sigma-delta modulators and digital decimation filters. The decimation filters are comb-type filters with selectable oversampling ratios of up to 1024.

6.11.15 TA0

TA0 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing (see [表 6-11](#)). TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-11. TA0 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|-------------------|--------------|----------------------|----------------------|
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA0.0 | CCI0A | CCR0 | TA0 | PM_TA0.0 |
| DVSS | CCI0B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA0.1 | CCI1A | CCR1 | TA1 | PM_TA0.1 |
| ACLK (internal) | CCI1B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA0.2 | CCI2A | CCR2 | TA2 | PM_TA0.2 |
| DVSS | CCI2B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

6.11.16 TA1

TA1 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-12). TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-12. TA1 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|-------------------|--------------|----------------------|----------------------|
| | | | | PZ |
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | CCR0 | TA0 | PM_TA1.0 |
| PM_TA1.0 | CC10A | | | |
| DVSS | CC10B | | | |
| DVSS | GND | | | |
| DVCC | VCC | CCR1 | TA1 | PM_TA1.1 |
| PM_TA1.1 | CC11A | | | |
| ACLK (internal) | CC11B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | |

6.11.17 TA2

TA2 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA2 can support multiple capture/compares, PWM outputs, and interval timing (see 表 6-13). TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-13. TA2 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|-------------------|--------------|----------------------|-------------------------------------|
| | | | | PZ |
| PM_TACLK | TACLK | Timer | NA | NA |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | CCR0 | TA0 | PM_TA2.0 |
| PM_TA2.0 | CC10A | | | |
| DVSS | CC10B | | | |
| DVSS | GND | | | |
| DVCC | VCC | CCR1 | TA1 | PM_TA2.1 |
| PM_TA2.1 | CC11A | | | |
| ACLK (internal) | CC11B | | | |
| DVSS | GND | | | |
| DVCC | VCC | | | SD24_B (internal) SD24SCSx = {2} |

6.11.18 TA3

TA3 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA3 can support multiple capture/comparers, PWM outputs, and interval timing (see 表 6-14). TA3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

表 6-14. TA3 Signal Connections

| DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|-------------------|--------------|----------------------|---------------------------------------|
| PM_TACLK | TACLK | Timer | NA | |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| PM_TACLK | INCLK | | | |
| PM_TA3.0 | CCIOA | CCR0 | TA0 | PM_TA3.0 |
| DVSS | CCIOB | | | ADC10_A (internal) ADC10SHSx = {2} |
| DVSS | GND | | | |
| DVCC | VCC | | | |
| PM_TA3.1 | CC1A | CCR1 | TA1 | PM_TA3.1 |
| ACLK (internal) | CC1B | | | SD24_B (internal) SD24SCSx = {3} |
| DVSS | GND | | | |
| DVCC | VCC | | | |

6.11.19 SD24_B Triggers

表 6-15 lists the input trigger connections to SD24_B converters from Timer_A modules and the output trigger pulse connection from SD24_B to ADC10_A.

表 6-15. SD24_B Input/Output Trigger Connections

| DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|---------------------|--------------------------|--------------|----------------------|---------------------------------------|
| TA0.1 (internal) | SD24_B SD24SCSx = {1} | SD24_B | Trigger Pulse | ADC10_A (internal) ADC10SHSx = {3} |
| TA2.1 (internal) | SD24_B SD24SCSx = {2} | | | |
| TA3.1 (internal) | SD24_B SD24SCSx = {3} | | | |

6.11.20 ADC10_A Triggers

表 6-16 lists the input trigger connections to ADC10_A from Timer_A modules and SD24_B.

表 6-16. ADC10_A Input Trigger Connections

| DEVICE INPUT SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK |
|---------------------|----------------------------|--------------|
| TA0.1 (internal) | ADC10_A ADC10SHSx = {1} | ADC10_A |
| TA3.0 (internal) | ADC10_A ADC10SHSx = {2} | |

6.11.21 Real-Time Clock (RTC_C)

The RTC_C module can be configured for real-time clock or calendar mode that provides seconds, hours, day of week, day of month, month, and year. The RTC_C control and configuration registers are password-protected to ensure clock integrity against runaway code. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset calibration, and temperature compensation. The RTC_C on this device operates on dedicated AUXVCC3 supply and supports operation in LPM3.5.

6.11.22 Reference (REF) Module Voltage Reference

The REF is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device. These include the ADC10_A, LCD_C, and SD24_B modules.

6.11.23 LCD_C

The LCD_C driver generates the segment and common signals required to drive a segment liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, 4-mux, up to 8-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage, and thus contrast, by software. The module also provides an automatic blinking capability for individual segments in static, 2-mux, 3-mux, and 4-mux modes.

6.11.24 Embedded Emulation Module (EEM) (S Version)

The EEM supports real-time in-system debugging. The S version of the EEM has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.12 Input/Output Diagrams

6.12.1 Port P1 (P1.0 and P1.1) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ and MSP430F67xxAIPN)

图 6-2 shows the port diagram. 表 6-17 summarizes the selection of the pin functions.

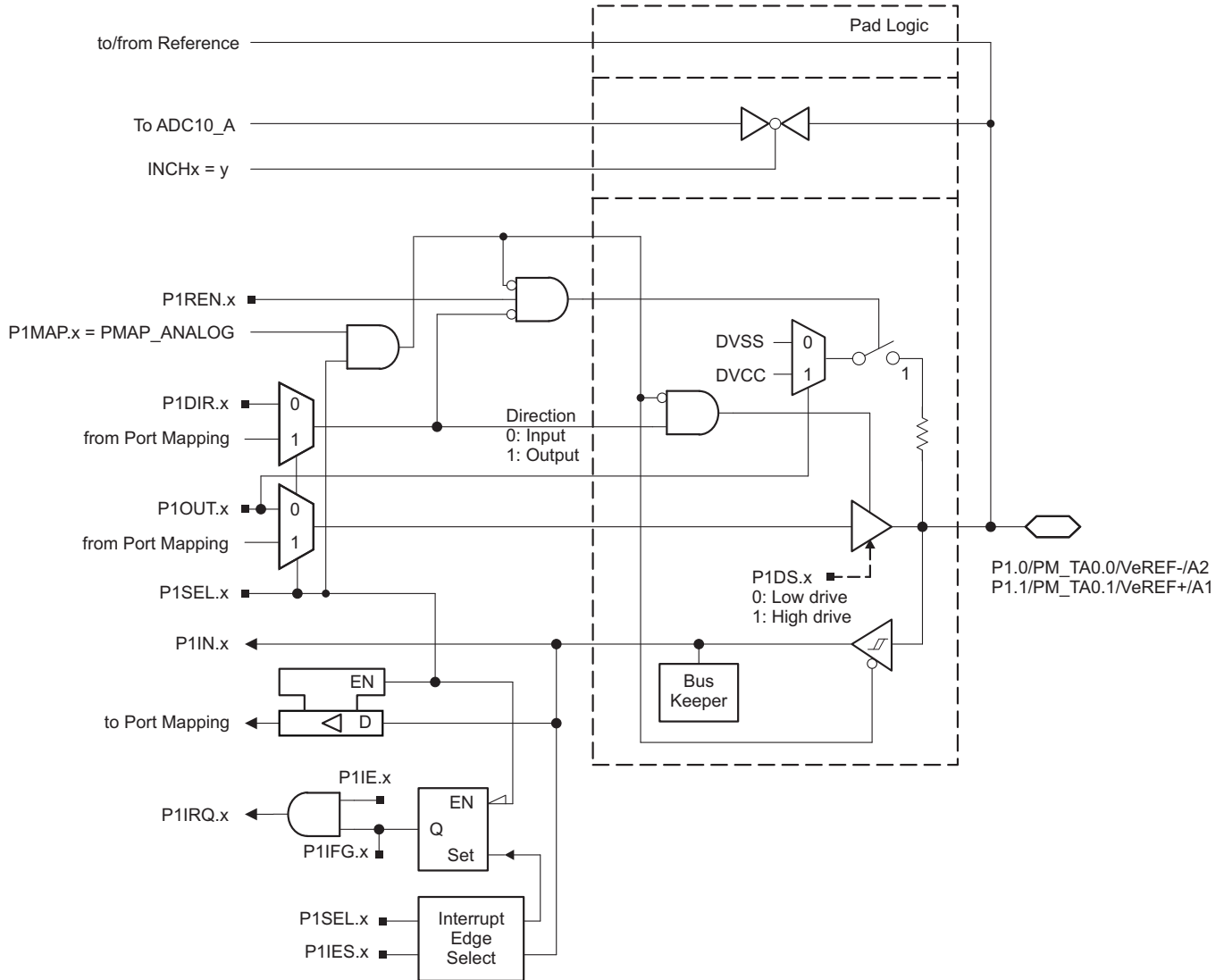


图 6-2. Port P1 (P1.0 and P1.1) Diagram (MSP430F67xxAIPZ and MSP430F67xxAIPN)

表 6-17. Port P1 (P1.0 and P1.1) Pin Functions (MSP430F67xxAIPZ and MSP430F67xxAIPN)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------------------|---|--------------------------|--|---------|---------|
| | | | P1DIR.x | P1SEL.x | P1MAPx |
| P1.0/PM_TA0.0/ VeREF-/A2 | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA0.CCI0A | 0 | 1 | default |
| | | TA0.TA0 | 1 | 1 | default |
| | | VeREF-/A2 ⁽²⁾ | X | 1 | = 31 |
| P1.1/PM_TA0.1/ VeREF+/A1 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA0.CCI1A | 0 | 1 | default |
| | | TA0.TA1 | 1 | 1 | default |
| | | VeREF+/A1 ⁽²⁾ | X | 1 | = 31 |

(1) X = Don't care

(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.

6.12.2 Port P1 (P1.2) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ and MSP430F67xxAIPN)

图 6-3 shows the port diagram. 表 6-18 summarizes the selection of the pin functions.

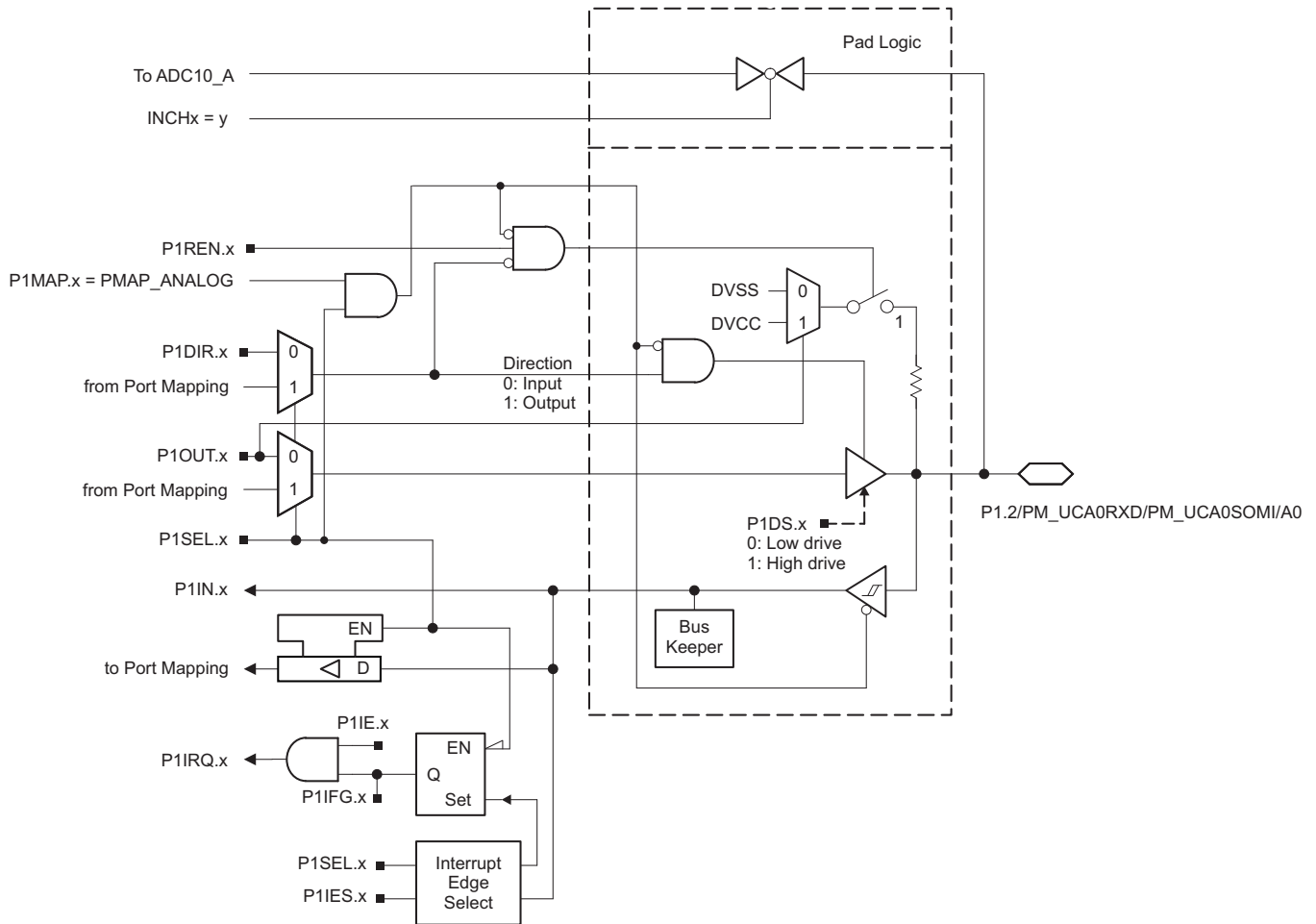


图 6-3. Port P1 (P1.2) Diagram (MSP430F67xxAIPZ and MSP430F67xxAIPN)

表 6-18. Port P1 (P1.2) Pin Functions (MSP430F67xxAIPZ and MSP430F67xxAIPN)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|------------------------------------|---|-------------------|--|---------|---------|
| | | | P1DIR.x | P1SEL.x | P1MAPx |
| P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA0RXD/UCA0SOMI | X | 1 | default |
| | | A0 ⁽²⁾ | X | 1 | = 31 |

(1) X = Don't care

(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.

6.12.3 Port P1 (P1.3 to P1.5) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ and MSP430F67xxAIPN)

图 6-4 shows the port diagram. 表 6-19 summarizes the selection of the pin functions.

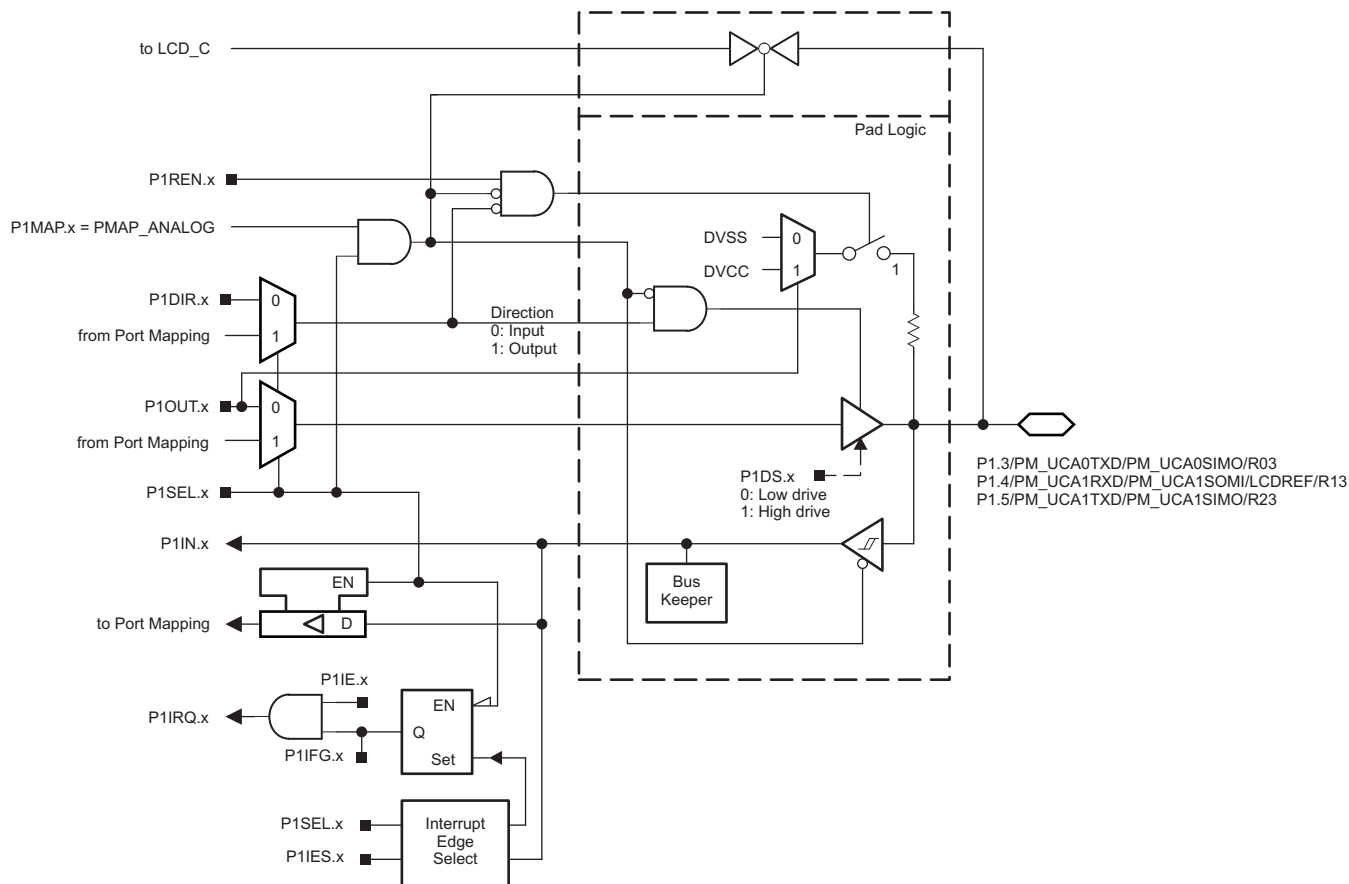


图 6-4. Port P1 (P1.3 to P1.5) Diagram (MSP430F67xxAIPZ and MSP430F67xxAIPN)

表 6-19. Port P1 (P1.3 to P1.5) Pin Functions (MSP430F67xxAIPZ and MSP430F67xxAIPN)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|--|---|---------------------------|--|---------|---------|
| | | | P1DIR.x | P1SEL.x | P1MAPx |
| P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA0TXD/UCA0SIMO | X | 1 | default |
| | | R03 ⁽²⁾ | X | 1 | = 31 |
| P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13 | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA1RXD/UCA1SOMI | X | 1 | default |
| | | LCDREF/R13 ⁽²⁾ | X | 1 | = 31 |
| P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA1TXD/UCA1SIMO | X | 1 | default |
| | | R23 ⁽²⁾ | X | 1 | = 31 |

(1) X = Don't care

(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver and the input Schmitt trigger.

6.12.4 Port P1 (P1.6 and P1.7) (MSP430F67xxAIPZ and MSP430F67xxAIPN) and Port P2 (P2.0 and P2.1) (MSP430F67xxAIPZ Only) Input/Output With Schmitt Trigger

图 6-5 shows the port diagram. 表 6-20 and 表 6-21 summarize the selection of the pin functions.

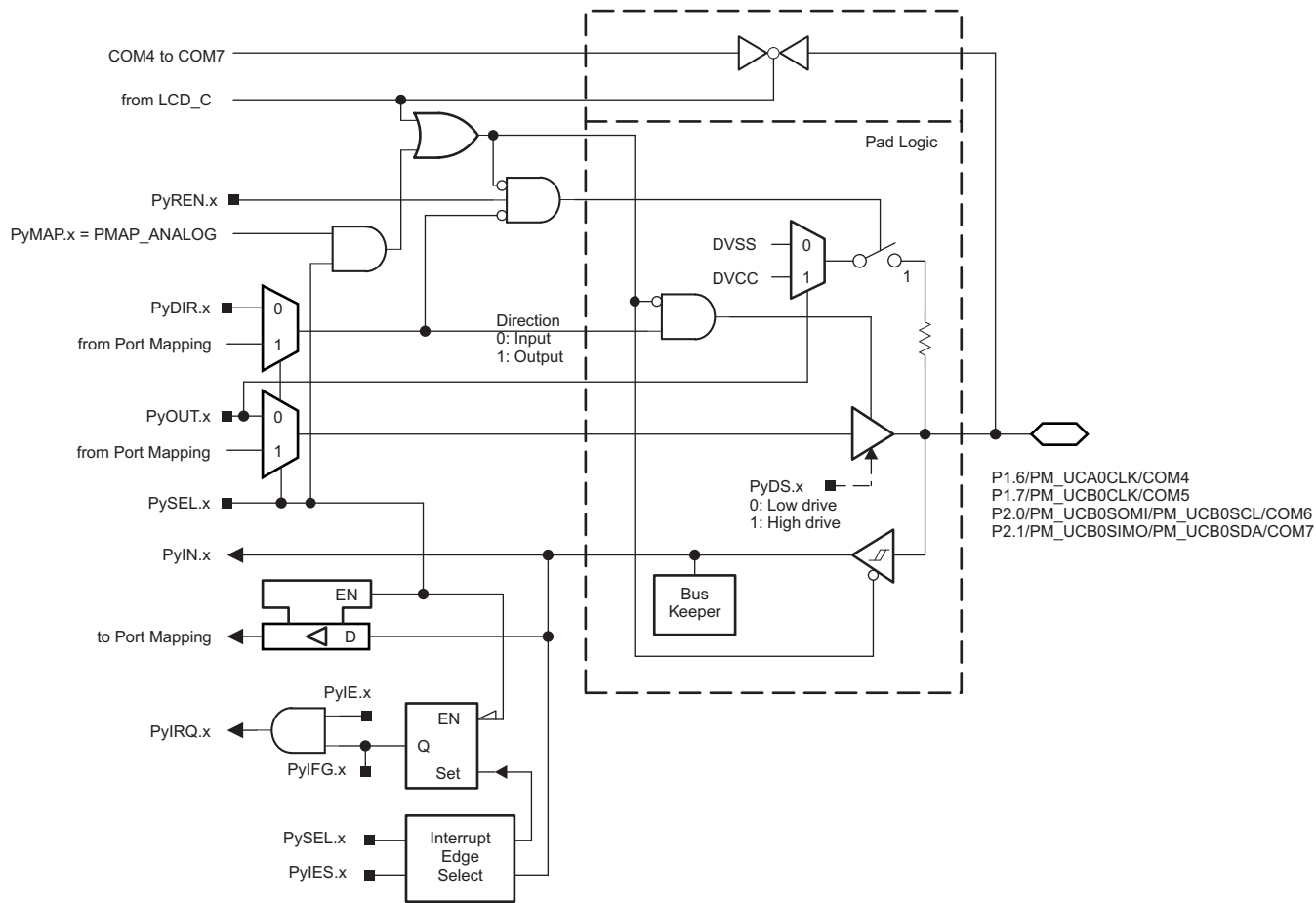


图 6-5. Port P1 (P1.6 and P1.7) (MSP430F67xxAIPZ and MSP430F67xxAIPN), Port P2 (P2.0 and P2.1) (MSP430F67xxAIPZ Only) Diagram

表 6-20. Port P1 (P1.6 and P1.7) Pin Functions (MSP430F67xxAIPZ and MSP430F67xxAIPN)

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|----------------------|---|--|--|---------|---------|--------------------------|
| | | | P1DIR.x | P1SEL.x | P1MAPx | COM4, COM5 Enable Signal |
| P1.6/PM_UCA0CLK/COM4 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA0CLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM4 | X | X | X | 1 |
| P1.7/PM_UCB0CLK/COM5 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCB0CLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM5 | X | X | X | 1 |

(1) X = Don't care

表 6-21. Port P2 (P2.0 and P2.1) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|--------------------------------------|---|--|--|---------|---------|--------------------------|
| | | | P2DIR.x | P2SEL.x | P2MAPx | COM6, COM7 Enable Signal |
| P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6 | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCB0SOMI/UCB0SCL | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM6 | X | X | X | 1 |
| P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCB0SIMO/UCB0SDA | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | COM7 | X | X | X | 1 |

(1) X = Don't care

6.12.5 Port P2 (P2.2 to P2.7) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ Only)

图 6-6 shows the port diagram. 表 6-22 summarizes the selection of the pin functions.

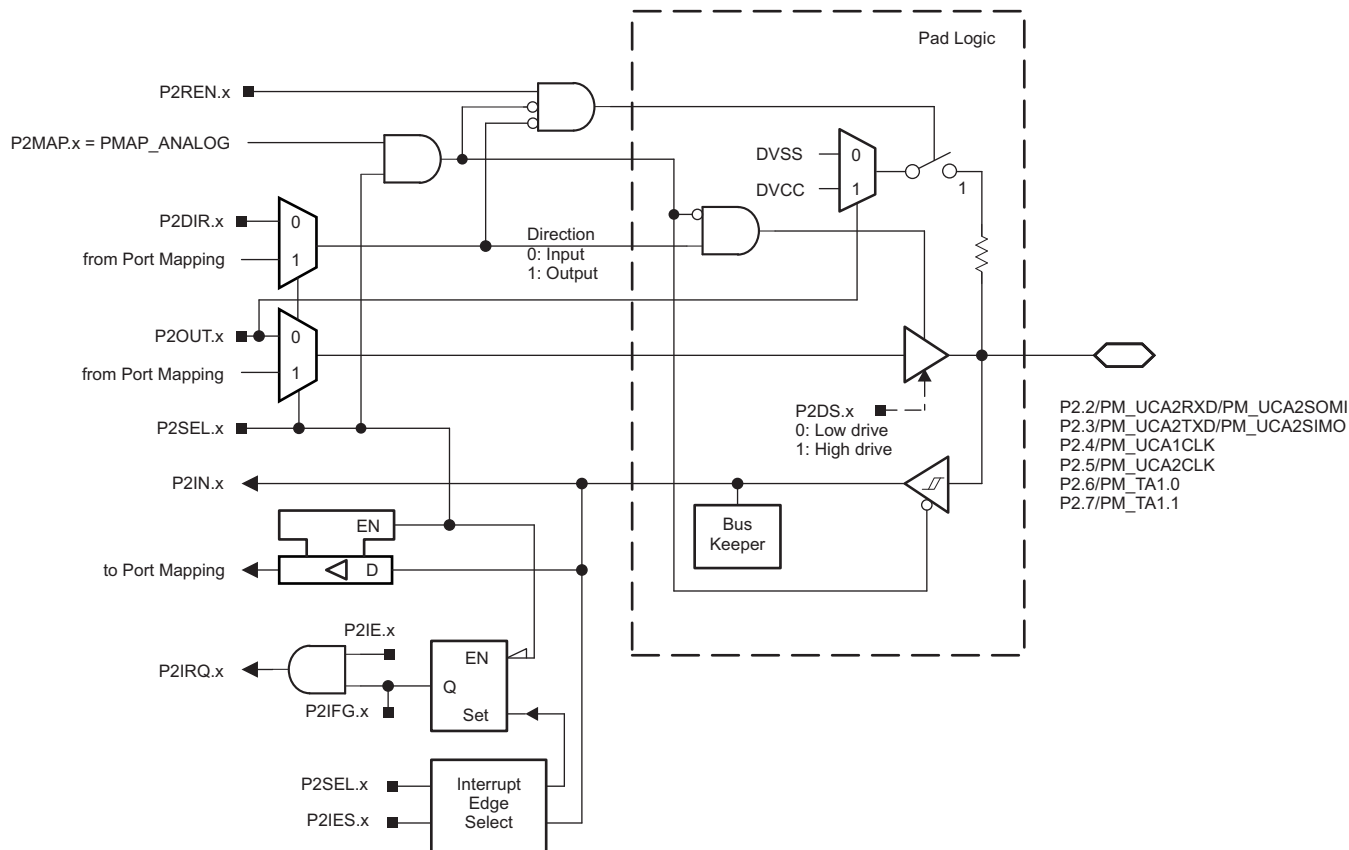


图 6-6. Port P2 (P2.2 to P2.7) Diagram (MSP430F67xxAIPZ Only)

表 6-22. Port P2 (P2.2 to P2.7) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|---------------------------------|---|--|--|---------|---------|
| | | | P2DIR.x | P2SEL.x | P2MAPx |
| P2.2/PM_UCA2RXD/ PM_UCA2SOMI | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA2RXD/UCA2SOMI | X | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.3/PM_UCA2TXD/ PM_UCA2SIMO | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA2TXD/UCA2SIMO | X | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.4/PM_UCA1CLK | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA1CLK | X | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.5/PM_UCA2CLK | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 | X |
| | | UCA2CLK | X | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.6/PM_TA1.0 | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA1.CC10A | 0 | 1 | default |
| | | TA1.TA0 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P2.7/PM_TA1.1 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA1.CC11A | 0 | 1 | default |
| | | TA1.TA1 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = Don't care

6.12.6 Port P3 (P3.0 to P3.3) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ Only)

图 6-7 shows the port diagram. 表 6-23 summarizes the selection of the pin functions.

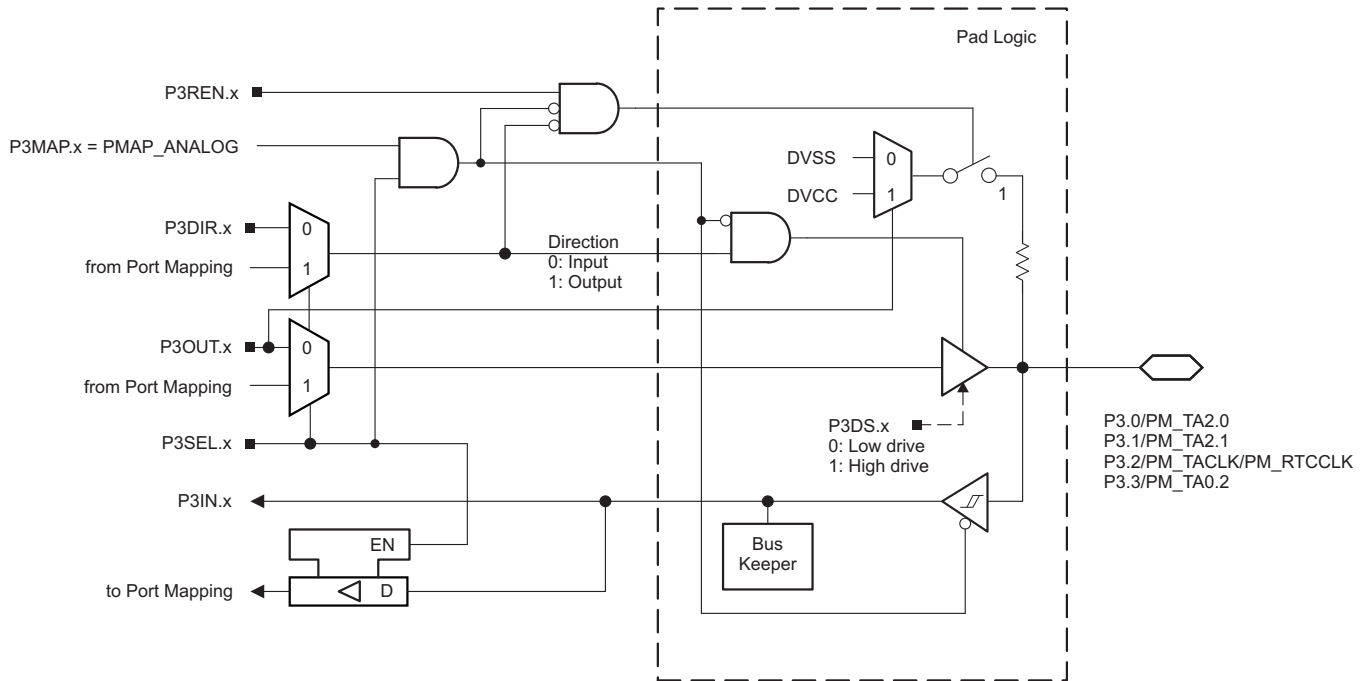


图 6-7. Port P3 (P3.0 to P3.3) Diagram (MSP430F67xxAIPZ Only)

表 6-23. Port P3 (P3.0 to P3.3) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------------------|---|--|--|---------|---------|
| | | | P3DIR.x | P3SEL.x | P3MAPx |
| P3.0/PM_TA2.0 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA2.CC10A | 0 | 1 | default |
| | | TA2.TA0 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.1/PM_TA2.1 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA2.CC11A | 0 | 1 | default |
| | | TA2.TA1 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.2/PM_TACLK/ PM_RTCCLK | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | X |
| | | TACLK | 0 | 1 | default |
| | | RTCCLK | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |
| P3.3/PM_TA0.2 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | X |
| | | TA0.CC12A | 0 | 1 | default |
| | | TA0.TA2 | 1 | 1 | default |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 |

(1) X = Don't care

6.12.7 Port P3 (P3.4 to P3.7) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ Only)

图 6-8 shows the port diagram. 表 6-24 summarizes the selection of the pin functions.

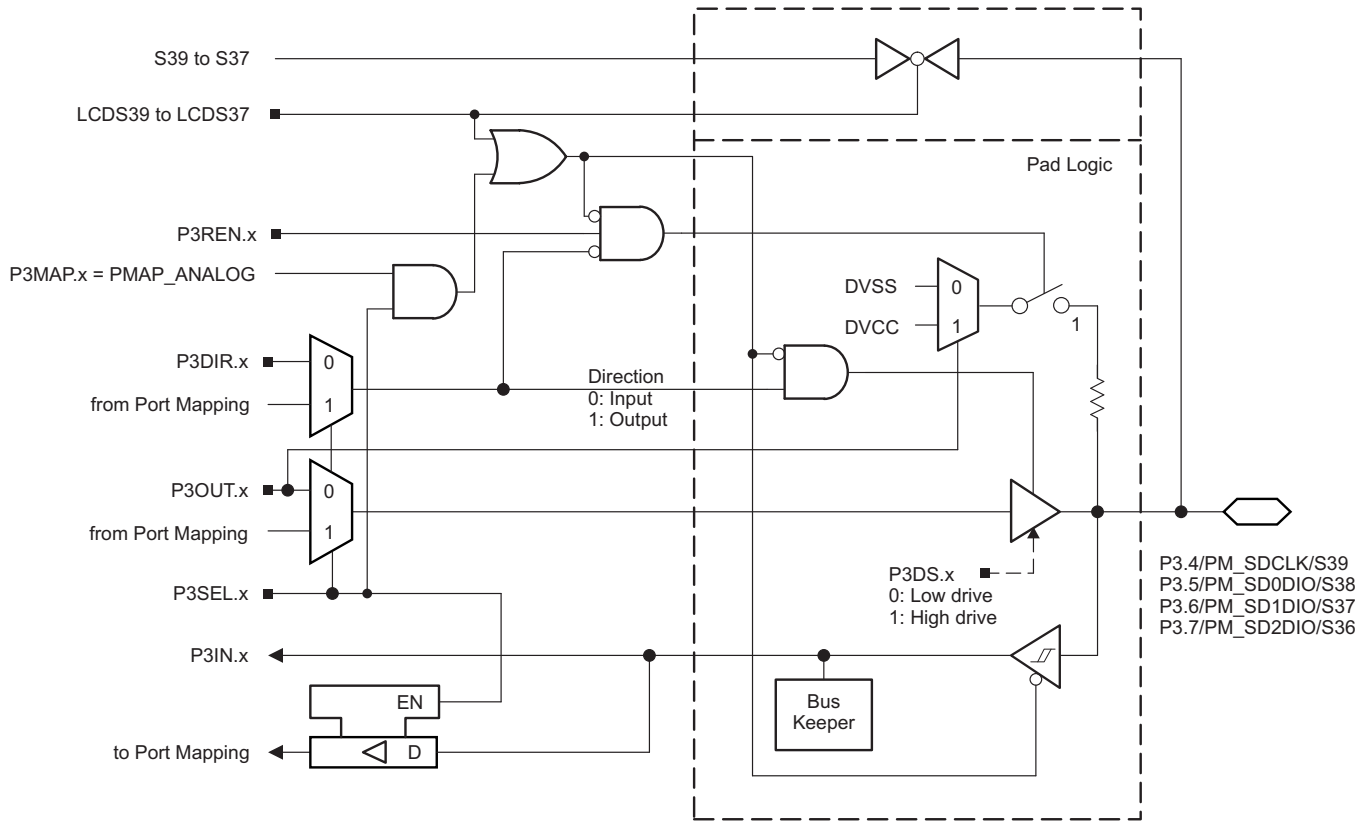


图 6-8. Port P3 (P3.4 to P3.7) Diagram (MSP430F67xxAIPZ Only)

表 6-24. Port P3 (P3.4 to P3.7) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|--------------------|---|--|--|---------|---------|---------------------|
| | | | P3DIR.x | P3SEL.x | P3MAPx | LCDS39... LCDS36 |
| P3.4/PM_SDCLK/S39 | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SDCLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S39 | X | X | X | 1 |
| P3.5/PM_SD0DIO/S38 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD0DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S38 | X | X | X | 1 |
| P3.6/PM_SD1DIO/S37 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD1DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S37 | X | X | X | 1 |
| P3.7/PM_SD2DIO/S36 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD2DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S36 | X | X | X | 1 |

(1) X = Don't care

6.12.8 Port P4 (P4.0 to P4.7), Port P5 (P5.0 to P5.7), Port P6 (P6.0 to P6.7), Port P7 (P7.0 to P7.7), Port P8 (P8.0 to P8.3) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ Only)

图 6-9 shows the port diagram. 表 6-25 through 表 6-29 summarize the selection of the pin functions.

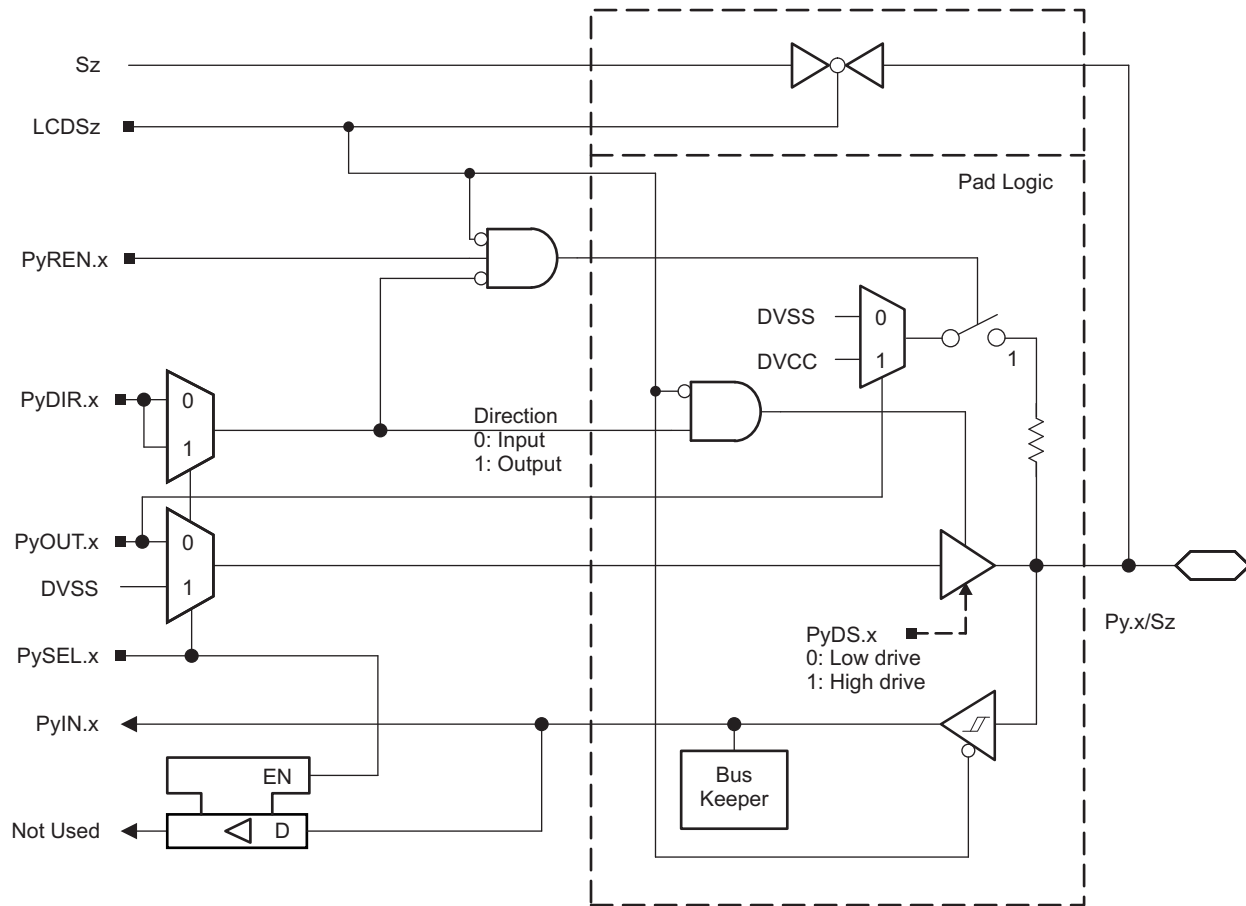


图 6-9. Port P4 (P4.0 to P4.7), Port P5 (P5.0 to P5.7), Port P6 (P6.0 to P6.7), Port P7 (P7.0 to P7.7), Port P8 (P8.0 to P8.3) Diagram (MSP430F67xxAIPZ Only)

表 6-25. Port P4 (P4.0 to P4.7) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|---------------------|
| | | | P4DIR.x | P4SEL.x | LCDS35... LCDS28 |
| P4.0/S35 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S35 | X | X | 1 |
| P4.1/S34 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S34 | X | X | 1 |
| P4.2/S33 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S33 | X | X | 1 |
| P4.3/S32 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S32 | X | X | 1 |
| P4.4/S31 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S31 | X | X | 1 |
| P4.5/S30 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S30 | X | X | 1 |
| P4.6/S29 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S29 | X | X | 1 |
| P4.7/S28 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S28 | X | X | 1 |

(1) X = Don't care

表 6-26. Port P5 (P5.0 to P5.7) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|---------------------|
| | | | P5DIR.x | P5SEL.x | LCDS27... LCDS20 |
| P5.0/S27 | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S27 | X | X | 1 |
| P5.1/S26 | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S26 | X | X | 1 |
| P5.2/S25 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S25 | X | X | 1 |
| P5.3/S24 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S24 | X | X | 1 |
| P5.4/S23 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P5.5/S22 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P5.6/S21 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P5.7/S20 | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S20 | X | X | 1 |

(1) X = Don't care

表 6-27. Port P6 (P6.0 to P6.7) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|---------------------|
| | | | P6DIR.x | P6SEL.x | LCDS19... LCDS12 |
| P6.0/S19 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P6.1/S18 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P6.2/S17 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S17 | X | X | 1 |
| P6.3/S16 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |
| P6.4/S15 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P6.5/S14 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P6.6/S13 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P6.7/S12 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |

(1) X = Don't care

表 6-28. Port P7 (P7.0 to P7.7) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|--------------------|
| | | | P7DIR.x | P7SEL.x | LCDS11... LCDS4 |
| P7.0/S11 | 0 | P7.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P7.1/S10 | 1 | P7.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P7.2/S9 | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |
| P7.3/S8 | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |
| P7.4/S7 | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P7.5/S6 | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P7.6/S5 | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P7.7/S4 | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |

(1) X = Don't care

表 6-29. Port P8 (P8.0 to P8.3) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|-------------------|
| | | | P8DIR.x | P8SEL.x | LCDS3... LCDS0 |
| P8.0/S3 | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P8.1/S2 | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P8.2/S1 | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |
| P8.3/S0 | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

(1) X = Don't care

6.12.9 Port P8 (P8.4 to P8.7) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ Only)

图 6-10 shows the port diagram. 表 6-30 summarizes the selection of the pin functions.

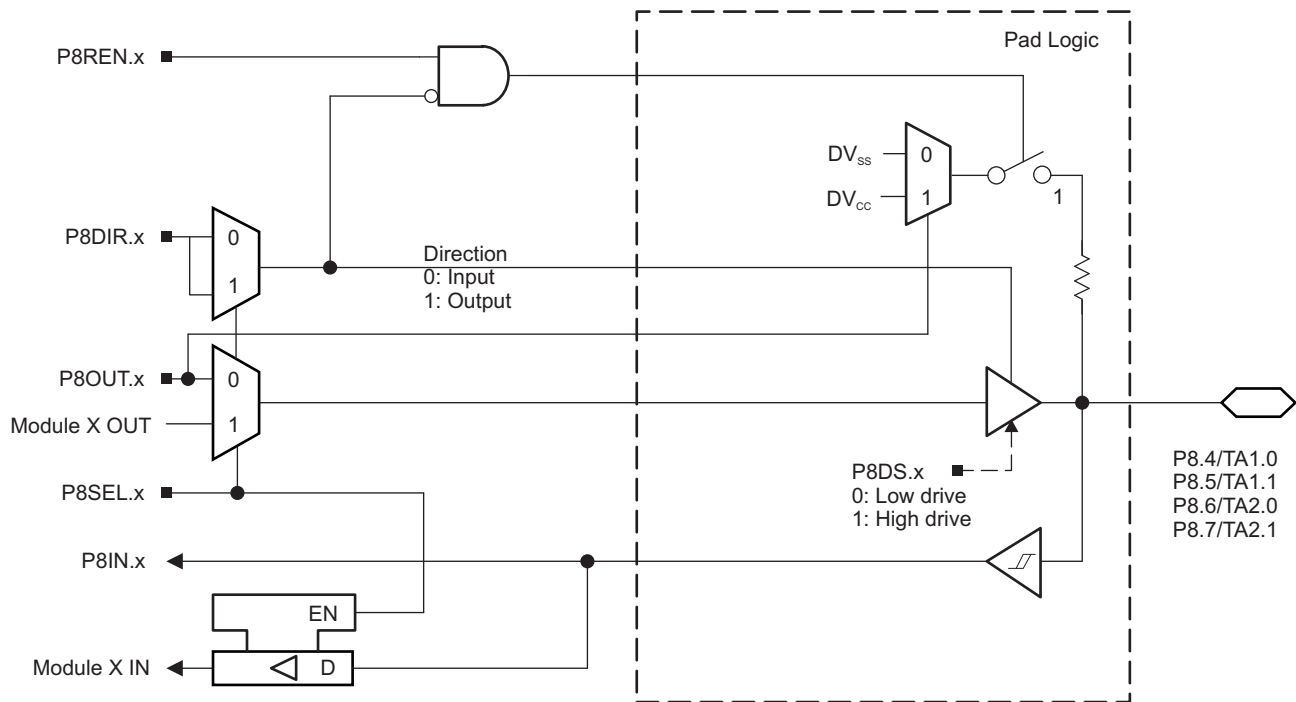


图 6-10. Port P8 (P8.4 to P8.7) Diagram (MSP430F67xxAIPZ Only)

表 6-30. Port P8 (P8.4 to P8.7) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|-----------------|---|------------|-------------------------|---------|
| | | | P8DIR.x | P8SEL.x |
| P8.4/TA1.0 | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI0A | 0 | 1 |
| | | TA1.TA0 | 1 | 1 |
| P8.5/TA1.1 | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI1A | 0 | 1 |
| | | TA1.TA1 | 1 | 1 |
| P8.6/TA2.0 | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 |
| | | TA2.CCI0A | 0 | 1 |
| | | TA2.TA0 | 1 | 1 |
| P8.7/TA2.1 | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 |
| | | TA2.CCI1A | 0 | 1 |
| | | TA2.TA1 | 1 | 1 |

6.12.10 Port P9 (P9.0) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ Only)

图 6-11 shows the port diagram. 表 6-31 summarizes the selection of the pin functions.

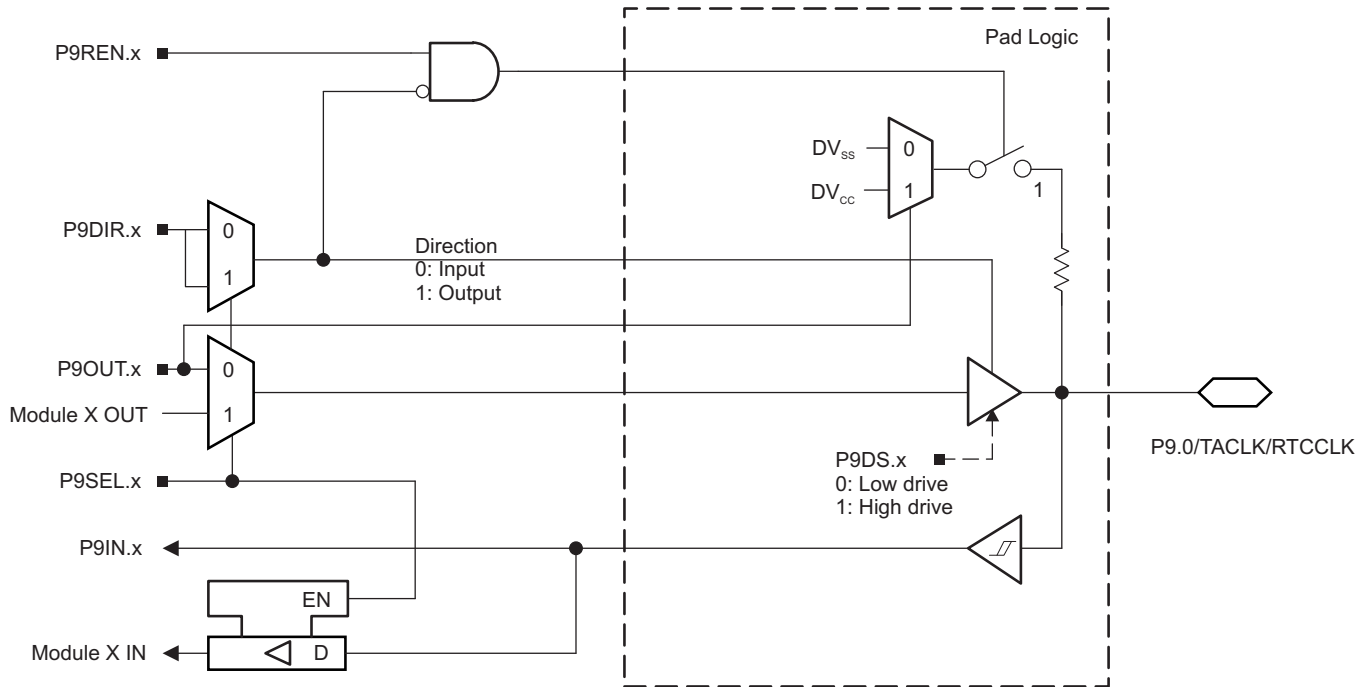


图 6-11. Port P9 (P9.0) Diagram (MSP430F67xxAIPZ Only)

表 6-31. Port P9 (P9.0) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | |
|-------------------|---|------------|-------------------------|---------|
| | | | P9DIR.x | P9SEL.x |
| P9.0/TACLK/RTCCLK | 0 | P9.0 (I/O) | I: 0; O: 1 | 0 |
| | | TACLK | 0 | 1 |
| | | RTCCLK | 1 | 1 |

6.12.11 Port P9 (P9.1 to P9.3) Input/Output With Schmitt Trigger (MSP430F67xxAIPZ Only)

图 6-12 shows the port diagram. 表 6-32 summarizes the selection of the pin functions.

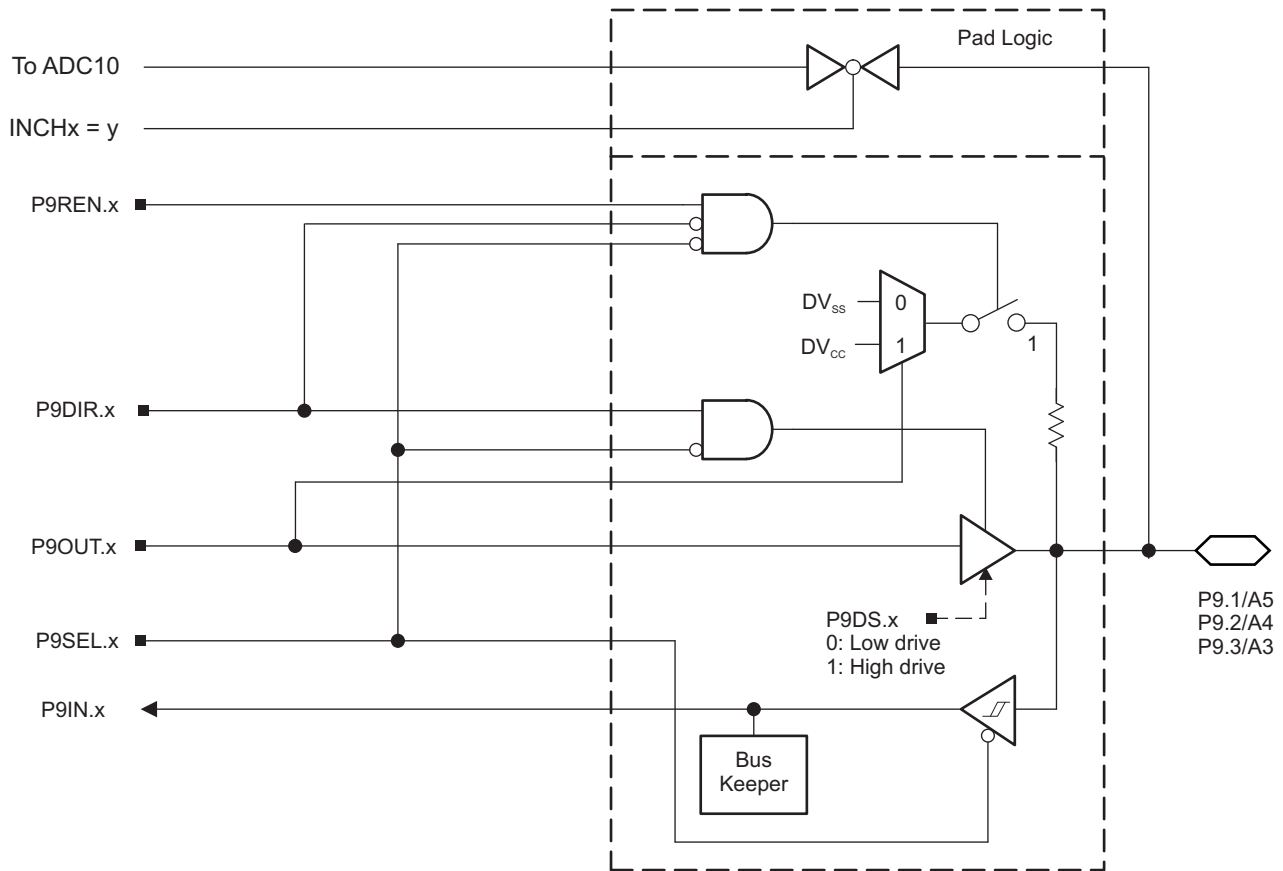


图 6-12. Port P9 (P9.1 to P9.3) Diagram (MSP430F67xxAIPZ Only)

表 6-32. Port P9 (P9.1 to P9.3) Pin Functions (MSP430F67xxAIPZ Only)

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | |
|-----------------|---|-------------------|--|---------|
| | | | P9DIR.x | P9SEL.x |
| P9.1/A5 | 1 | P9.1 (I/O) | I: 0; O: 1 | 0 |
| | | A5 ⁽²⁾ | X | 1 |
| P9.2/A4 | 2 | P9.2 (I/O) | I: 0; O: 1 | 0 |
| | | A4 ⁽²⁾ | X | 1 |
| P9.3/A3 | 3 | P9.3 (I/O) | I: 0; O: 1 | 0 |
| | | A3 ⁽²⁾ | X | 1 |

(1) X = Don't care

(2) Setting P9SEL.x bit disables the output driver and the input Schmitt trigger.

6.12.12 Port P2 (P2.0 and P2.1) Input/Output With Schmitt Trigger (MSP430F67xxAIPN Only)

图 6-13 shows the port diagram. 表 6-33 summarizes the selection of the pin functions.

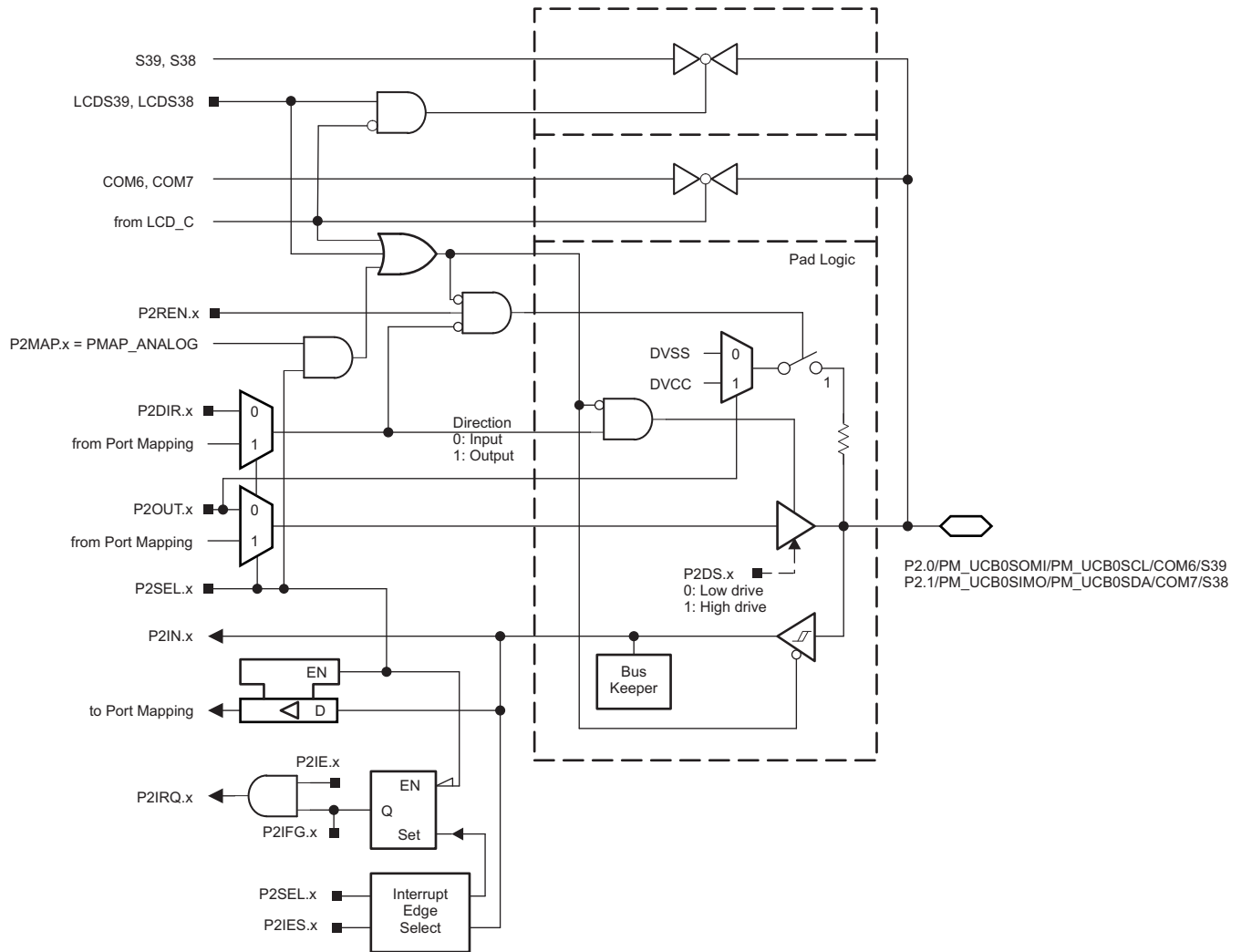


图 6-13. Port P2 (P2.0 and P2.1) Diagram (MSP430F67xxAIPN Only)

表 6-33. Port P2 (P2.0 and P2.1) Pin Functions (MSP430F67xxAIPN Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | | |
|--|---|--|--|---------|---------|-------------------|-----------------------------------|
| | | | P2DIR.x | P2SEL.x | P2MAPx | LCDS39, LCDS38 | COM6, COM7 Enable Signal |
| P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6/ S39 | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | X | 0 | 0 |
| | | UCB0SOMI/UCB0SCL | X | 1 | default | 0 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 | 0 |
| | | COM6 | X | X | X | X | 1 |
| | | S39 | X | X | X | 1 | 0 |
| P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7/ S38 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | X | 0 | 0 |
| | | UCB0SIMO/UCB0SDA | X | 1 | default | 0 | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 | 0 |
| | | COM7 | X | X | X | X | 1 |
| | | S38 | X | X | X | 1 | 0 |

(1) X = Don't care

6.12.13 Port P2 (P2.2 to P2.7) Input/Output With Schmitt Trigger (MSP430F67xxAIPN Only)

图 6-14 shows the port diagram. 表 6-34 summarizes the selection of the pin functions.

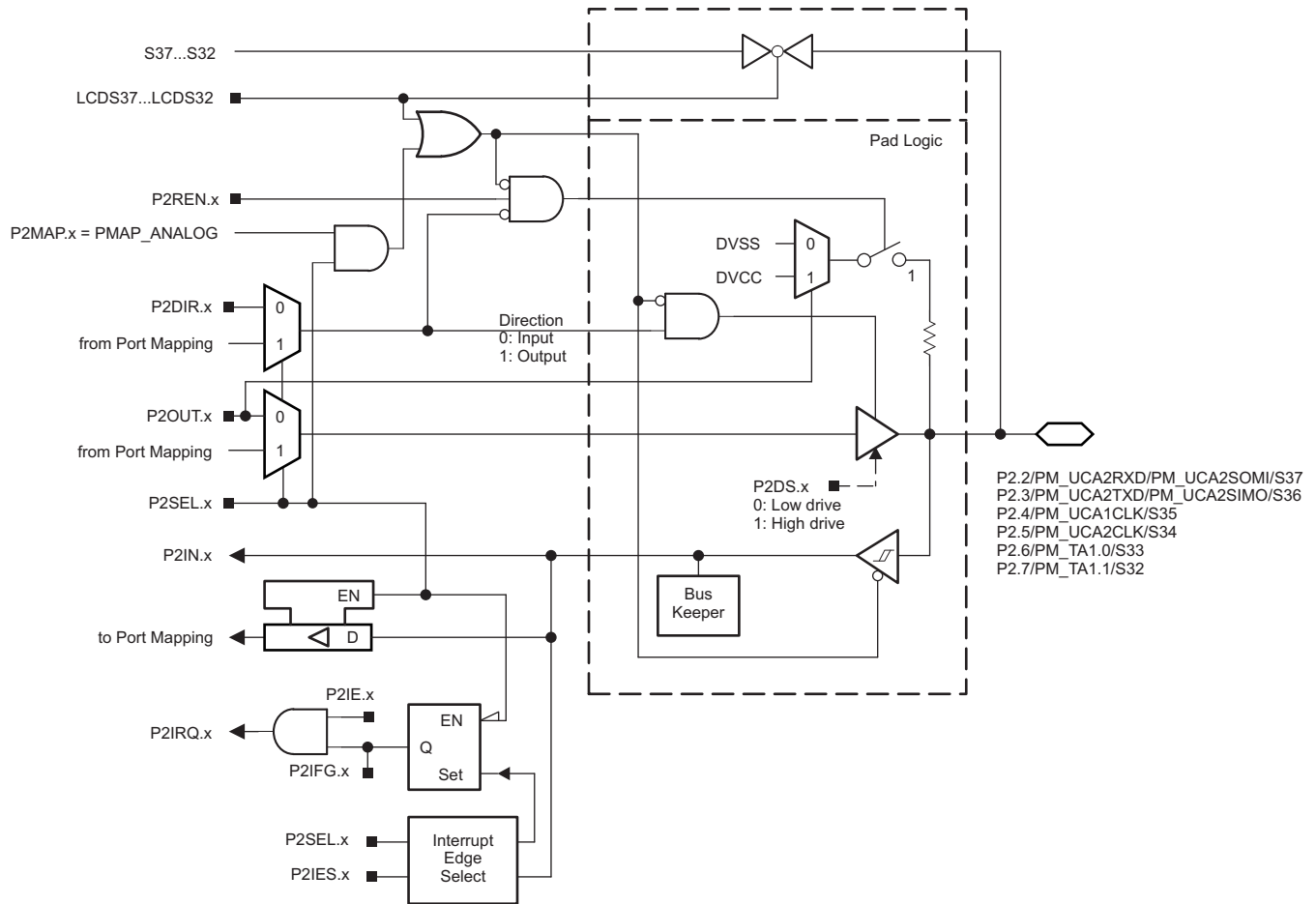


图 6-14. Port P2 (P2.2 to P2.7) Diagram (MSP430F67xxAIPN Only)

表 6-34. Port P2 (P2.2 to P2.7) Pin Functions (MSP430F67xxAIPN Only)

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|-------------------------------------|---|--|--|---------|---------|---------------------|
| | | | P2DIR.x | P2SEL.x | P2MAPx | LCDS37... LCDS32 |
| P2.2/PM_UCA2RXD/ PM_UCA2SOMI/S37 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA2RXD/UCA2SOMI | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S37 | X | X | X | 1 |
| P2.3/PM_UCA2TXD/ PM_UCA2SIMO/S36 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA2TXD/UCA2SIMO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S36 | X | X | X | 1 |
| P2.4/PM_UCA1CLK/S35 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA1CLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S35 | X | X | X | 1 |
| P2.5/PM_UCA2CLK/S34 | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | UCA2CLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S34 | X | X | X | 1 |
| P2.6/PM_TA1.0/S33 | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA1.CCI0A | 0 | 1 | default | 0 |
| | | TA1.TA0 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S33 | X | X | X | 1 |
| P2.7/PM_TA1.1/S32 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA1.CCI1A | 0 | 1 | default | 0 |
| | | TA1.TA1 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S32 | X | X | X | 1 |

(1) X = Don't care

6.12.14 Port P3 (P3.0 to P3.7) Input/Output With Schmitt Trigger (MSP430F67xxAIPN Only)

图 6-15 shows the port diagram. 表 6-35 summarizes the selection of the pin functions.

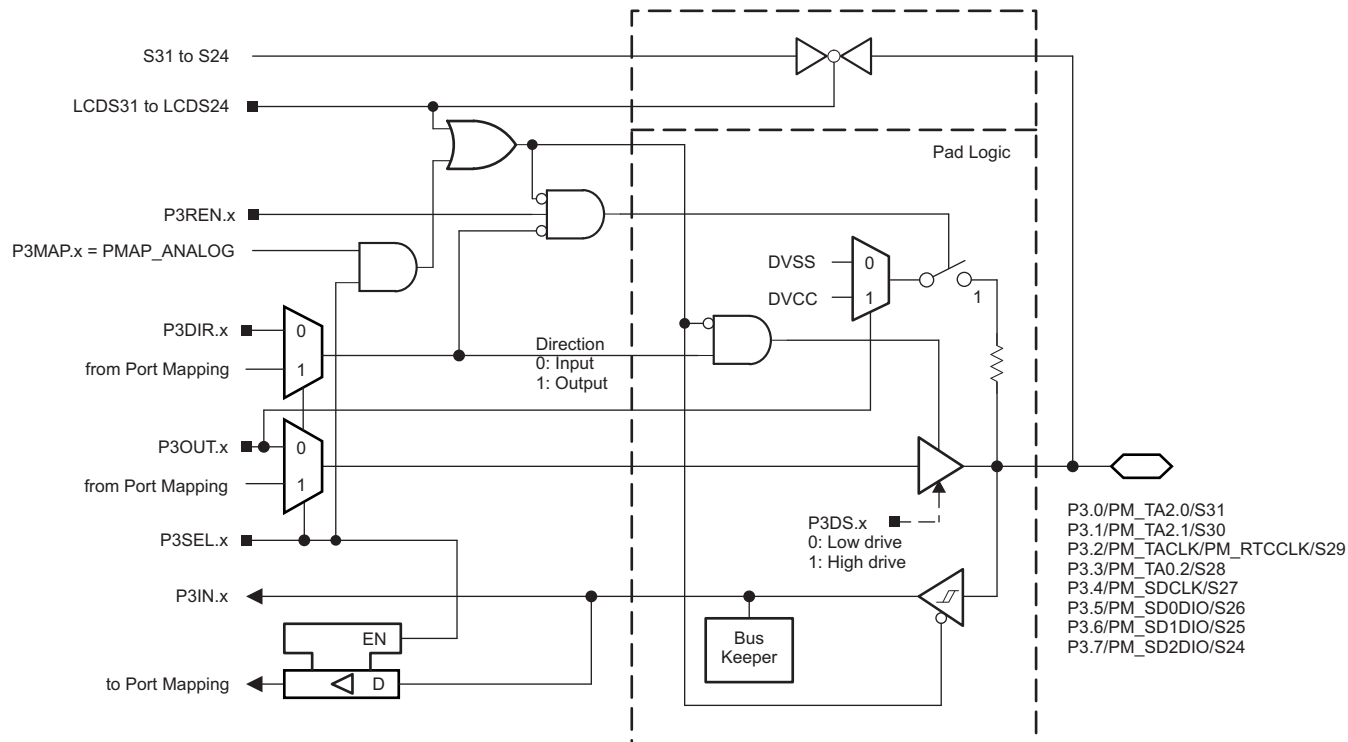


图 6-15. Port P3 (P3.0 to P3.7) Diagram (MSP430F67xxAIPN Only)

表 6-35. Port P3 (P3.0 to P3.7) Pin Functions (MSP430F67xxAIPN Only)

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | | |
|---------------------------------|---|--|--|---------|---------|---------------------|
| | | | P3DIR.x | P3SEL.x | P3MAPx | LCDS31... LCDS24 |
| P3.0/PM_TA2.0/S31 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA2.CCI0A | 0 | 1 | default | 0 |
| | | TA2.TA0 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S31 | X | X | X | 1 |
| P3.1/PM_TA2.1/S30 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA2.CCI1A | 0 | 1 | default | 0 |
| | | TA2.TA1 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S30 | X | X | X | 1 |
| P3.2/PM_TACLK/ PM_RTCCLK/S29 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TACLK | 0 | 1 | default | 0 |
| | | RTCCLK | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S29 | X | X | X | 1 |
| P3.3/PM_TA0.2/S28 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | TA0.CCI2A | 0 | 1 | default | 0 |
| | | TA0.TA2 | 1 | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S28 | X | X | X | 1 |
| P3.4/PM_SDCLK/S27 | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SDCLK | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S27 | X | X | X | 1 |
| P3.5/PM_SD0DIO/S26 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD0DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S26 | X | X | X | 1 |
| P3.6/PM_SD1DIO/S25 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD1DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S25 | X | X | X | 1 |
| P3.7/PM_SD2DIO/S24 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | X | 0 |
| | | SD2DIO | X | 1 | default | 0 |
| | | Output driver and input Schmitt trigger disabled | X | 1 | = 31 | 0 |
| | | S24 | X | X | X | 1 |

(1) X = Don't care

6.12.15 Port P4 (P4.0 to P4.7), Port P5 (P5.0 to P5.7), Port P6 (P6.0 to P6.7) Input/Output With Schmitt Trigger (MSP430F67xxAIPN Only)

图 6-16 shows the port diagram. 表 6-36 through 表 6-38 summarize the selection of the pin functions.

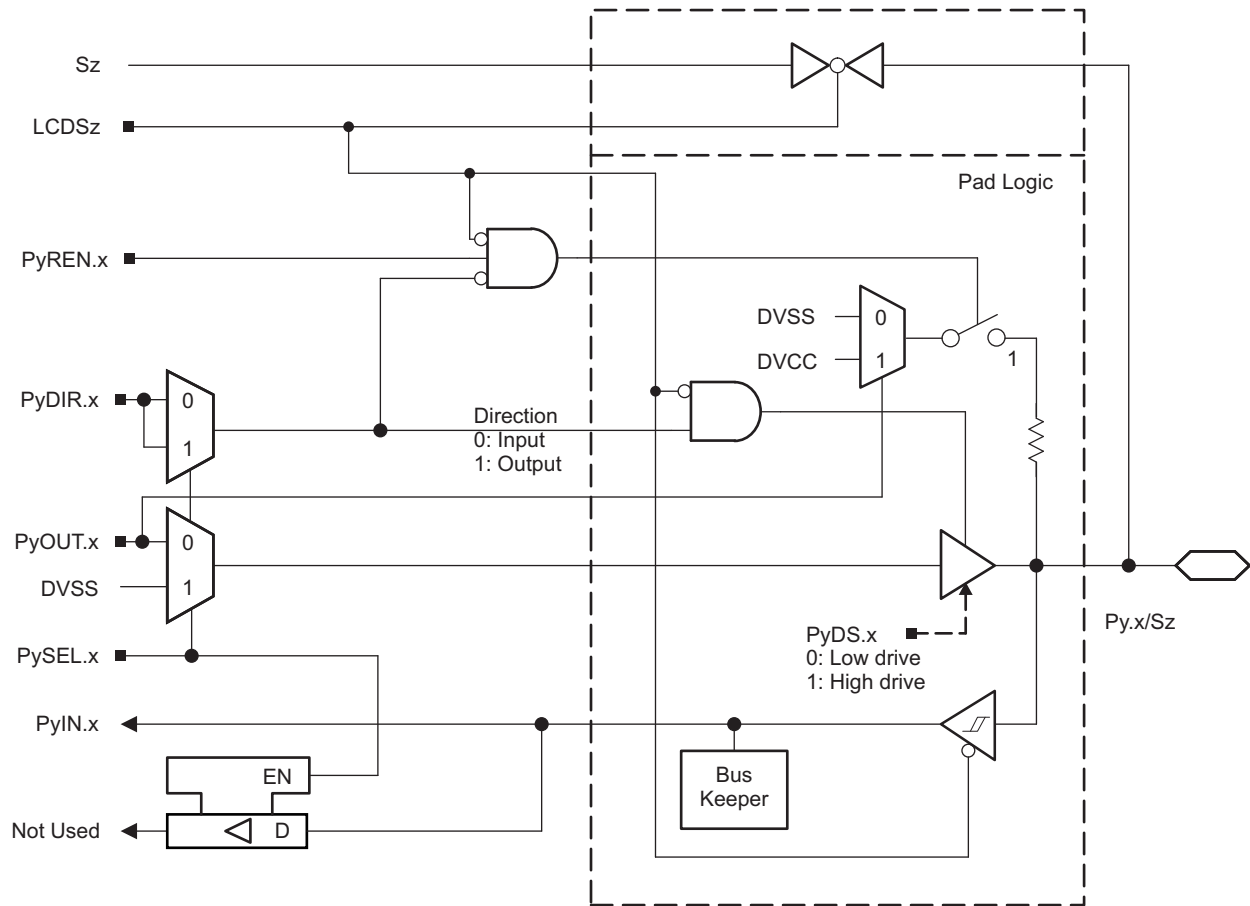


图 6-16. Port P4 (P4.0 to P4.7), Port P5 (P5.0 to P5.7), Port P6 (P6.0 to P6.7) Diagram (MSP430F67xxAIPN Only)

表 6-36. Port P4 (P4.0 to P4.7) Pin Functions (MSP430F67xxAIPN Only)

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|---------------------|
| | | | P4DIR.x | P4SEL.x | LCDS23... LCDS16 |
| P4.0/S23 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S23 | X | X | 1 |
| P4.1/S22 | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S22 | X | X | 1 |
| P4.2/S21 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S21 | X | X | 1 |
| P4.3/S20 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S20 | X | X | 1 |
| P4.4/S19 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S19 | X | X | 1 |
| P4.5/S18 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S18 | X | X | 1 |
| P4.6/S17 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S17 | X | X | 1 |
| P4.7/S16 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S16 | X | X | 1 |

(1) X = Don't care

表 6-37. Port P5 (P5.0 to P5.7) Pin Functions (MSP430F67xxAIPN Only)

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|--------------------|
| | | | P5DIR.x | P5SEL.x | LCDS15... LCDS8 |
| P5.0/S15 | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S15 | X | X | 1 |
| P5.1/S14 | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S14 | X | X | 1 |
| P5.2/S13 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S13 | X | X | 1 |
| P5.3/S12 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S12 | X | X | 1 |
| P5.4/S11 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S11 | X | X | 1 |
| P5.5/S10 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S10 | X | X | 1 |
| P5.6/S9 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S9 | X | X | 1 |
| P5.7/S8 | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S8 | X | X | 1 |

(1) X = Don't care

表 6-38. Port P6 (P6.0 to P6.7) Pin Functions (MSP430F67xxAIPN Only)

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|--|---------|-------------------|
| | | | P6DIR.x | P6SEL.x | LCDS7... LCDS0 |
| P6.0/S7 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S7 | X | X | 1 |
| P6.1/S6 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S6 | X | X | 1 |
| P6.2/S5 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S5 | X | X | 1 |
| P6.3/S4 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S4 | X | X | 1 |
| P6.4/S3 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S3 | X | X | 1 |
| P6.5/S2 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S2 | X | X | 1 |
| P6.6/S1 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S1 | X | X | 1 |
| P6.7/S0 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | 1 | 0 |
| | | S0 | X | X | 1 |

(1) X = Don't care

6.12.16 Port PJ (PJ.0) JTAG Pin TDO, Input/Output With Schmitt Trigger or Output

图 6-17 shows the port diagram. 表 6-39 summarizes the selection of the pin functions.

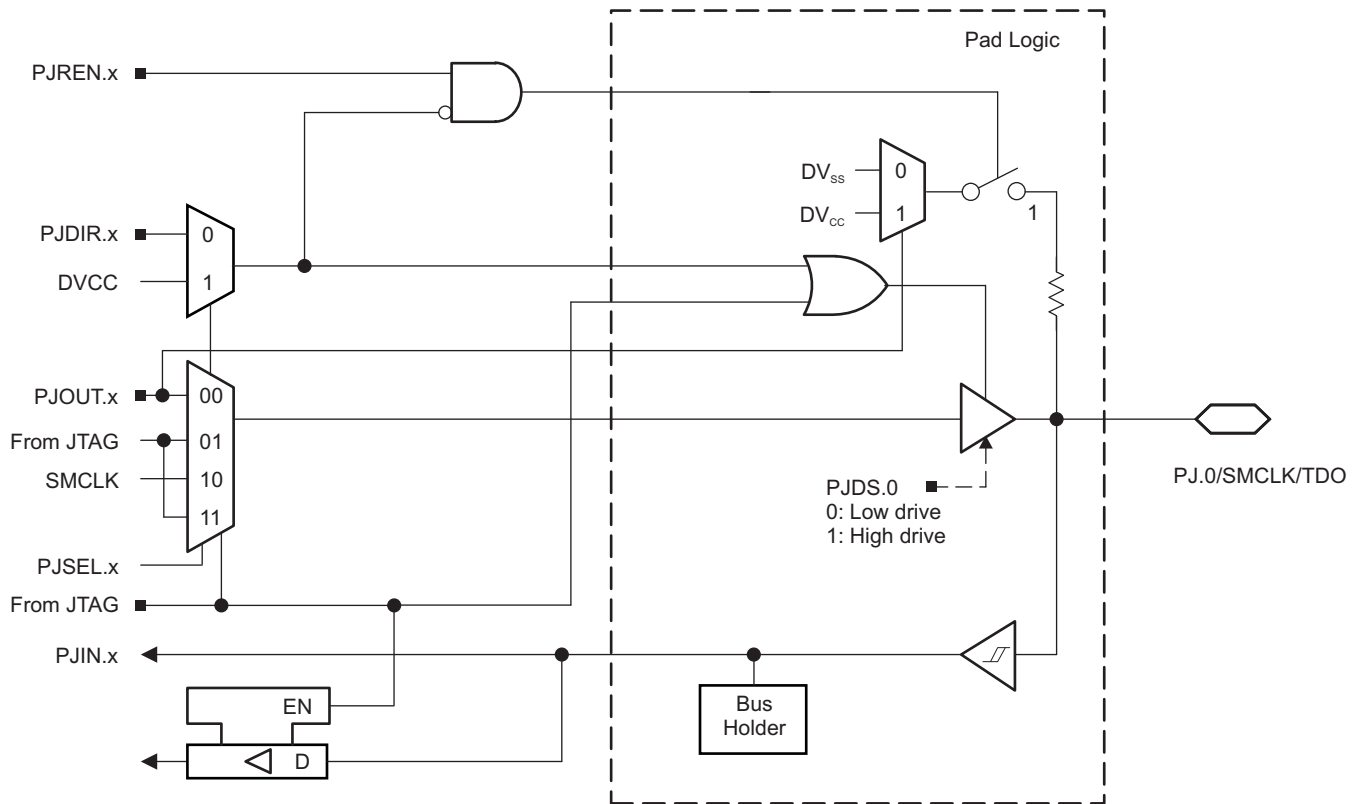


图 6-17. Port PJ (PJ.0) Diagram

6.12.17 Port PJ (PJ.1 to PJ.3) JTAG Pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

图 6-18 shows the port diagram. 表 6-39 summarizes the selection of the pin functions.

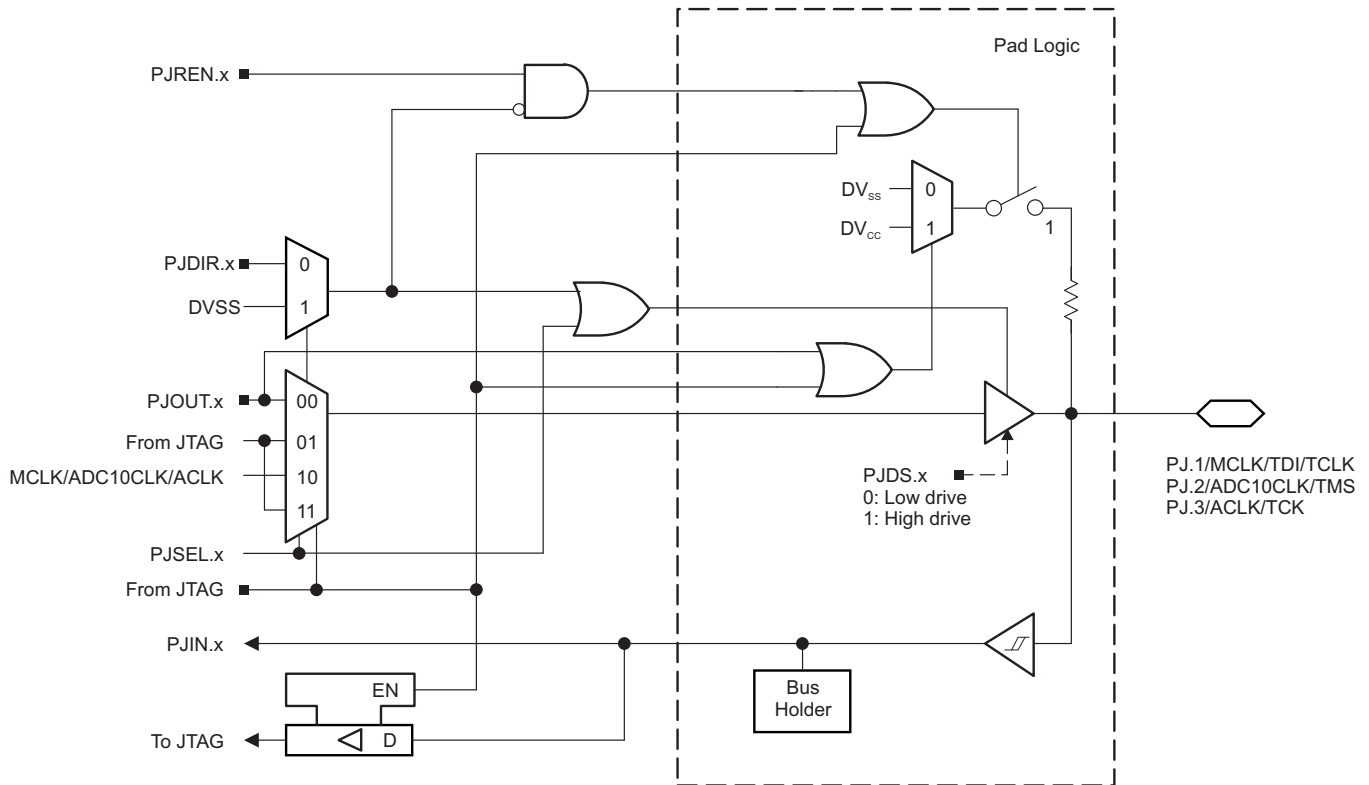


图 6-18. Port PJ (PJ.1 to PJ.3) Diagram

表 6-39. Port PJ (PJ.0 to PJ.3) Pin Functions

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS ⁽¹⁾ | | |
|--------------------|---|-----------------------------|--|---------|------------------|
| | | | PJDIR.x | PJSEL.x | JTAG Mode Signal |
| PJ.0/SMCLK/TDO | 0 | PJ.0 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | SMCLK | 1 | 1 | 0 |
| | | TDO ⁽³⁾ | X | X | 1 |
| PJ.1/MCLK/TDI/TCLK | 1 | PJ.1 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | MCLK | 1 | 1 | 0 |
| | | TDI/TCLK ^{(3) (4)} | X | X | 1 |
| PJ.2/ADC10CLK/TMS | 2 | PJ.2 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | ADC10CLK | 1 | 1 | 0 |
| | | TMS ^{(3) (4)} | X | X | 1 |
| PJ.3/ACLK/TCK | 3 | PJ.3 (I/O) ⁽²⁾ | I: 0; O: 1 | 0 | 0 |
| | | ACLK | 1 | 1 | 0 |
| | | TCK ^{(3) (4)} | X | X | 1 |

(1) X = Don't care

(2) Default condition

(3) The pin direction is controlled by the JTAG module.

(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

6.13 Device Descriptors (TLV)

表 6-40 和 表 6-41 列出设备描述符 tag-length-value (TLV) 结构的完整内容，适用于每个设备类型。

表 6-40. MSP430F673xA Device Descriptors

| DESCRIPTION | ADDRESS | SIZE (bytes) | VALUE | | | | | | |
|-------------------|--|-----------------|--------|----------|----------|----------|----------|----------|----------|
| | | | F6736A | F6735A | F6734A | F6733A | F6731A | F6730A | |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 01A04h | 1 | 86h | 85h | 84h | 83h | 81h | 80h |
| | Device ID | 01A05h | 1 | 82h | 82h | 82h | 82h | 82h | 82h |
| | Hardware revision | 01A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 01A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die X position | 01A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die Y position | 01A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test results | 01A12h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC10 calibration tag | 01A14h | 1 | 13h | 13h | 13h | 13h | 13h | 13h |
| | ADC10 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 01A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 30°C | 01A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 85°C | 01A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |

表 6-41. MSP430F672xA Device Descriptors

| DESCRIPTION | ADDRESS | SIZE (bytes) | VALUE | | | | | | |
|-------------------|--|-----------------|--------|----------|----------|----------|----------|----------|----------|
| | | | F6726A | F6725A | F6724A | F6723A | F6721A | F6720A | |
| Info Block | Info length | 01A00h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC length | 01A01h | 1 | 06h | 06h | 06h | 06h | 06h | 06h |
| | CRC value | 01A02h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Device ID | 01A04h | 1 | 7Ch | 7Bh | 7Ah | 79h | 77h | 76h |
| | Device ID | 01A05h | 1 | 82h | 82h | 82h | 82h | 82h | 82h |
| | Hardware revision | 01A06h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Firmware revision | 01A07h | 1 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| Die Record | Die record tag | 01A08h | 1 | 08h | 08h | 08h | 08h | 08h | 08h |
| | Die record length | 01A09h | 1 | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah | 0Ah |
| | Lot/wafer ID | 01A0Ah | 4 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die X position | 01A0Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Die Y position | 01A10h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | Test results | 01A12h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| ADC10 Calibration | ADC10 calibration tag | 01A14h | 1 | 13h | 13h | 13h | 13h | 13h | 13h |
| | ADC10 calibration length | 01A15h | 1 | 10h | 10h | 10h | 10h | 10h | 10h |
| | ADC gain factor | 01A16h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC offset | 01A18h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 30°C | 01A1Ah | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 1.5-V reference Temperature sensor 85°C | 01A1Ch | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 30°C | 01A1Eh | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.0-V reference Temperature sensor 85°C | 01A20h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 30°C | 01A22h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |
| | ADC 2.5-V reference Temperature sensor 85°C | 01A24h | 2 | Per unit | Per unit | Per unit | Per unit | Per unit | Per unit |

6.14 Memory

6.14.1 Memory Organization

表 6-42 和 表 6-43 总结所有器件变体的内存图。

表 6-42. Memory Organization

| | | MSP430F6730A MSP430F6720A | MSP430F6731A MSP430F6721A | MSP430F6733A MSP430F6723A |
|---------------------------------|------------|------------------------------|------------------------------|------------------------------|
| Main Memory (flash) | Total Size | 16KB | 32KB | 64KB |
| Main: Interrupt vector | | 00FFFFh–00FF80h | 00FFFFh–00FF80h | 00FFFFh–00FF80h |
| Main: code memory | Bank 3 | Not available | Not available | Not available |
| | Bank 2 | Not available | Not available | Not available |
| | Bank 1 | Not available | 16KB 00FFFFh–00C000h | 32KB 013FFFh–00C000h |
| | Bank 0 | 16KB 00FFFFh–00C000h | 16KB 00BFFFh–008000h | 32KB 00BFFFh–004000h |
| RAM | Total Size | 1KB | 2KB | 4KB |
| | Sector 3 | Not available | Not available | Not available |
| | Sector 2 | Not available | Not available | Not available |
| | Sector 1 | Not available | Not available | 2KB 002BFFh–002400h |
| | Sector 0 | 1KB 001FFFh–001C00h | 2KB 0023FFh–001C00h | 2KB 0023FFh–001C00h |
| Information memory (flash) | Info A | 128 B 0019FFh–001980h | 128 B 0019FFh–001980h | 128 B 0019FFh–001980h |
| | Info B | 128 B 00197Fh–001900h | 128 B 00197Fh–001900h | 128 B 00197Fh–001900h |
| | Info C | 128 B 0018FFh–001880h | 128 B 0018FFh–001880h | 128 B 0018FFh–001880h |
| | Info D | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B 0017FFh–001600h | 512 B 0017FFh–001600h | 512 B 0017FFh–001600h |
| | BSL 2 | 512 B 0015FFh–001400h | 512 B 0015FFh–001400h | 512 B 0015FFh–001400h |
| | BSL 1 | 512 B 0013FFh–001200h | 512 B 0013FFh–001200h | 512 B 0013FFh–001200h |
| | BSL 0 | 512 B 0011FFh–001000h | 512 B 0011FFh–001000h | 512 B 0011FFh–001000h |
| Peripherals | | 4 KB 000FFFh–0h | 4 KB 000FFFh–0h | 4 KB 000FFFh–0h |

表 6-43. Memory Organization

| | | MSP430F6734A MSP430F6724A | MSP430F6735A MSP430F6725A | MSP430F6736A MSP430F6726A |
|---------------------------------|------------|------------------------------|------------------------------|------------------------------|
| Main Memory (flash) | Total Size | 96KB | 128KB | 128KB |
| Main: Interrupt vector | | 00FFFFh–00FF80h | 00FFFFh–00FF80h | 00FFFFh–00FF80h |
| Main: code memory | Bank 3 | Not available | 32KB 023FFFh–01C000h | 32KB 023FFFh–01C000h |
| | Bank 2 | 32KB 01BFFFh–014000h | 32KB 01BFFFh–014000h | 32KB 01BFFFh–014000h |
| | Bank 1 | 32KB 013FFFh–00C000h | 32KB 013FFFh–00C000h | 32KB 013FFFh–00C000h |
| | Bank 0 | 32KB 00BFFFh–004000h | 32KB 00BFFFh–004000h | 32KB 00BFFFh–004000h |
| RAM | Total Size | 4KB | 4KB | 8KB |
| | Sector 3 | Not available | Not available | 2KB 003BFFFh–003400h |
| | Sector 2 | Not available | Not available | 2KB 0033FFFh–002C00h |
| | Sector 1 | 2KB 002BFFFh–002400h | 2KB 002BFFFh–002400h | 2KB 002BFFFh–002400h |
| | Sector 0 | 2KB 0023FFFh–001C00h | 2KB 0023FFFh–001C00h | 2KB 0023FFFh–001C00h |
| Information memory (flash) | Info A | 128 B 0019FFFh–001980h | 128 B 0019FFFh–001980h | 128 B 0019FFFh–001980h |
| | Info B | 128 B 00197Fh–001900h | 128 B 00197Fh–001900h | 128 B 00197Fh–001900h |
| | Info C | 128 B 0018FFFh–001880h | 128 B 0018FFFh–001880h | 128 B 0018FFFh–001880h |
| | Info D | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h | 128 B 00187Fh–001800h |
| Bootloader (BSL) memory (flash) | BSL 3 | 512 B 0017FFFh–001600h | 512 B 0017FFFh–001600h | 512 B 0017FFFh–001600h |
| | BSL 2 | 512 B 0015FFFh–001400h | 512 B 0015FFFh–001400h | 512 B 0015FFFh–001400h |
| | BSL 1 | 512 B 0013FFFh–001200h | 512 B 0013FFFh–001200h | 512 B 0013FFFh–001200h |
| | BSL 0 | 512 B 0011FFFh–001000h | 512 B 0011FFFh–001000h | 512 B 0011FFFh–001000h |
| Peripherals | | 4 KB 000FFFh–0h | 4 KB 000FFFh–0h | 4 KB 000FFFh–0h |

6.14.2 Peripheral File Map

表 6-44 lists the available modules with the base address and the offset range for each. 表 6-45 through 表 6-82 list all of the available registers for each module.

表 6-44. Peripheral File Map

| MODULE NAME | BASE ADDRESS | OFFSET ADDRESS RANGE |
|--|--------------|----------------------|
| Special Functions (see 表 6-45) | 0100h | 000h–01Fh |
| PMM (see 表 6-46) | 0120h | 000h–01Fh |
| Flash Control (see 表 6-47) | 0140h | 000h–00Fh |
| CRC16 (see 表 6-48) | 0150h | 000h–007h |
| RAM Control (see 表 6-49) | 0158h | 000h–001h |
| Watchdog (see 表 6-50) | 015Ch | 000h–001h |
| UCS (see 表 6-51) | 0160h | 000h–01Fh |
| SYS (see 表 6-52) | 0180h | 000h–01Fh |
| Shared Reference (see 表 6-53) | 01B0h | 000h–001h |
| Port Mapping Control (see 表 6-54) | 01C0h | 000h–007h |
| Port Mapping Port P1 (see 表 6-55) | 01C8h | 000h–007h |
| Port Mapping Port P2 (see 表 6-56) | 01D0h | 000h–007h |
| Port Mapping Port P3 (see 表 6-57) | 01D8h | 000h–007h |
| Port P1, P2 (see 表 6-58) | 0200h | 000h–01Fh |
| Port P3, P4 (see 表 6-59) | 0220h | 000h–00Bh |
| Port P5, P6 (see 表 6-60) | 0240h | 000h–00Bh |
| Port P7, P8 (see 表 6-61) (Port P7, P8 not available in MSP430F67xxAIPN) | 0260h | 000h–00Bh |
| Port P9 (Port P9 not available in MSP430F67xxAIPN) (see 表 6-62) | 0280h | 000h–00Bh |
| Port PJ (refer to 表 6-63) | 0320h | 000h–01Fh |
| Timer TA0 (see 表 6-64) | 0340h | 000h–03Fh |
| Timer TA1 (see 表 6-65) | 0380h | 000h–03Fh |
| Timer TA2 (see 表 6-66) | 0400h | 000h–03Fh |
| Timer TA3 (see 表 6-67) | 0440h | 000h–03Fh |
| Backup Memory (see 表 6-68) | 0480h | 000h–00Fh |
| RTC_C (see 表 6-69) | 04A0h | 000h–01Fh |
| 32-Bit Hardware Multiplier (see 表 6-70) | 04C0h | 000h–02Fh |
| DMA General Control (see 表 6-71) | 0500h | 000h–00Fh |
| DMA Channel 0 (see 表 6-72) | 0500h | 010h–01Fh |
| DMA Channel 1 (see 表 6-73) | 0500h | 020h–02Fh |
| DMA Channel 2 (see 表 6-74) | 0500h | 030h–03Fh |
| eUSCI_A0 (see 表 6-75) | 05C0h | 000h–01Fh |
| eUSCI_A1 (see 表 6-76) | 05E0h | 000h–01Fh |
| eUSCI_A2 (see 表 6-77) | 0600h | 000h–01Fh |
| eUSCI_B0 (see 表 6-78) | 0640h | 000h–02Fh |
| ADC10_A (see 表 6-79) | 0740h | 000h–01Fh |
| SD24_B (see 表 6-80) | 0800h | 000h–06Fh |
| Auxiliary Supply (see 表 6-74) | 09E0h | 000h–01Fh |
| LCD_C (see 表 6-82) | 0A00h | 000h–05Fh |

表 6-45. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

表 6-46. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| PMM control 0 | PMMCTL0 | 00h |
| PMM control 1 | PMMCTL1 | 02h |
| SVS high-side control | SVSMHCTL | 04h |
| SVS low-side control | SVSMLCTL | 06h |
| PMM interrupt flags | PMMIFG | 0Ch |
| PMM interrupt enable | PMMIE | 0Eh |
| PMM power mode 5 control 0 | PM5CTL0 | 10h |

表 6-47. Flash Control Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Flash control 1 | FCTL1 | 00h |
| Flash control 3 | FCTL3 | 04h |
| Flash control 4 | FCTL4 | 06h |

表 6-48. CRC16 Registers (Base Address: 0150h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRC16DIRB | 02h |
| CRC result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

表 6-49. RAM Control Registers (Base Address: 0158h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RAM control 0 | RCCTL0 | 00h |

表 6-50. Watchdog Registers (Base Address: 015Ch)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

表 6-51. UCS Registers (Base Address: 0160h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 0 | UCSCTL0 | 00h |
| UCS control 1 | UCSCTL1 | 02h |
| UCS control 2 | UCSCTL2 | 04h |
| UCS control 3 | UCSCTL3 | 06h |
| UCS control 4 | UCSCTL4 | 08h |
| UCS control 5 | UCSCTL5 | 0Ah |
| UCS control 6 | UCSCTL6 | 0Ch |
| UCS control 7 | UCSCTL7 | 0Eh |

表 6-51. UCS Registers (Base Address: 0160h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| UCS control 8 | UCSCTL8 | 10h |

表 6-52. SYS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-----------|--------|
| System control | SYSCTL | 00h |
| Bootloader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |

表 6-53. Shared Reference Registers (Base Address: 01B0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------|----------|--------|
| Shared reference control | REFCTL | 00h |

表 6-54. Port Mapping Controller (Base Address: 01C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| Port mapping password | PMAPPWD | 00h |
| Port mapping control | PMAPCTL | 02h |

表 6-55. Port Mapping for Port P1 (Base Address: 01C8h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Port P1.0 mapping | P1MAP0 | 00h |
| Port P1.1 mapping | P1MAP1 | 01h |
| Port P1.2 mapping | P1MAP2 | 02h |
| Port P1.3 mapping | P1MAP3 | 03h |
| Port P1.4 mapping | P1MAP4 | 04h |
| Port P1.5 mapping | P1MAP5 | 05h |
| Port P1.6 mapping | P1MAP6 | 06h |
| Port P1.7 mapping | P1MAP7 | 07h |

表 6-56. Port Mapping for Port P2 (Base Address: 01D0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Port P2.0 mapping | P2MAP0 | 00h |
| Port P2.1 mapping | P2MAP2 | 01h |
| Port P2.2 mapping | P2MAP2 | 02h |
| Port P2.3 mapping | P2MAP3 | 03h |
| Port P2.4 mapping | P2MAP4 | 04h |
| Port P2.5 mapping | P2MAP5 | 05h |
| Port P2.6 mapping | P2MAP6 | 06h |
| Port P2.7 mapping | P2MAP7 | 07h |

表 6-57. Port Mapping for Port P3 (Base Address: 01D8h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Port P3.0 mapping | P3MAP0 | 00h |
| Port P3.1 mapping | P3MAP3 | 01h |
| Port P3.2 mapping | P3MAP2 | 02h |
| Port P3.3 mapping | P3MAP3 | 03h |
| Port P3.4 mapping | P3MAP4 | 04h |
| Port P3.5 mapping | P3MAP5 | 05h |
| Port P3.6 mapping | P3MAP6 | 06h |
| Port P3.7 mapping | P3MAP7 | 07h |

表 6-58. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 resistor enable | P1REN | 06h |
| Port P1 drive strength | P1DS | 08h |
| Port P1 selection | P1SEL | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 resistor enable | P2REN | 07h |
| Port P2 drive strength | P2DS | 09h |
| Port P2 selection | P2SEL | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

表 6-59. Port P3, P4 Registers (Base Address: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 resistor enable | P3REN | 06h |
| Port P3 drive strength | P3DS | 08h |
| Port P3 selection | P3SEL | 0Ah |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 resistor enable | P4REN | 07h |
| Port P4 drive strength | P4DS | 09h |
| Port P4 selection | P4SEL | 0Bh |

表 6-60. Port P5, P6 Registers (Base Address: 0240h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 resistor enable | P5REN | 06h |
| Port P5 drive strength | P5DS | 08h |
| Port P5 selection | P5SEL | 0Ah |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 resistor enable | P6REN | 07h |
| Port P6 drive strength | P6DS | 09h |
| Port P6 selection | P6SEL | 0Bh |

表 6-61. Port P7, P8 Registers (Base Address: 0260h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 resistor enable | P7REN | 06h |
| Port P7 drive strength | P7DS | 08h |
| Port P7 selection | P7SEL | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 resistor enable | P8REN | 07h |
| Port P8 drive strength | P8DS | 09h |
| Port P8 selection | P8SEL | 0Bh |

表 6-62. Port P9 Registers (Base Address: 0280h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port P9 input | P9IN | 00h |
| Port P9 output | P9OUT | 02h |
| Port P9 direction | P9DIR | 04h |
| Port P9 resistor enable | P9REN | 06h |
| Port P9 drive strength | P9DS | 08h |
| Port P9 selection | P9SEL | 0Ah |

表 6-63. Port J Registers (Base Address: 0320h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------|----------|--------|
| Port PJ input | PJIN | 00h |
| Port PJ output | PJOUT | 02h |
| Port PJ direction | PJDIR | 04h |
| Port PJ resistor enable | PJREN | 06h |
| Port PJ drive strength | PJDS | 08h |
| Port PJ selection | PJSEL | 0Ah |

表 6-64. TA0 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter | TA0R | 10h |
| Capture/compare 0 | TA0CCR0 | 12h |
| Capture/compare 1 | TA0CCR1 | 14h |
| Capture/compare 2 | TA0CCR2 | 16h |
| TA0 expansion 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

表 6-65. TA1 Registers (Base Address: 0380h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| TA1 counter | TA1R | 10h |
| Capture/compare 0 | TA1CCR0 | 12h |
| Capture/compare 1 | TA1CCR1 | 14h |
| TA1 expansion 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

表 6-66. TA2 Registers (Base Address: 0400h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA2 control | TA2CTL | 00h |
| Capture/compare control 0 | TA2CCTL0 | 02h |
| Capture/compare control 1 | TA2CCTL1 | 04h |
| TA2 counter | TA2R | 10h |
| Capture/compare 0 | TA2CCR0 | 12h |
| Capture/compare 1 | TA2CCR1 | 14h |
| TA2 expansion 0 | TA2EX0 | 20h |
| TA2 interrupt vector | TA2IV | 2Eh |

表 6-67. TA3 Registers (Base Address: 0440h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---------------------------|----------|--------|
| TA3 control | TA3CTL | 00h |
| Capture/compare control 0 | TA3CCTL0 | 02h |
| Capture/compare control 1 | TA3CCTL1 | 04h |
| TA3 counter | TA3R | 10h |
| Capture/compare 0 | TA3CCR0 | 12h |
| Capture/compare 1 | TA3CCR1 | 14h |
| TA3 expansion 0 | TA3EX0 | 20h |
| TA3 interrupt vector | TA3IV | 2Eh |

表 6-68. Backup Memory Registers (Base Address: 0480h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Backup memory 0 | BAKMEM0 | 00h |
| Backup memory 1 | BAKMEM1 | 02h |
| Backup memory 2 | BAKMEM2 | 04h |
| Backup memory 3 | BAKMEM3 | 06h |

表 6-69. RTC_C Registers (Base Address: 04A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------|-----------|--------|
| RTC control 0 | RTCCTL0 | 00h |
| RTC password | RTCPWD | 01h |
| RTC control 1 | RTCCTL1 | 02h |
| RTC control 3 | RTCCTL3 | 03h |
| RTC offset calibration | RTCOCAL | 04h |
| RTC temperature compensation | RTCTCMP | 06h |
| RTC prescaler 0 control | RTCPS0CTL | 08h |
| RTC prescaler 1 control | RTCPS1CTL | 0Ah |
| RTC prescaler 0 | RTCPS0 | 0Ch |
| RTC prescaler 1 | RTCPS1 | 0Dh |
| RTC interrupt vector word | RTCIV | 0Eh |
| RTC seconds | RTCSEC | 10h |
| RTC minutes | RTCMIN | 11h |
| RTC hours | RTCHOUR | 12h |
| RTC day of week | RTCDOW | 13h |
| RTC days | RTCDAY | 14h |
| RTC month | RTCMON | 15h |
| RTC year | RTCYEAR | 16h |
| RTC alarm minutes | RTCAMIN | 18h |
| RTC alarm hours | RTCAHOUR | 19h |
| RTC alarm day of week | RTCADOW | 1Ah |
| RTC alarm days | RTCADAY | 1Bh |
| Binary-to-BCD conversion | BIN2BCD | 1Ch |
| BCD-to-binary conversion | BCD2BIN | 1Eh |

表 6-70. 32-Bit Hardware Multiplier Registers (Base Address: 04C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| 16-bit operand 1 – multiply | MPY | 00h |
| 16-bit operand 1 – signed multiply | MPYS | 02h |
| 16-bit operand 1 – multiply accumulate | MAC | 04h |
| 16-bit operand 1 – signed multiply accumulate | MACS | 06h |
| 16-bit operand 2 | OP2 | 08h |
| 16 × 16 result low word | RESLO | 0Ah |
| 16 × 16 result high word | RESHI | 0Ch |
| 16 × 16 sum extension | SUMEXT | 0Eh |
| 32-bit operand 1 – multiply low word | MPY32L | 10h |
| 32-bit operand 1 – multiply high word | MPY32H | 12h |
| 32-bit operand 1 – signed multiply low word | MPYS32L | 14h |
| 32-bit operand 1 – signed multiply high word | MPYS32H | 16h |
| 32-bit operand 1 – multiply accumulate low word | MAC32L | 18h |
| 32-bit operand 1 – multiply accumulate high word | MAC32H | 1Ah |
| 32-bit operand 1 – signed multiply accumulate low word | MACS32L | 1Ch |
| 32-bit operand 1 – signed multiply accumulate high word | MACS32H | 1Eh |
| 32-bit operand 2 – low word | OP2L | 20h |
| 32-bit operand 2 – high word | OP2H | 22h |
| 32 × 32 result 0 – least significant word | RES0 | 24h |
| 32 × 32 result 1 | RES1 | 26h |
| 32 × 32 result 2 | RES2 | 28h |
| 32 × 32 result 3 – most significant word | RES3 | 2Ah |
| MPY32 control 0 | MPY32CTL0 | 2Ch |

表 6-71. DMA General Control Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| DMA module control 0 | DMACTL0 | 00h |
| DMA module control 1 | DMACTL1 | 02h |
| DMA module control 2 | DMACTL2 | 04h |
| DMA module control 3 | DMACTL3 | 06h |
| DMA module control 4 | DMACTL4 | 08h |
| DMA interrupt vector | DMAIV | 0Eh |

表 6-72. DMA Channel 0 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 0 control | DMA0CTL | 10h |
| DMA channel 0 source address low | DMA0SAL | 12h |
| DMA channel 0 source address high | DMA0SAH | 14h |
| DMA channel 0 destination address low | DMA0DAL | 16h |
| DMA channel 0 destination address high | DMA0DAH | 18h |
| DMA channel 0 transfer size | DMA0SZ | 1Ah |

表 6-73. DMA Channel 1 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 1 control | DMA1CTL | 20h |
| DMA channel 1 source address low | DMA1SAL | 22h |
| DMA channel 1 source address high | DMA1SAH | 24h |
| DMA channel 1 destination address low | DMA1DAL | 26h |
| DMA channel 1 destination address high | DMA1DAH | 28h |
| DMA channel 1 transfer size | DMA1SZ | 2Ah |

表 6-74. DMA Channel 2 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| DMA channel 2 control | DMA2CTL | 30h |
| DMA channel 2 source address low | DMA2SAL | 32h |
| DMA channel 2 source address high | DMA2SAH | 34h |
| DMA channel 2 destination address low | DMA2DAL | 36h |
| DMA channel 2 destination address high | DMA2DAH | 38h |
| DMA channel 2 transfer size | DMA2SZ | 3Ah |

表 6-75. eUSCI_A0 Registers (Base Address: 05C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI_A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA0BR0 | 06h |
| eUSCI_A baud rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |

表 6-76. eUSCI_A1 Registers (Base Address:05E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0 | UCA1CTLW0 | 00h |
| eUSCI_A control word 1 | UCA1CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA1BR0 | 06h |
| eUSCI_A baud rate 1 | UCA1BR1 | 07h |
| eUSCI_A modulation control | UCA1MCTLW | 08h |
| eUSCI_A status | UCA1STAT | 0Ah |
| eUSCI_A receive buffer | UCA1RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA1TXBUF | 0Eh |
| eUSCI_A LIN control | UCA1ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA1IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA1IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA1IE | 1Ah |
| eUSCI_A interrupt flags | UCA1IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA1IV | 1Eh |

表 6-77. eUSCI_A2 Registers (Base Address:0600h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|------------|--------|
| eUSCI_A control word 0 | UCA2CTLW0 | 00h |
| eUSCI_A control word 1 | UCA2CTLW1 | 02h |
| eUSCI_A baud rate 0 | UCA2BR0 | 06h |
| eUSCI_A baud rate 1 | UCA2BR1 | 07h |
| eUSCI_A modulation control | UCA2MCTLW | 08h |
| eUSCI_A status | UCA2STAT | 0Ah |
| eUSCI_A receive buffer | UCA2RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA2TXBUF | 0Eh |
| eUSCI_A LIN control | UCA2ABCTL | 10h |
| eUSCI_A IrDA transmit control | UCA2IRTCTL | 12h |
| eUSCI_A IrDA receive control | UCA2IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA2IE | 1Ah |
| eUSCI_A interrupt flags | UCA2IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA2IV | 1Eh |

表 6-78. eUSCI_B0 Registers (Base Address: 0640h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B received address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI I2C slave address | UCB0I2CSA | 20h |
| eUSCI interrupt enable | UCB0IE | 2Ah |
| eUSCI interrupt flags | UCB0IFG | 2Ch |
| eUSCI interrupt vector word | UCB0IV | 2Eh |

表 6-79. ADC10_A Registers (Base Address: 0740h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|------------|--------|
| ADC10_A control 0 | ADC10CTL0 | 00h |
| ADC10_A control 1 | ADC10CTL1 | 02h |
| ADC10_A control 2 | ADC10CTL2 | 04h |
| ADC10_A window comparator low threshold | ADC10LO | 06h |
| ADC10_A window comparator high threshold | ADC10HI | 08h |
| ADC10_A memory control 0 | ADC10MCTL0 | 0Ah |
| ADC10_A conversion memory | ADC10MCTL0 | 12h |
| ADC10_A interrupt enable | ADC10IE | 1Ah |
| ADC10_A interrupt flags | ADC10IGH | 1Ch |
| ADC10_A interrupt vector word | ADC10IV | 1Eh |

表 6-80. SD24_B Registers (Base Address: 0800h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|-------------|--------|
| SD24_B control 0 | SD24BCTL0 | 00h |
| SD24_B control 1 | SD24BCTL1 | 02h |
| SD24_B interrupt flag | SD24BIFG | 0Ah |
| SD24_B interrupt enable | SD24BIE | 0Ch |
| SD24_B interrupt vector | SD24BIV | 0Eh |
| SD24_B converter 0 control | SD24BCCTL0 | 10h |
| SD24_B converter 0 input control | SD24BINCTL0 | 12h |
| SD24_B converter 0 OSR control | SD24BOSR0 | 14h |
| SD24_B converter 0 preload | SD24BPRE0 | 16h |
| SD24_B converter 1 control | SD24BCCTL1 | 18h |
| SD24_B converter 1 input control | SD24BINCTL1 | 1Ah |
| SD24_B converter 1 OSR control | SD24BOSR1 | 1Ch |
| SD24_B converter 1 preload | SD24BPRE1 | 1Eh |
| SD24_B converter 2 control | SD24BCCTL2 | 20h |
| SD24_B converter 2 input control | SD24BINCTL2 | 22h |
| SD24_B converter 2 OSR control | SD24BOSR2 | 24h |
| SD24_B converter 2 preload | SD24BPRE2 | 26h |
| SD24_B converter 0 conversion memory low word | SD24BMEML0 | 50h |
| SD24_B converter 0 conversion memory high word | SD24BMEMH0 | 52h |
| SD24_B converter 1 conversion memory low word | SD24BMEML1 | 54h |
| SD24_B converter 1 conversion memory high word | SD24BMEMH1 | 56h |
| SD24_B converter 2 conversion memory low word | SD24BMEML2 | 58h |
| SD24_B converter 2 conversion memory high word | SD24BMEMH2 | 5Ah |

表 6-81. Auxiliary Supplies Registers (Base Address: 09E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|-----------|--------|
| Auxiliary supply control 0 | AUXCTL0 | 00h |
| Auxiliary supply control 1 | AUXCTL1 | 02h |
| Auxiliary supply control 2 | AUXCTL2 | 04h |
| AUX2 charger control | AUX2CHCTL | 12h |
| AUX3 charger control | AUX3CHCTL | 14h |
| AUX ADC control | AUXADCCTL | 16h |
| AUX interrupt flag | AUXIFG | 1Ah |
| AUX interrupt enable | AUXIE | 1Ch |
| AUX interrupt vector word | AUXIV | 1Eh |

表 6-82. LCD_C Registers (Base Address: 0A00h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|------------|--------|
| LCD_C control 0 | LCDCCTL0 | 000h |
| LCD_C control 1 | LCDCCTL1 | 002h |
| LCD_C blinking control | LCDCBLKCTL | 004h |
| LCD_C memory control | LCDCMEMCTL | 006h |
| LCD_C voltage control | LCDCVCTL | 008h |
| LCD_C port control 0 | LCDCPCTL0 | 00Ah |
| LCD_C port control 1 | LCDCPCTL1 | 00Ch |
| LCD_C port control 2 | LCDCPCTL2 | 00Eh |
| LCD_C charge pump control | LCDCCPCTL | 012h |
| LCD_C interrupt vector | LCDCIV | 01Eh |
| Static and 2 to 4 mux modes | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_C memory 20 | LCDM20 | 033h |
| LCD_C blinking memory 1 | LCDBM1 | 040h |
| LCD_C blinking memory 2 | LCDBM2 | 041h |
| ⋮ | ⋮ | ⋮ |
| LCD_C blinking memory 20 | LCDBM20 | 053h |
| 5 to 8 mux modes | | |
| LCD_C memory 1 | LCDM1 | 020h |
| LCD_C memory 2 | LCDM2 | 021h |
| ⋮ | ⋮ | ⋮ |
| LCD_C memory 40 | LCDM40 | 047h |

6.15 Identification

6.15.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [节 8.4](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in [节 6.13](#).

6.15.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata sheet describes these markings. For links to all of the errata sheets for the devices in this data sheet, see [节 8.4](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in [节 6.13](#).

6.15.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the [MSP430 Programming With the JTAG Interface](#).

7 Applications, Implementation, and Layout

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The following resources provide application guidelines and best practices when designing with the MSP430F673xA and MSP430F672xA.

Implementation of a Single-Phase Electronic Watt-Hour Meter Using the MSP430F6736(A)

This application report describes the implementation of a single-phase electronic electricity meter using the Texas Instruments MSP430F673x(A) metering processor. It also includes the necessary information with regard to metrology software and hardware procedures for this single-chip implementation.

High-Accuracy Single-Phase Electricity Meter With Tamper Detection

This design, featuring the MSP430F6736(A) device, implements a highly-integrated single-chip electricity metering (e-meter) solution. Hardware and software design files are provided to enable calculation of various parameters for single phase energy measurement, such as RMS current and voltage, active and reactive power and energies, power factor, and frequency.

Features

- Low-power single-phase e-metering implementation
- Calculate parameters such as RMS current and voltage, active and reactive power and energies, power factor and frequency
- Based on the highly-integrated MSP430F67xx(A) family of metering-focused MCU SoCs
- Segment LCD is also implemented in this design
- RF modules can also be added to this design to enable unique connectivity solutions.

8 器件和文档支持

8.1 入门和后续步骤

要获得有助于您开发工作的 MSP430™ 系列器件、工具和库的更多相关信息，请访问 [入门](#) 页面。

8.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. [图 8-1](#) provides a legend for reading the complete device name.

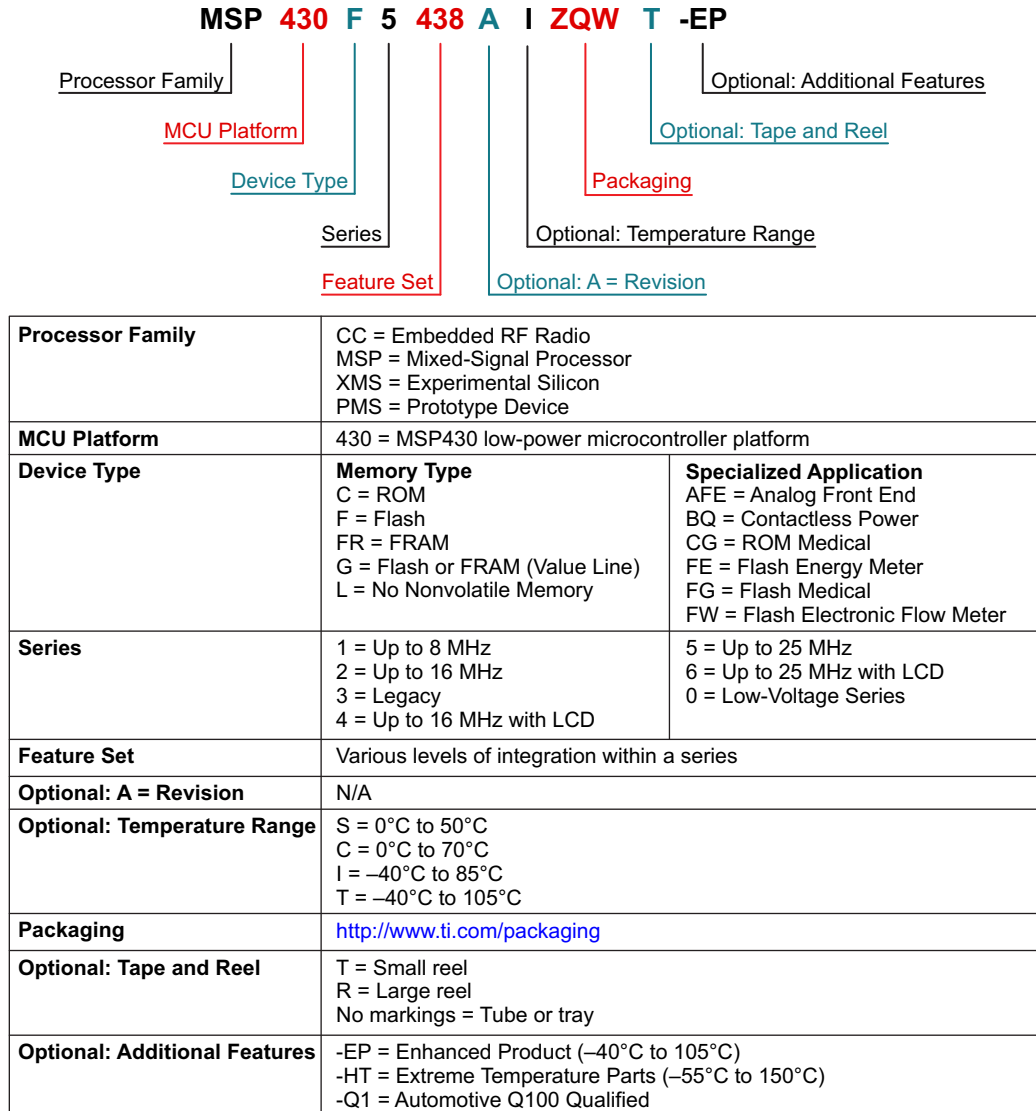


图 8-1. Device Nomenclature

8.3 工具与软件

所有 MSP 微控制器均受多种软件和硬件开发工具的支持。相关工具由 TI 以及多家第三方供应商提供。请参阅《MSP430 超低功耗 MCU – 工具与软件》了解所有工具。

表 8-1 列出了 MSP430F673xA 和 MSP430F672xA MCU 的调试特性。关于可用特性的详细信息，请参见《适用于 MSP430 的 Code Composer Studio 用户指南》。

表 8-1. 硬件调试 特性

| MSP430 架构 | 四线制 JTAG | 两线制 JTAG | 断点 (N) | 范围断点 | 时钟控制 | 状态序列发生器 | 跟踪缓冲器 | LPMx.5 调试支持 |
|-----------|----------|----------|--------|------|------|---------|-------|-------------|
| MSP430Xv2 | 有 | 有 | 3 | 有 | 是 | 否 | 否 | 否 |

设计套件与评估模块

MSP-TS430PZ100B - 适用于 MSP430F6x MCU 的 100 引脚目标开发板 MSP-TS430PZ100B 是一款独立的 100 引脚 ZIF 插座目标板，用于通过 JTAG 接口或 Spy-Bi-Wire（两线制 JTAG）协议在系统内对 MSP430 MCU 进行编程和调试。

适用于 MSP430F6x MCU 的 100 引脚目标开发板和 MSP-FET 编程器捆绑包 MSP-FET 是一款强大的闪存仿真工具，可在 MSP430 MCU 上快速开始应用开发。它包含 USB 调试接口，用于通过 JTAG 接口或节省引脚的 Spy-Bi-Wire（两线制 JTAG）协议在系统内对 MSP430 进行编程和调试。

EVM430-F6736 - 用于计量的 MSP430F6736 EVM EVM430-F6736 是一个基于 MSP430F6736 器件的单相电表评估模块。该电表不仅可连接至主电力线，而且还具备电压和电流输入，以及可用于防篡改设置的第三连接系统。

软件

MSP430Ware™ 软件 MSP430Ware 软件集合了所有 MSP430 器件的代码示例、数据表以及其他设计资源，打包提供给用户。除了提供已有 MSP430 设计资源的完整集合外，MSP430Ware 软件还包含名为 MSP 驱动程序库的高级 API。借助该库可以轻松地对 MSP430 硬件进行编程。MSP430Ware 软件以 CCS 组件或独立软件包两种形式提供。

适用于 MSP430 MCU 的能量测量设计中心 能量测量设计中心是一款快速开发工具，它使用 TI MSP430i20xx 和 MSP430F67xx 基于闪存的微控制器 (MCU) 实现能量测量。它包含能够在各种电源监控和能量测量应用（包括智能电网和楼宇自动化）中简化开发和加快设计的图形用户界面 (GUI)、文档、软件库和示例。使用该设计中心，您无需编写任何代码即可配置、校准并查看结果。

MSP 驱动程序库 MSP 驱动程序库的抽象 API 提供易用的函数调用，无需直接操纵 MSP430 硬件的位与字节。完整的文档通过具有帮助意义的 API 指南交付，其中包括有关每个函数调用和经过验证的参数的详细信息。开发人员可使用驱动程序库函数以尽可能低的费用编写全部项目。

IEC60730 软件包 IEC60730 MSP430 软件包经过专门开发，用于协助客户达到 IEC 60730-1:2010（家用及类似用途的自动化电气控制 - 第 1 部分：一般要求）B 类产品的要求。其中涵盖家用电器、电弧检测器、电源转换器、电动工具、电动自行车及其他诸多产品。IEC60730 MSP430 软件包可以嵌入在 MSP430 MCU 中运行的客户应用，从而帮助客户简化其消费类器件在功能安全方面遵循 IEC 60730-1:2010 B 类规范的认证工作。

MSP430F673xA、MSP430F672xA 代码示例 根据不同应用需求配置各集成外设的每个 MSP 器件均具备相应的 C 代码示例。

电容式触摸软件库 可在 MSP430 MCU 启用电容触控功能的免费 C 代码库。MSP430 MCU 库版本采用多种电容触控实现方法，包括 RO 和 RC 方法。

MSP EnergyTrace™ 技术 适用于 MSP430 微控制器的 EnergyTrace 技术是基于电能的代码分析工具，适用于测量和显示应用的电能系统配置并帮助优化应用以实现超低功耗。

ULP (超低功耗) Advisor ULP Advisor™ 软件是一款辅助工具，旨在指导开发人员编写更为高效的代码，从而充分利用 MSP430 和 MSP432 微控制器独特功能。ULP Advisor 的目标人群是微控制器的资深开发者和开发新手，可以根据详尽的 ULP 检验表检查代码，以便最大限度地减少应用程序的能耗。在编译时，ULP Advisor 会提供通知和备注以突出显示代码中可以进一步优化的区域，进而实现更低功耗。

适用于 MSP 的定点数学库 MSP IQmath 和 Qmath 库是为 C 语言开发者提供的一套经过高度优化的高精度数学运算函数集合，能够将浮点算法无缝嵌入 MSP430 和 MSP432 器件的定点代码中。这些例程通常用于计算密集型实时应用，而优化的执行速度、高精度以及超低能耗通常是影响这些实时应用的关键因素。与使用浮点数学算法编写的同等代码相比，使用 IQmath 和 Qmath 库可以大幅提高执行速度并显著降低能耗。

适用于 MSP430 的浮点数学运算库 TI 在低功耗和低成本微控制器领域锐意创新，为您提供 MSPMATHLIB。此标量函数的浮点数学运算库，能够充分利用器件的智能外设，使速度最高达到标准 MSP430 数学函数的 26 倍。Mathlib 能够轻松集成到您的设计中。该运算库免费使用并集成在 Code Composer Studio IDE 和 IAR Embedded Workbench IDE 中。

开发工具

适用于 MSP 微控制器的 Code Composer Studio™ 集成开发环境 Code Composer Studio (CCS) 集成开发环境 (IDE) 支持所有 MSP 微控制器器件。CCS 包含一整套用于开发和调试嵌入式应用的工具。它包含了优化的 C/C++ 编译器、源代码编辑器、项目构建环境、调试器、描述器以及其他多种功能。

命令行编程器 MSP Flasher 是一款基于 shell 的开源接口，可使用 JTAG 或 Spy-Bi-Wire (SBW) 通信通过 FET 编程器或 eZ430 对 MSP 微控制器进行编程。MSP Flasher 可用于将二进制文件 (.txt 或 .hex 文件) 直接下载到 MSP 微控制器，而无需使用 IDE。

MSP MCU 编程器和调试器 MSP-FET 是一款强大的仿真开发工具 (通常称为调试探针)，可帮助用户在 MSP 低功耗微控制器 (MCU) 中快速开发应用。创建 MCU 软件通常需要将生成的二进制程序下载到 MSP 器件中，从而进行验证和调试。

MSP-GANG 生产编程器 MSP Gang 编程器是一款 MSP430 或 MSP432 器件编程器，可同时对多达八个完全相同的 MSP430 或 MSP432 闪存或 FRAM 器件进行编程。MSP Gang 编程器可使用标准的 RS-232 或 USB 连接与主机 PC 相连并提供灵活的编程选项，允许用户完全自定义流程。

8.4 文档支持

以下文档对 MSP430F673xA 和 MSP430F672xA MCU 进行了介绍。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括器件勘误表），请转至 ti.com.cn 上相关器件的产品文件夹（请参阅节 8.5 提供的链接）。请单击右上角的“通知我”按钮。点击注册后，即可收到产品信息更改每周摘要（如有）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

- 《[MSP430F6736A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6735A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6734A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6733A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6731A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6730A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6726A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6725A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6724A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6723A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6721A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。
- 《[MSP430F6720A 器件勘误表](#)》 说明了功能技术规格的已知例外情况。

用户指南

- 《[MSP430x5xx 和 MSP430x6xx 系列用户指南](#)》 详细介绍了该器件系列提供的模块和外设。
- 《[MSP430™ 闪存器件引导加载程序 \(BSL\) 用户指南](#)》 MSP430 引导加载程序 (BSL) 允许用户在原型设计、投产和维护等各阶段与 MSP430 微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器 (RAM) 可根据相关要求进行变更。不要将此处的引导加载程序与某些数字信号处理器 (DSP) 中将外部存储器中的程序代码（和数据）自动加载到 DSP 内部存储器的引导装载程序混为一谈。
- 《[通过 JTAG 接口对 MSP430 进行编程](#)》 此文档介绍了使用 JTAG 通信端口擦除、编程和验证基于 MSP430 闪存和 FRAM 的微控制器系列的存储器模块所需的功能。此外，该文档还介绍了如何编程所有 MSP430 器件上均具备的 JTAG 访问安全保险丝。此文档介绍了使用标准四线制 JTAG 接口和两线制 JTAG 接口（也称为 Spy-Bi-Wire (SBW)）的器件访问。
- 《[MSP430 硬件工具用户指南](#)》 此手册介绍了 TI MSP-FET430 闪存仿真工具 (FET) 的硬件。FET 是针对 MSP430 超低功耗微控制器的程序开发工具。文中对提供的接口类型，即并行端口接口和 USB 接口进行了说明。

应用报告

- 《使用 **MSP430F6736(A)** 实施单相电子电表》 该应用报告介绍了如何使用德州仪器 (TI) MSP430F673x(A) 计量处理器实现单相电子电表。它还包含有关此单芯片实现的计量软件和硬件程序的必要信息。
- 《**MSP430F67xx** 与 **MSP430F67xxA** 器件之间的差异》 该应用报告介绍了 MSP430F67xxA 器件在非 A MSP430F67xx 器件基础上实现的增强功能。该应用报告介绍了在 MSP430F67xxA 中修复的 MSP430F67xx 勘误表以及向 MSP430F67xxA 器件添加的其他功能。此外，还比较了计量结果，以进一步展示 MSP430F67xxA 器件中实现的更改不会影响计量性能。
- 《**MSP430 32kHz** 晶体振荡器》 对于稳定的晶体振荡器，选择合适的晶振、正确的负载电路和适当的电路板布局布线至关重要。该应用报告总结了晶体振荡器的功能，介绍了用于选择合适的晶体以实现 MSP430 超低功耗运行的参数。此外，还给出了正确电路板布局的提示和示例。此外，为了确保振荡器在大规模生产后能够稳定运行，还可能需要进行一些振荡器测试，该文档中提供了有关这些测试的详细信息。
- 《**MSP430 系统级 ESD 注意事项**》 随着硅晶技术向更低电压方向发展以及设计具有成本效益的超低功耗组件的需求的出现，系统级 ESD 要求变得越来越苛刻。该应用报告介绍了三个不同的 ESD 主题，旨在帮助电路板设计人员和 OEM 理解并设计出稳健耐用的系统级设计。
- 《使用 **MSP430** 和段式 **LCD** 进行设计》 从智能电表，到电子货架标签 (ESL)，再到医疗设备，各式各样的应用 都需要使用段式液晶显示屏 (LCD) 为用户 提供相关信息。部分 MSP430™ 微控制器系列内置低功耗 LCD 驱动电路，MSP430 MCU 借此能够直接控制段式 LCD 玻璃。本应用手册可帮助您理解段式 LCD 的工作原理、MSP430 MCU 系列各种 LCD 模块的不同特性，并提供了 LCD 硬件布线技巧、编写高效易用的 LCD 驱动软件的相关指导以及 具有不同 LCD 特性的 MSP430 器件的 产品组合概述， 旨在协助您进行器件选型。

8.5 相关链接

表 8-2 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

表 8-2. 相关链接

| 器件 | 产品文件夹 | 立即订购 | 技术文档 | 工具与软件 | 支持和社区 |
|--------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| MSP430F6736A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6735A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6734A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6733A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6731A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6730A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6726A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6725A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6724A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6723A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6721A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |
| MSP430F6720A | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 | 请单击此处 |

8.6 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参见 TI 的《使用条款》。

TI E2E™ 社区

TI 的工程师交流 (E2E) 社区。此社区的创建目的是为了促进工程师之间协作。在 e2e.ti.com 中，您可以提问、共享知识、拓展思路，在同领域工程师的帮助下解决问题。

TI 嵌入式处理器维基网页

德州仪器 (TI) 嵌入式处理器维基网页。此网站的建立是为了帮助开发人员熟悉德州仪器 (TI) 的嵌入式处理器，并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

8.7 商标

MSP430, MSP430Ware, EnergyTrace, ULP Advisor, 适用于 MSP 微控制器的 Code Composer Studio, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

8.8 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

8.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F6720AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6720A | Samples |
| MSP430F6720AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6720A | Samples |
| MSP430F6720AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6720A | Samples |
| MSP430F6720AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6720A | Samples |
| MSP430F6721AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6721A | Samples |
| MSP430F6721AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6721A | Samples |
| MSP430F6721AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6721A | Samples |
| MSP430F6721AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6721A | Samples |
| MSP430F6723AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723A | Samples |
| MSP430F6723AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723A | Samples |
| MSP430F6723AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723A | Samples |
| MSP430F6723AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6723A | Samples |
| MSP430F6724AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6724A | Samples |
| MSP430F6724AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6724A | Samples |
| MSP430F6724AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6724A | Samples |
| MSP430F6724AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6724A | Samples |
| MSP430F6725AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6725A | Samples |
| MSP430F6725AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6725A | Samples |
| MSP430F6725AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6725A | Samples |
| MSP430F6725AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6725A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F6726AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6726A | Samples |
| MSP430F6726AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6726A | Samples |
| MSP430F6726AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6726A | Samples |
| MSP430F6726AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6726A | Samples |
| MSP430F6730AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6730A | Samples |
| MSP430F6730AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6730A | Samples |
| MSP430F6730AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6730A | Samples |
| MSP430F6730AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6730A | Samples |
| MSP430F6731AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6731A | Samples |
| MSP430F6731AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6731A | Samples |
| MSP430F6731AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6731A | Samples |
| MSP430F6731AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6731A | Samples |
| MSP430F6733AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6733A | Samples |
| MSP430F6733AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6733A | Samples |
| MSP430F6733AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6733A | Samples |
| MSP430F6733AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6733A | Samples |
| MSP430F6734AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6734A | Samples |
| MSP430F6734AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6734A | Samples |
| MSP430F6734AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6734A | Samples |
| MSP430F6734AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6734A | Samples |
| MSP430F6735AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6735A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| MSP430F6735AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6735A | Samples |
| MSP430F6735AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6735A | Samples |
| MSP430F6735AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6735A | Samples |
| MSP430F6736AIPN | ACTIVE | LQFP | PN | 80 | 119 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6736A | Samples |
| MSP430F6736AIPNR | ACTIVE | LQFP | PN | 80 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6736A | Samples |
| MSP430F6736AIPZ | ACTIVE | LQFP | PZ | 100 | 90 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6736A | Samples |
| MSP430F6736AIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | F6736A | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F6720AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6720AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6721AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6721AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6723AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6723AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6724AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6724AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6725AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6725AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6726AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6726AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6730AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6730AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6731AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6731AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

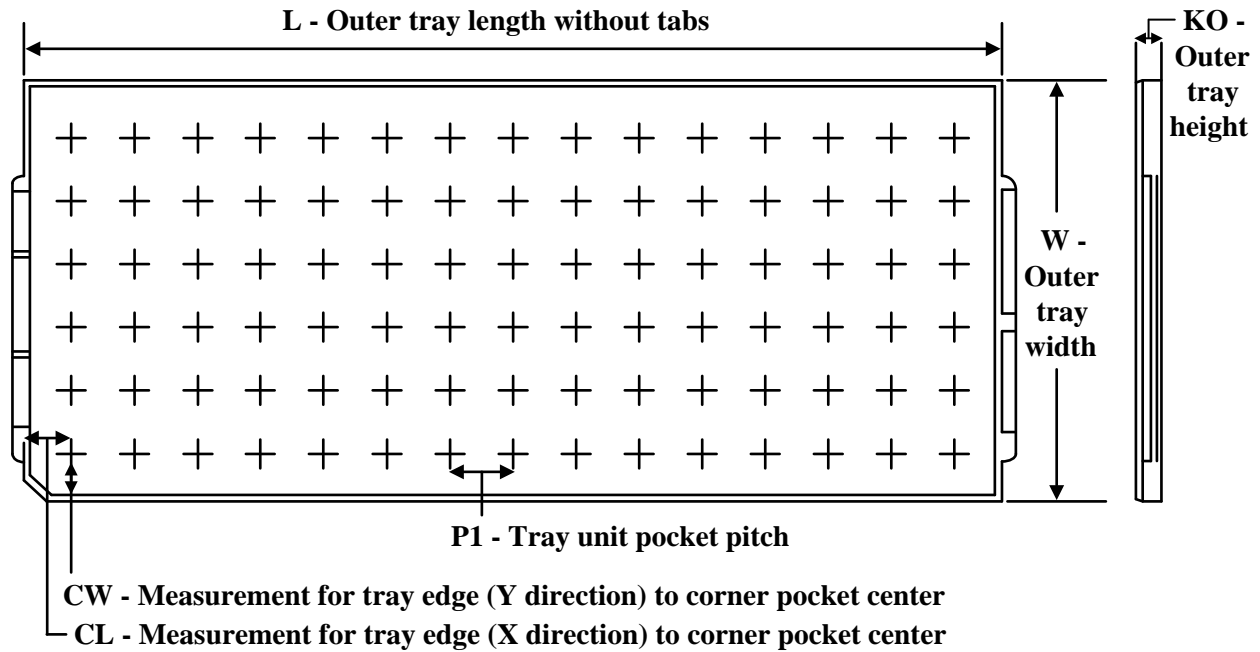
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| MSP430F6733AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6733AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6734AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6734AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6735AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6735AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6736AIPNR | LQFP | PN | 80 | 1000 | 330.0 | 24.4 | 15.0 | 15.0 | 2.1 | 20.0 | 24.0 | Q2 |
| MSP430F6736AIPZR | LQFP | PZ | 100 | 1000 | 330.0 | 24.4 | 17.0 | 17.0 | 2.1 | 20.0 | 24.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F6720AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6720AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6721AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6721AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6723AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6723AIPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F6724AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6724AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6725AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6725AIPZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F6726AIPNR | LQFP | PN | 80 | 1000 | 367.0 | 367.0 | 45.0 |
| MSP430F6726AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6730AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6730AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6731AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6731AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6733AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6733AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| MSP430F6734AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6734AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6735AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6735AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6736AIPNR | LQFP | PN | 80 | 1000 | 350.0 | 350.0 | 43.0 |
| MSP430F6736AIPZR | LQFP | PZ | 100 | 1000 | 350.0 | 350.0 | 43.0 |

TRAY


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|-----------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| MSP430F6720AIPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6721AIPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6731AIPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6733AIPN | PN | LQFP | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| MSP430F6735AIPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |
| MSP430F6736AIPZ | PZ | LQFP | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.45 |

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

PN0080A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



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NOTES:

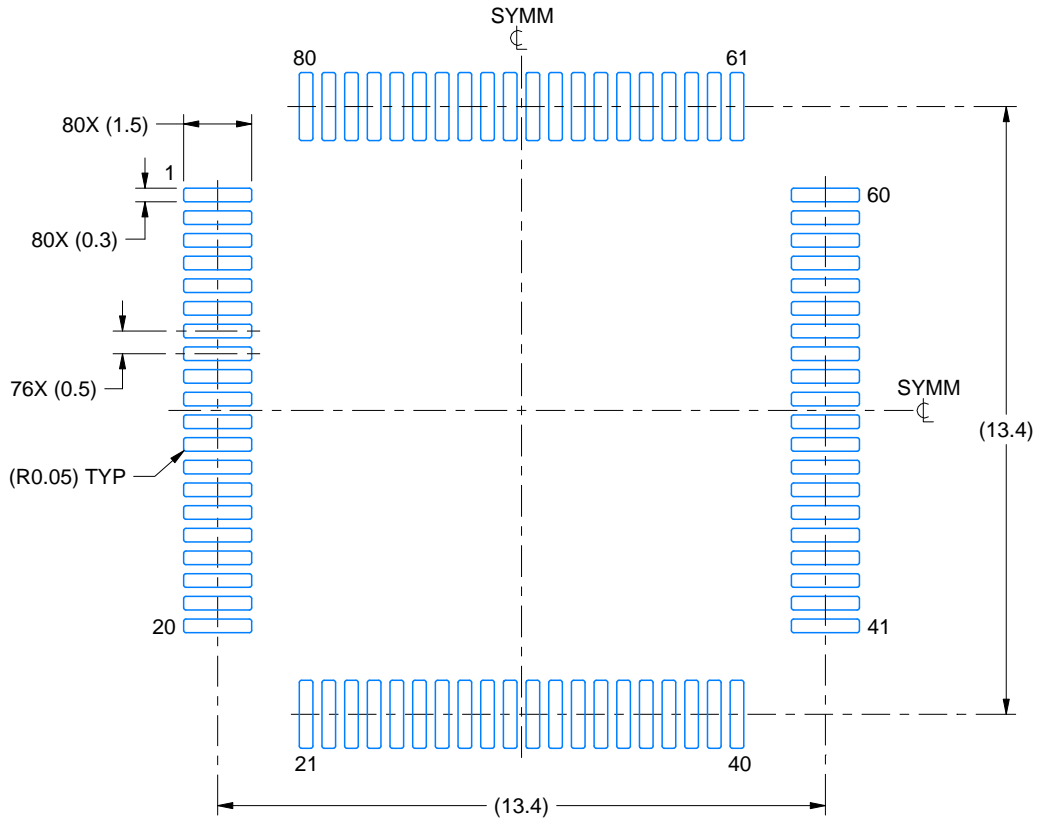
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

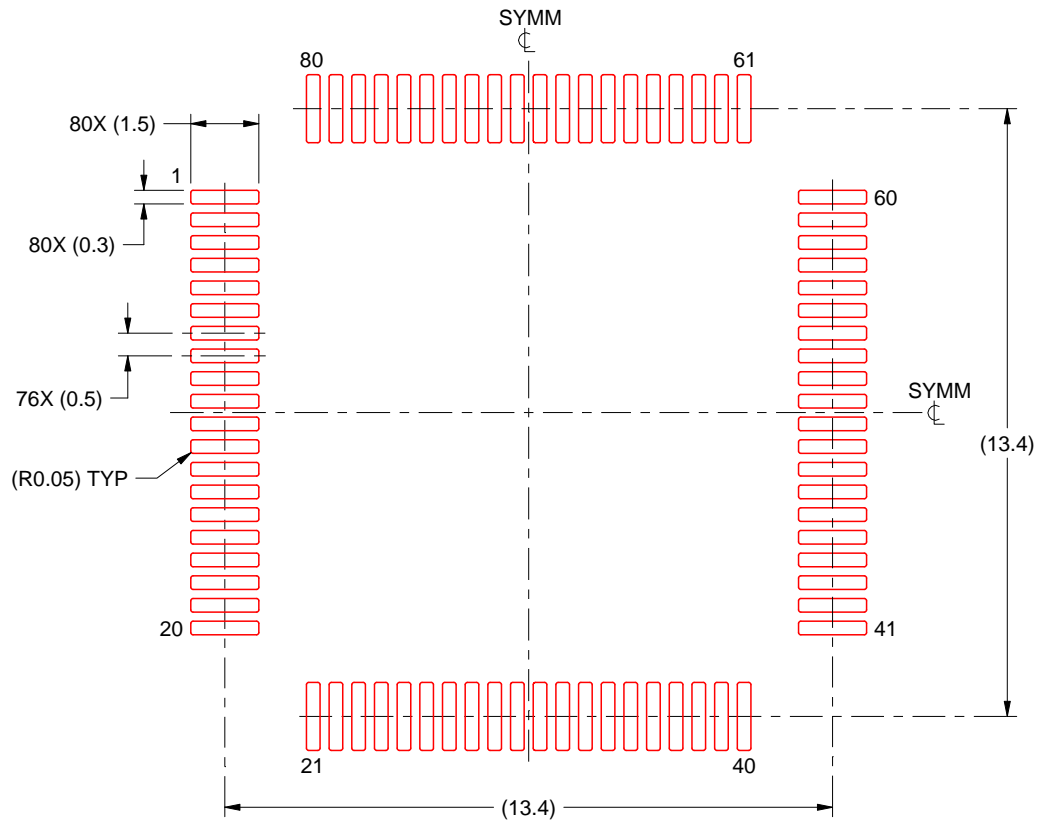
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PN0080A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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