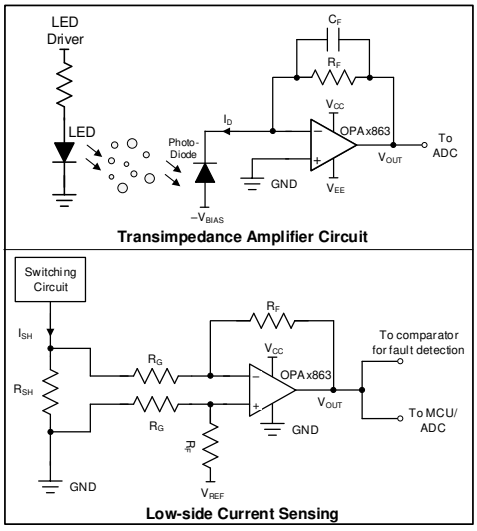
OPAx863 低功耗、110MHz、轨至轨输入和输出放大器

1 特性

- 宽带宽
  - 单位增益带宽：110MHz (A_V = 1V/V)
  - 增益带宽积：50 MHz
- 低功耗
  - 静态电流：700 μA/通道（典型值）
  - 断电模式：1.5 μA（最大值，V_S= 3V）
  - 电源电压：2.7V 至 12.6V
- 输入电压噪声：5.9 nV/ √Hz
- 压摆率：105 V/μs
- 轨到轨输入和输出
- HD_2/HD_3：在 20 kHz ($2V_{PP}$) 时为 –129dBc/–138dBc
- 工作温度范围：
  –40°C 至 +125°C
- 其他特性：
  - 过载功率限制
  - 输出短路保护
- 高精度版：OPAx863A

2 应用

- 低功耗 SAR 和 Δ-Σ ADC 驱动器
- ADC 基准缓冲器
- 低侧电流感测
- 光电二极管 TIA 接口
- 电感式传感
- 超声波流量计
- 多功能打印机
- MDAC 输出缓冲器
- 增益和有源滤波器级



使用 OPAx863 的应用电路

3 说明

OPAx863 器件是单位增益稳定的低功耗、轨至轨输入/输出、电压反馈运算放大器，需在 2.7V 至 12.6V 的电源电压范围内运行。OPAx863 器件每通道仅消耗 700 μA 的电流，提供的增益带宽积为 50 MHz、压摆率为 105 V/μs，电压噪声密度为 5.9 nV/ √Hz。

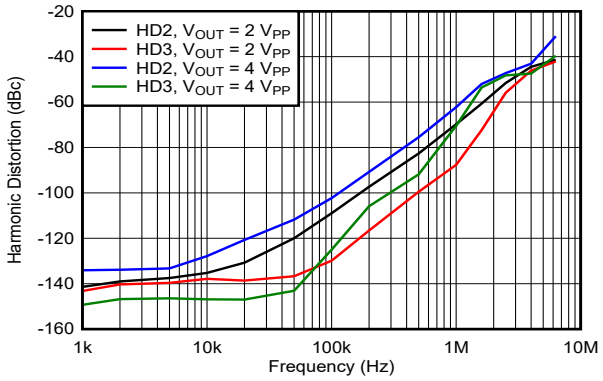
具有 2.7V 电源电压的轨至轨输入级在便携式电池供电型应用中非常有用。轨至轨输入级可在整个输入共模电压范围内很好地适应增益带宽积和噪声，从而在宽输入动态范围内实现出色的性能。OPA863 具有断电 (PD) 模式，PD 静态电流 (I_Q) 为 1.5 μA（最大值），并在 6.5 μs（电源电压为 3V）内开启或关闭。

OPAx863 器件包括过载功率限制功能，可限制输出饱和时 I_Q 的增加，从而避免电池供电的功率敏感型系统中出现过度功率耗散。输出级具有短路保护功能，使得该器件适用于恶劣的环境。

器件信息(1)(2)

器件型号	封装	封装尺寸（标称值）
OPA863	SOT-23 (5) (DBV)(3)	2.90mm × 1.60mm
	SOT-23 (6) (DBV)	2.90mm × 1.60mm
OPA2863	VSSOP (8) (DGK)	3.00mm × 3.00mm
	WQFN (10) (RUN)	2.00mm × 2.00mm
	SOIC (8) (D)	4.90mm × 3.91mm
OPA4863	TSSOP (14) (PW)(3)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 有关相关产品，请参阅*器件比较*
(3) 预发布封装。



G = 1V/V 时的失真性能

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (July 2022) to Revision H (August 2022) — **Page**

- Changed the status of the RUN Package, from: *preview* to: *production* 4

Changes from Revision F (April 2022) to Revision G (July 2022) — **Page**

- 向*特性* 部分添加了 OPAx863A 信息 1
- 向数据表添加了 DBV 5 引脚 SOT23 封装 1
- Changed the status of the D Package, from: *preview* to: *production* 4
- Updated the *Output Voltage vs Load Current* and *Output Voltage vs Load Current* figures to show typical device performance 13

Changes from Revision E (November 2021) to Revision F (April 2022) — **Page**

- 在数据表中添加了 D 封装、8 引脚 SOIC 和 RUN 封装、10 引脚 WQFN 1

Changes from Revision D (July 2021) to Revision E (November 2021) — **Page**

- 更新了数据表标题 1
- 更新了*说明* 部分 1
- Changed the status of the DBV Package, from: *preview* to: *production* 4
- Removed footnote from Electrical Characteristics: 10 V and Electrical Characteristics: 3 V tables 9
- Removed the links to the *Noninverting* and *Inverting Amplifier* figures in the *Typical Characteristics: V_S = 10 V*, *Typical Characteristics: V_S = 3 V*, and *Typical Characteristics: V_S = 3 V to 10 V* sections 13
- Updated the title of the *Frequency Response vs Load Capacitance*, *Frequency Response vs Ambient Temperature*, and *Frequency Response vs Output Voltage* figures in the *Typical Characteristics: V_S = 10 V* section 13
- Added the *Quiescent Current Distribution*, *Input Bias Current Distribution*, *Input Offset Voltage Distribution*, *Input Offset Voltage Drift Distribution*, *Input Offset Voltage Drift Distribution*, *Quiescent Current vs Ambient*

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Changes from Revision C (April 2021) to Revision D (July 2021) **Page**

Changes from Revision B (April 2021) to Revision C (April 2021) **Page**

Changes from Revision A (June 2020) to Revision B (April 2021) **Page**

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5 Device Comparison Table

DEVICE	±V_S (V)	I_Q / CHANNEL (mA)	GBWP (MHz)	SLEW RATE (V/µs)	VOLTAGE NOISE (nV/√Hz)	AMPLIFIER DESCRIPTION
OPAx863	±6.3	0.70	50	105	5.9	Unity-gain stable RRIO Bipolar Amplifier
LMH6643	±6.4	2.7	65	130	17	Unity-gain stable NRI/RRO Bipolar Amplifier
OPAx810	±13.5	3.6	70	200	6.3	Unity-gain stable RRIO FET-Input Amplifier
OPAx837	±2.7	0.6	50	105	4.7	Unity-gain stable NRI/RRO Bipolar Amplifier
OPAx607	±2.75	0.9	50	24	3.8	Decompensated Gain of 6 V/V stable CMOS Amplifier

6 Pin Configuration and Functions

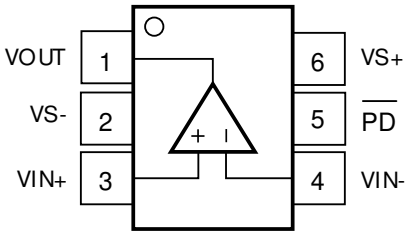

图 6-1. DBV Package, 6-Pin SOT-23 (Top View)

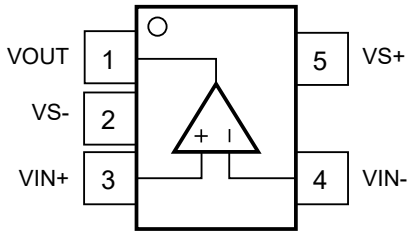

图 6-2. DBV Package (Preview), 5-Pin SOT-23 (Top View)

表 6-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	OPA863			
	SOT-23 (6)	SOT-23 (5)		
$\overline{PD}$	5	—	I	Power down. Low = disabled, high = normal operation (pin must be driven).
VIN+	3	3	I	Noninverting input pin
VIN –	4	4	I	Inverting input pin
VOUT	1	1	O	Output pin
VS –	2	2	P	Negative power-supply pin
VS+	6	5	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

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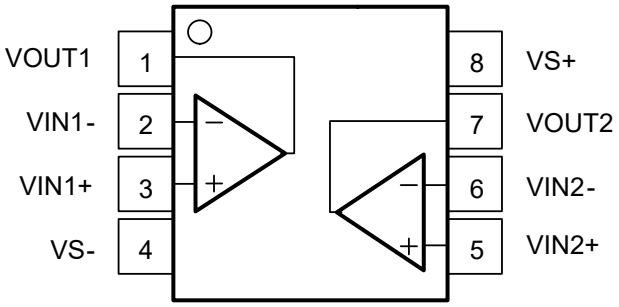

图 6-3. D Package, 8-Pin SOIC and DGK Package, 8-Pin VSSOP, (Top View)

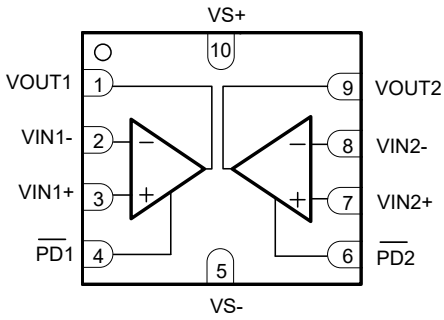

图 6-4. RUN Package, 10-Pin WQFN (Top View)

表 6-2. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	OPA2863			
	SOIC, VSSOP	WQFN		
$\overline{PD1}$	—	4	I	Amplifier 1 power down. Low = disabled, high = normal operation (pin must be driven).
$\overline{PD2}$	—	6	I	Amplifier 2 power down. Low = disabled, high = normal operation (pin must be driven).
VIN1 –	2	2	I	Amplifier 1 inverting input pin
VIN1+	3	3	I	Amplifier 1 noninverting input pin
VIN2 –	6	8	I	Amplifier 2 inverting input pin
VIN2+	5	7	I	Amplifier 2 noninverting input pin
VOUT1	1	1	O	Amplifier 1 output pin
VOUT2	7	9	O	Amplifier 2 output pin
VS –	4	5	P	Negative power-supply pin
VS+	8	10	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

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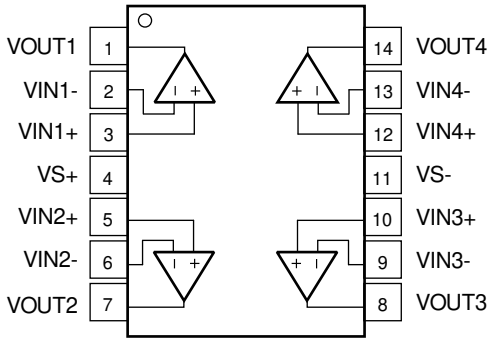

图 6-5. PW Package (Preview), 14-Pin TSSOP (Top View)

表 6-3. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	OPA4863 TSSOP		
VIN1 –	2	I	Amplifier 1 inverting input pin
VIN1+	3	I	Amplifier 1 noninverting input pin
VIN2 –	6	I	Amplifier 2 inverting input pin
VIN2+	5	I	Amplifier 2 noninverting input pin
VIN3 –	9	I	Amplifier 3 inverting input pin
VIN3+	10	I	Amplifier 3 noninverting input pin
VIN4 –	13	I	Amplifier 4 inverting input pin
VIN4+	12	I	Amplifier 4 noninverting input pin
VOUT1	1	O	Amplifier 1 output pin
VOUT2	7	O	Amplifier 2 output pin
VOUT3	8	O	Amplifier 3 output pin
VOUT4	14	O	Amplifier 4 output pin
VS –	11	P	Negative power-supply pin
VS+	4	P	Positive power-supply pin

(1) I = input, O = output, and P = power.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		13	V
	Supply turn-on/off maximum dV/dt, DBV and D packages		0.1	V/µs
V_I	Input voltage	V_{S-} – 0.5	V_{S+} + 0.5	V
V_{ID}	Differential input voltage		±1	V
I_I	Continuous input current(2)		±10	mA
I_O	Continuous output current(3)		±30	mA
	Continuous power dissipation	See *Thermal Information*		
T_J	Maximum junction temperature		150	°C
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Continuous input current limit for both the ESD diodes to supply pins and amplifier differential input clamp diode. The differential input clamp diode limits the voltage across it to 1 V with this continuous input current flowing through it.
(3) Long-term continuous current for electromigration limits.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S+} - V_{S-}	Total supply voltage	2.7	10	12.6	V
T_A	Ambient temperature	–40	25	125	°C

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7.4 Thermal Information: OPA863

THERMAL METRIC(1)		OPA863 DBV (SOT23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	161.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	21.2	°C/W
Y_{JB}	Junction-to-board characterization parameter	42.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Thermal Information: OPA2863

THERMAL METRIC(1)		OPA2863 DGK (VSSOP) 8 PINS	OPA2863 D (SOIC) 8 PINS	OPA2863 RUN (WQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180.3	120.0	110.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	67.5	63.3	66.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	101.9	63.2	43.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	9.8	17.2	2.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	100.1	62.5	43.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information: OPA4863

THERMAL METRIC(1)		OPA4863 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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7.7 Electrical Characteristics: V_S = 10 V

at V_{S+} = 5 V, V_{S-} = –5 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1, < 1 dB peaking		110		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 2 V_{PP}		17		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		15		MHz
SR	Slew rate	V_{OUT} = 2 V step, G = –1		105		V/µs
	Rise, fall time	V_{OUT} = 200 mV step		9		ns
	Settling time to 0.1%	V_{OUT} = 2 V step		57		ns
	Settling time to 0.01%			70		
	Overshoot/undershoot	V_{OUT} = 2 V step		1		%
	Overdrive recovery time	G = –1, 0.5 V overdrive beyond supplies		70		ns
		G = 1, 0.5 V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 2 V_{PP}		–129		dBc
HD3	Third-order harmonic distortion			–138		
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 2 V_{PP}		–107		dBc
HD3	Third-order harmonic distortion			–125		
e_N	Input voltage noise	Flatband, 1/f corner at 25 Hz		5.9		nV/√Hz
i_N	Input current noise	Flatband, 1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 2 V_{PP}		–124		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = ±2.5 V	110	128		dB
V_{OS}	Input-referred offset voltage		–1.3	±0.4	1.3	mV
	Input offset voltage drift	T_A = –40°C to +125°C, D, RUN and DGK packages	–3.5	±1	3.5	µV/°C
		T_A = 0°C to +85°C, DBV package	–4.4	±1	4.4	
		T_A = –40°C to +125°C, DBV package	–4.9	±1	4.9	
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = –40°C to +85°C			1.2	
		T_A = –40°C to +125°C			1.6	
	Input bias current drift	T_A = –40°C to +125°C		±3	7.6	nA/°C
	Input offset current		-30	±10	30	nA
INPUT						
	Input common-mode voltage range		V_{S-} – 0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM}=V_{S-} – 0.2 V to V_{S+} – 1.6 V	100	120		dB
	Input impedance common-mode			650 || 0.8		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		V_{S-}+0.14	V_{S-}+0.2	V
		T_A = –40°C to +125°C		V_{S-}+0.15	V_{S-}+0.22	
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+} – 0.2	V_{S+} – 0.14		V
		T_A = –40°C to +125°C	V_{S+} – 0.2	V_{S+} – 0.15		

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7.7 Electrical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, V_{S-} = –5 V, G = 1 V/V, R_F = 0 Ω for G = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, input and output common-mode is at mid-supply, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Linear output drive (sourcing/ sinking)	V_{OUT} = ±2.5 V, ΔV_{OS} < 1 mV(2)	25	30		mA
	Short-circuit current			45		mA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≅ 25°C		700	970	µA
		T_A = –40°C to +125°C			1280	
PSRR	Power-supply rejection ratio	ΔV_S = ±2 V(1)	100	120		dB
POWER DOWN (Pin Must be Driven)						
	Enable voltage threshold	Specified *on* above V_{S+} – 0.5 V			4.5	V
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	3.5			V
	Power-down quiescent current per channel	$\overline{PD} \leqslant V_{S+}$ – 1.5 V		2	3.3	µA
	Power-down pin bias current			2	50	nA
	Turn-on time delay			6		µs
	Turn-off time delay			4.5		µs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	Flatband, 1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.3	±0.15	1.3	mV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C		0.2	1.3	
	Common-mode rejection ratio	V_{CM} = 4.1 V to 5.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	120		dB

(1) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.
(2) Change in input offset voltage from no-load condition.

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7.8 Electrical Characteristics: V_S = 3 V

at V_{S+} = 3 V, V_{S-} = 0 V, G = 1, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
SSBW	Small-signal bandwidth	V_{OUT} = 20 mV_{PP}, G = 1		97		MHz
GBWP	Gain-bandwidth product			50		MHz
LSBW	Large-signal bandwidth	V_{OUT} = 1 V_{PP}		26		MHz
	Bandwidth for 0.1-dB flatness	V_{OUT} = 20 mV_{PP}		10		MHz
SR	Slew rate	V_{OUT} = 1 – V step, Gain = – 1		105		V/µs
	Rise, fall time	V_{OUT} = 200 – mV step		10		ns
	Settling time to 0.1%	V_{OUT} = 1 – V step		58		ns
	Settling time to 0.01%			90		
	Overshoot	V_{OUT} = 1 – V step		2		%
	Undershoot			16		
	Overdrive recovery time	G = – 1, 0.5V overdrive beyond supplies		95		ns
		G = 1, 0.5V overdrive beyond supplies		100		
HD2	Second-order harmonic distortion	f = 20 kHz, V_{OUT} = 1 V_{PP}		– 123		dBc
HD3	Third-order harmonic distortion			– 132		
HD2	Second-order harmonic distortion	f = 100 kHz, V_{OUT} = 1 V_{PP}		– 109		dBc
HD3	Third-order harmonic distortion			– 129		
e_N	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
i_N	Input current noise	Flatband, 1/f corner at 2 kHz		0.4		pA/√Hz
	Closed-loop output impedance	f = 1 MHz		0.2		Ω
	Channel-to-channel crosstalk	f = 1 MHz, V_{OUT} = 1 V_{PP}		– 127		dBc
DC PERFORMANCE						
A_{OL}	Open-loop voltage gain	V_{OUT} = 1 V to 2 V	104	123		dB
V_{OS}	Input-referred offset voltage		– 1.3	±0.4	1.3	mV
	Input offset voltage drift	T_A = – 40°C to +125°C, D, RUN and DGK packages	– 3.5	±1	3.5	uV/°C
		T_A = 0°C to +85°C, DBV package	– 4.4	±1	4.4	
		T_A = – 40°C to +125°C, DBV package	– 5	±1	5	
	Input bias current	T_A ≅ 25°C		0.3	0.73	µA
		T_A = – 40°C to +85°C			1.2	
		T_A = – 40°C to +125°C			1.56	
	Input bias current drift	T_A = – 40°C to +125°C		±3	7.4	nA/°C
	Input offset current		-30	±10	30	nA
INPUT						
	Input common-mode voltage range		V_{S-} – 0.2		V_{S+}+0.2	V
CMRR	Common-mode rejection ratio	V_{CM} = V_{S-} – 0.2 V to V_{S+} – 1.6 V	94	115		dB
	Input impedance common-mode			360 || 0.9		MΩ || pF
	Input impedance differential mode			200 || 0.5		kΩ || pF
OUTPUT						
V_{OL}	Output voltage, low	T_A ≅ 25°C		V_{S-} + 0.13	V_{S-} + 0.15	V
		T_A = – 40°C to +125°C		V_{S-} + 0.13	V_{S-} + 0.16	

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7.8 Electrical Characteristics: V_S = 3 V (continued)

at V_{S+} = 3 V, V_{S-} = 0 V, G = 1, R_F = 0 Ω for G =1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage, high	T_A ≅ 25°C	V_{S+} – 0.15	V_{S+} – 0.13		V
		T_A = –40°C to +125°C	V_{S+} – 0.15	V_{S+} – 0.13		
	Linear output drive (sourcing/ sinking)	V_{OUT} = ±0.7 V, ΔV_{OS} < 1 mV(2)	23	33		mA
	Short-circuit current			45		mA
POWER SUPPLY						
I_Q	Quiescent current per amplifier	T_A ≅ 25°C		690	910	µA
		T_A = –40°C to +125°C			1180	
PSRR	Power-supply rejection ratio	ΔV_S = ±1 V(1)	100	120		dB
POWER DOWN (Pin Must be Driven)						
	Enable voltage threshold	Specified *on* above V_{S+} – 0.5 V			2.5	V
	Disable voltage threshold	Specified *off* below V_{S+} – 1.5 V	1.5			V
	Power-down quiescent current per channel	$\overline{PD}$ ≤ V_{S+} – 1.5 V		0.8	1.5	µA
	Power-down pin bias current			1	50	nA
	Turn-on time delay			6.5		µs
	Turn-off time delay			5		µs
AUXILIARY INPUT STAGE						
	Gain-bandwidth product			50		MHz
	Input voltage noise	Flatband, 1/f corner at 25 Hz		6		nV/√Hz
	Input current noise	Flatband, 1/f corner at 100 Hz		0.4		pA/√Hz
	Input-referred offset voltage		–1.3	±0.15	1.3	mV
	Input bias current	T_A ≅ 25°C		0.2	0.6	µA
		T_A = –40°C to +125°C		0.4	1.2	
	Common-mode rejection ratio	V_{CM} = 2.1 V to 3.2 V	100	120		dB
	Power supply rejection ratio	ΔV_S = ±0.6 V	100	115		dB

(1) Change in supply voltage from the default test condition with only one of the positive or negative supplies changing corresponding to +PSRR and –PSRR.
(2) Change in input offset voltage from no-load condition.

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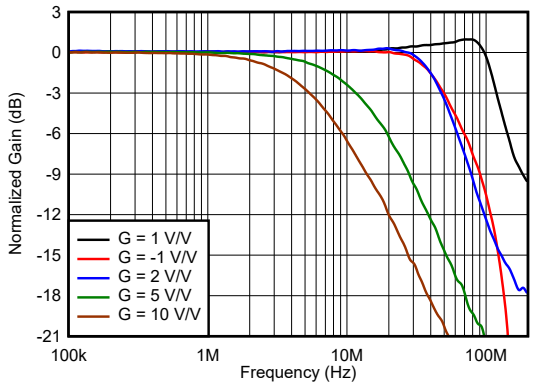
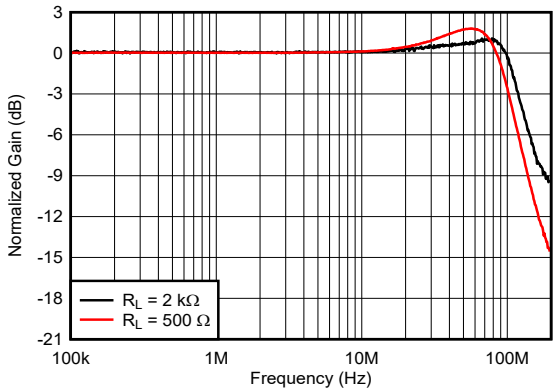
7.9 Typical Characteristics: V_S = 10 V

at V_{S+} = 5 V, V_{S-} = – 5 V, RF = 0 Ω for Gain = 1 V/V, otherwise RF = 1 kΩ for other gains, CL = 1 pF, RL = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



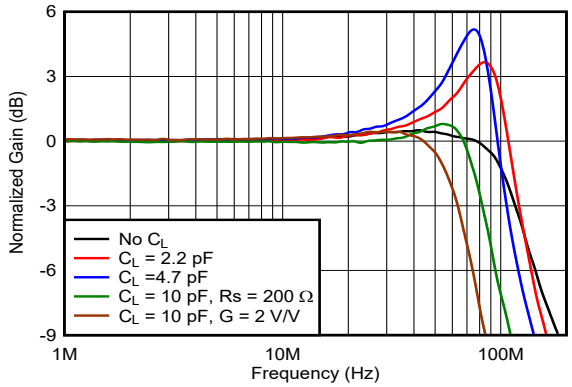
V_{OUT} = 20 mV_{PP}

图 7-1. Small-Signal Frequency Response vs Gain



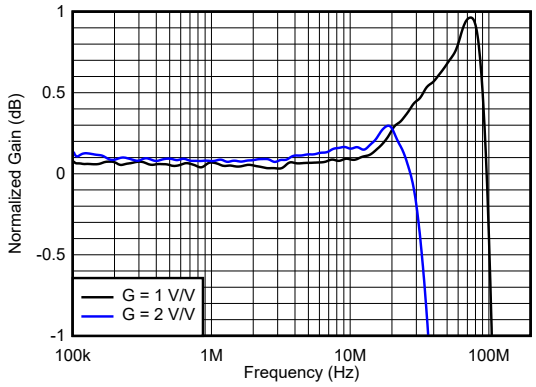
V_{OUT} = 20 mV_{PP}

图 7-2. Small-Signal Frequency Response vs Output Load



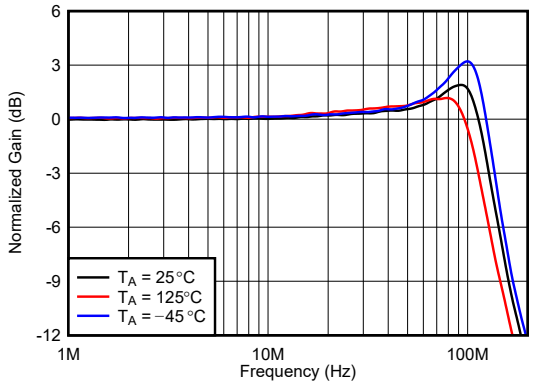
V_{OUT} = 20 mV_{PP}

图 7-3. Frequency Response vs Load Capacitance



V_{OUT} = 20 mV_{PP}

图 7-4. Small-Signal Response Flatness vs Gain



V_{OUT} = 20 mV_{PP}

图 7-5. Frequency Response vs Ambient Temperature

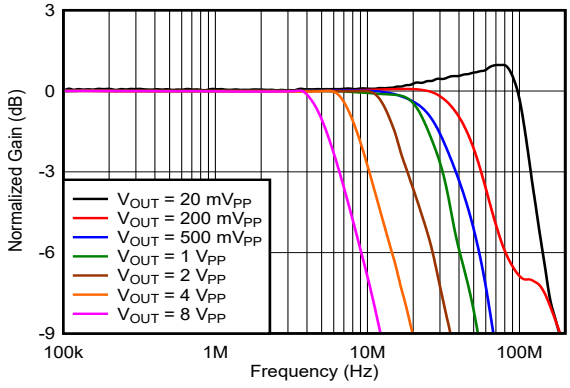


图 7-6. Frequency Response vs Output Voltage

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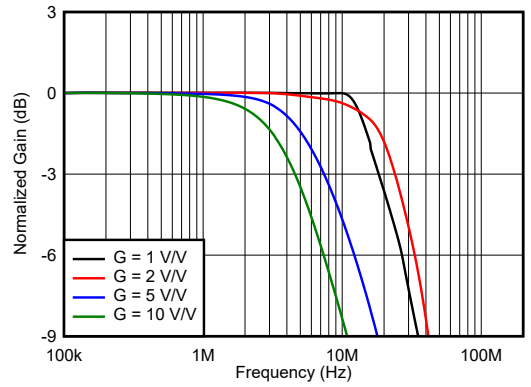
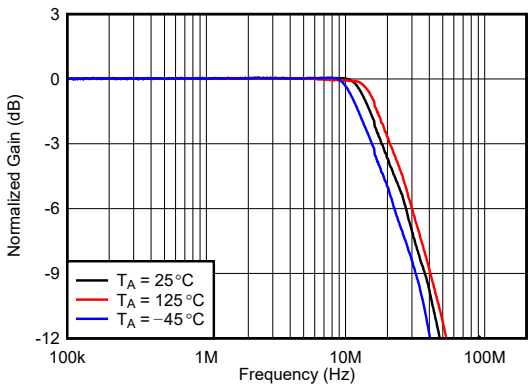
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, V_{S-} = –5 V, RF = 0 Ω for Gain = 1 V/V, otherwise RF = 1 kΩ for other gains, CL = 1 pF, RL = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



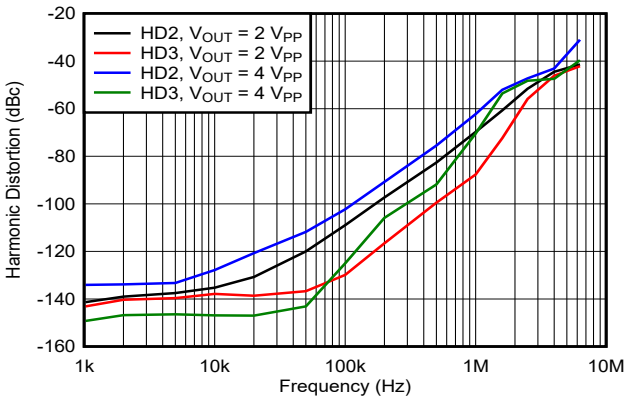
V_{OUT} = 2 V_{PP}

图 7-7. Large-Signal Frequency Response vs Gain



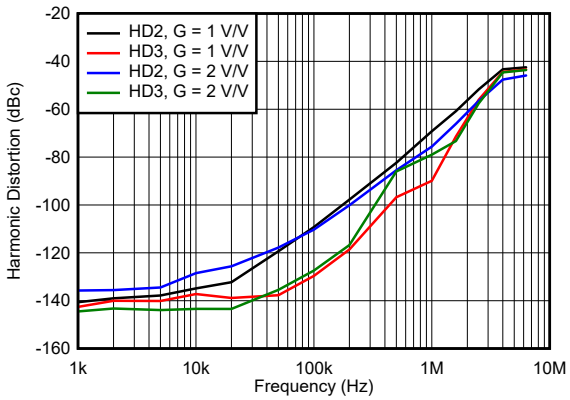
V_{OUT} = 2 V_{PP}

图 7-8. Frequency Response vs Ambient Temperature



G = 1 V/V

图 7-9. Harmonic Distortion vs Frequency



V_{OUT} = 2 V_{PP}

图 7-10. Harmonic Distortion vs Gain

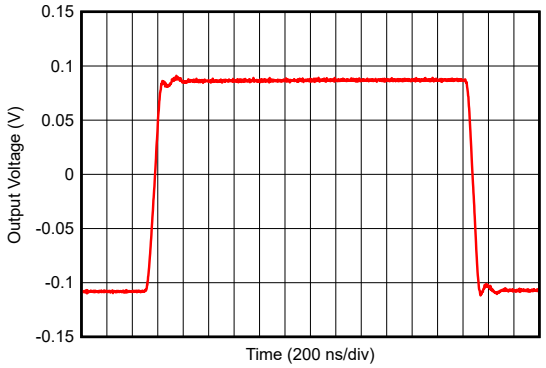


图 7-11. Small-Signal Transient Response

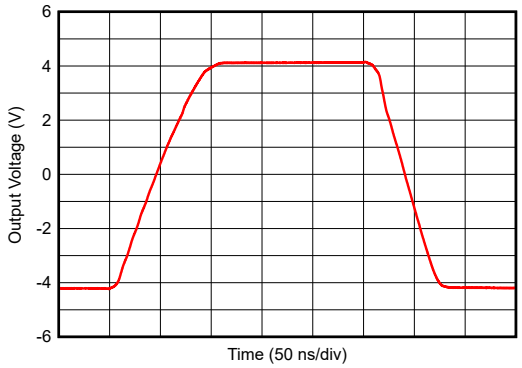


图 7-12. Large-Signal Transient Response

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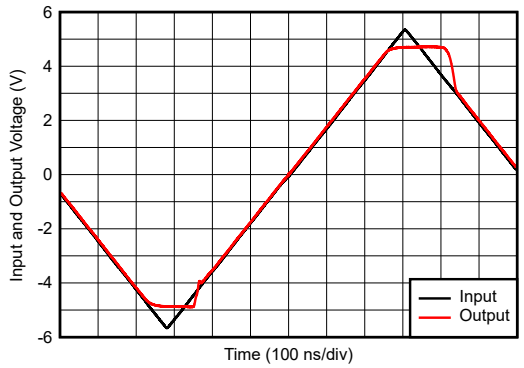
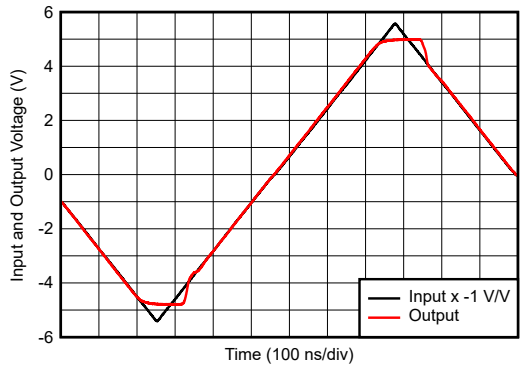
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, V_{S-} = – 5 V, RF = 0 Ω for Gain = 1 V/V, otherwise RF = 1 kΩ for other gains, CL = 1 pF, RL = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



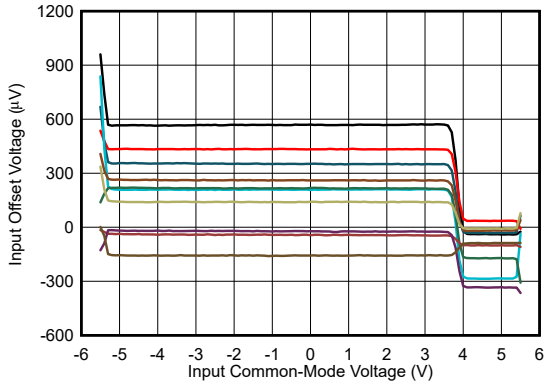
Gain = 1 V/V

图 7-13. Input Overdrive Recovery



Gain = -1 V/V

图 7-14. Output Overdrive Recovery



Measured for 10 units

图 7-15. Input Offset Voltage vs Input Common-Mode Voltage

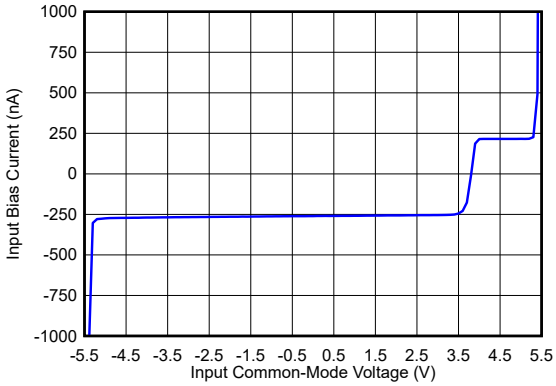


图 7-16. Input Bias Current vs Input Common-Mode Voltage

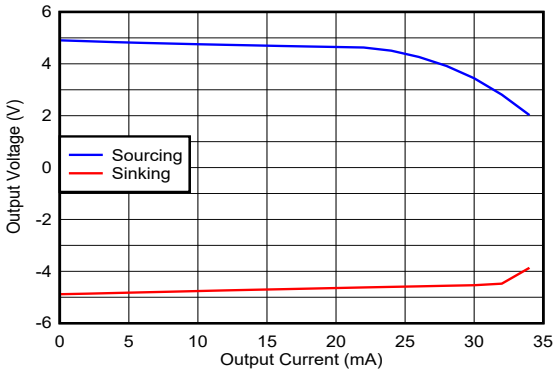
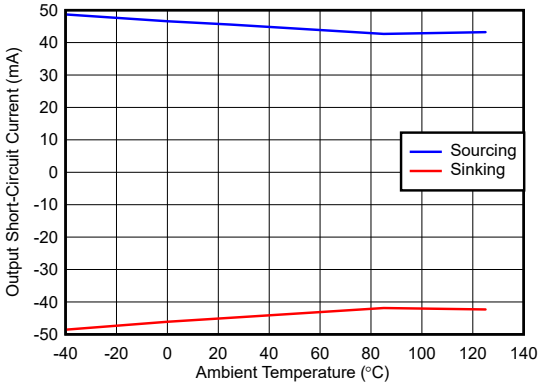


图 7-17. Output Voltage vs Load Current

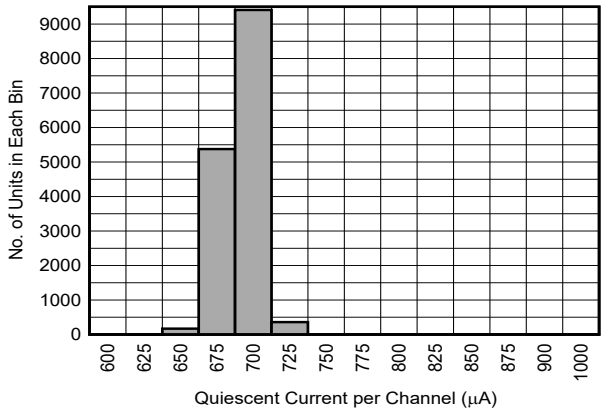


Output saturated and then short-circuited to opposite supply

图 7-18. Output Short-Circuit Current vs Ambient Temperature

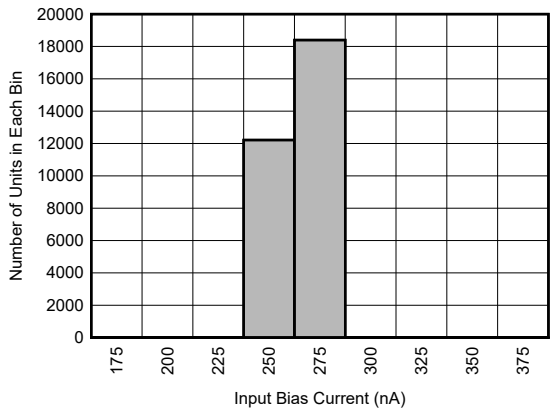
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, V_{S-} = –5 V, RF = 0 Ω for Gain = 1 V/V, otherwise RF = 1 kΩ for other gains, CL = 1 pF, RL = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



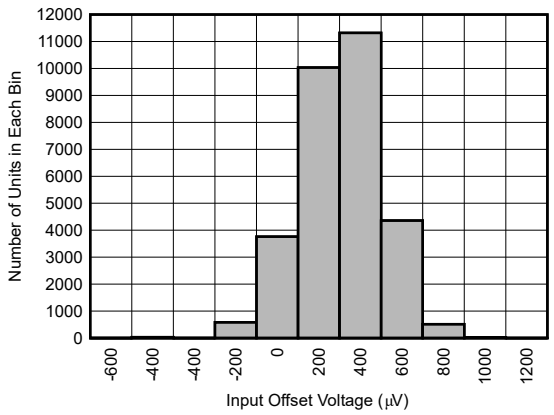
µ = 678 µA, σ = 13 µA

图 7-19. Quiescent Current Distribution



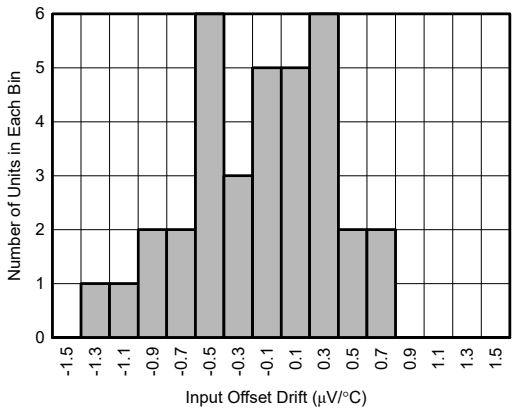
µ = 251 nA, σ = 5.6 nA

图 7-20. Input Bias Current Distribution



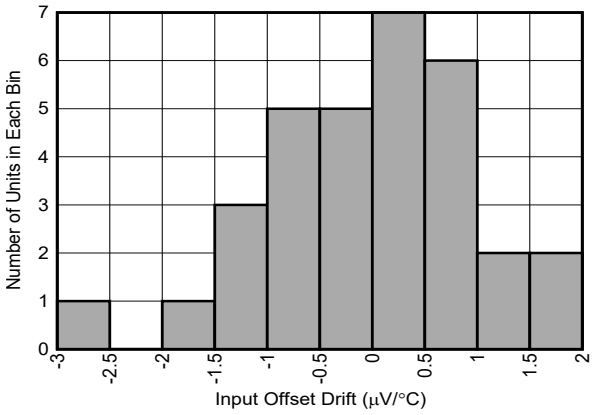
µ = 209 µV, σ = 193 µV

图 7-21. Input Offset Voltage Distribution



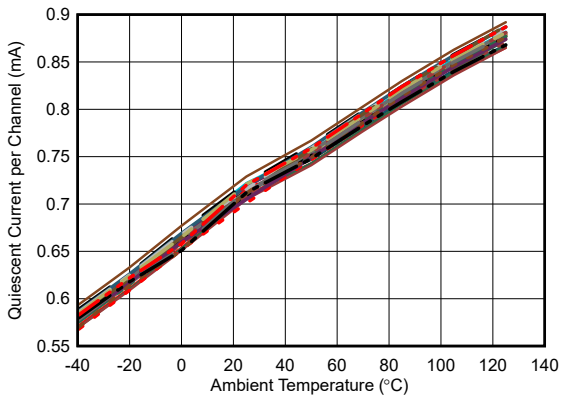
35 units, µ = -0.26 µV/°C, σ = 0.49 µV/°C, DGK package

图 7-22. Input Offset Voltage Drift Distribution



32 units, µ = −0.02 µV/°C, σ = 0.98 µV/°C, DBV package

图 7-23. Input Offset Voltage Drift Distribution



35 units

图 7-24. Quiescent Current vs Ambient Temperature

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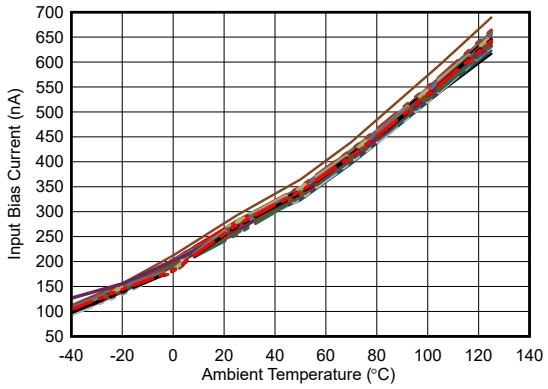
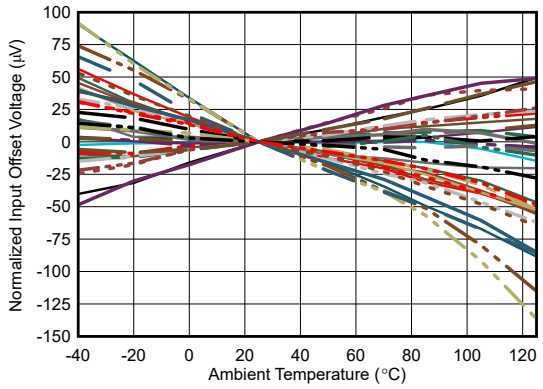
7.9 Typical Characteristics: V_S = 10 V (continued)

at V_{S+} = 5 V, V_{S-} = – 5 V, RF = 0 Ω for Gain = 1 V/V, otherwise RF = 1 kΩ for other gains, CL = 1 pF, RL = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and TA ≅ 25°C (unless otherwise noted)



35 units

图 7-25. Input Bias Current vs Ambient Temperature



Normalized to 25°C values, 35 units, DGK package

图 7-26. Input Offset Voltage vs Ambient Temperature

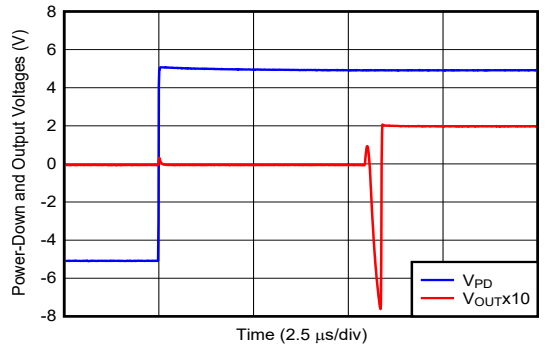


图 7-27. Turn-On Time to DC Input

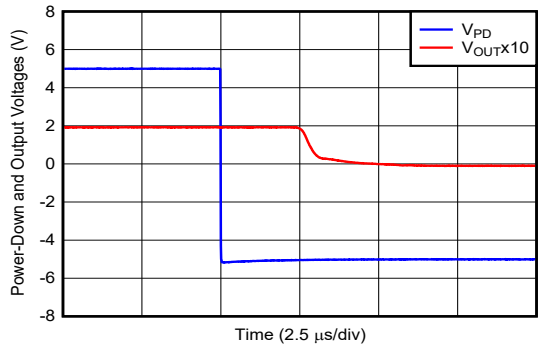
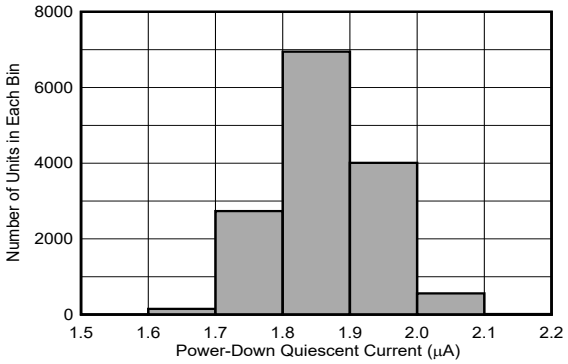


图 7-28. Turn-Off Time to DC Input



µ = 1.86 µA, σ = 0.076 µA

图 7-29. Power-Down Quiescent Current Distribution

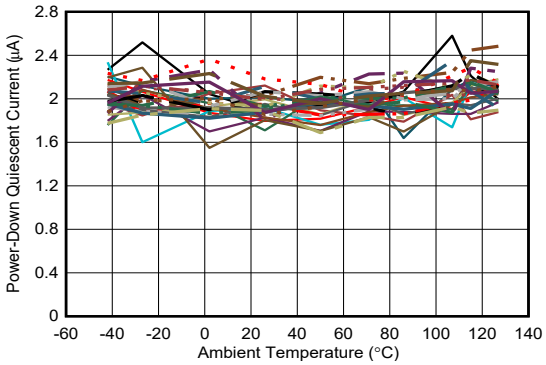
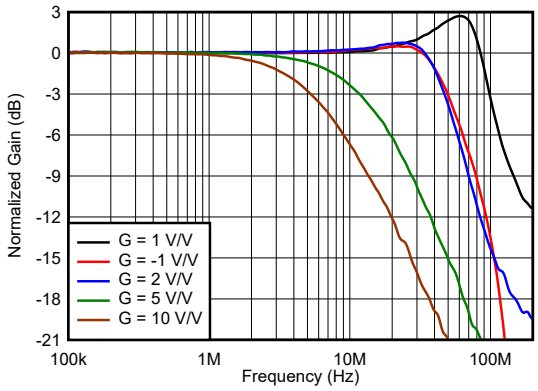


图 7-30. Power-Down I_Q vs Ambient Temperature

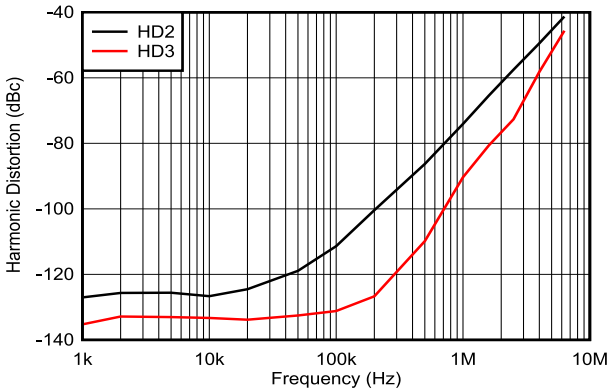
7.10 Typical Characteristics: V_S = 3 V

at V_{S+} = 3 V, V_{S-} = 0 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, G = 1 V/V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

图 7-31. Small-Signal Frequency Response vs Gain



V_{OUT} = 1 V_{PP}

图 7-32. Harmonic Distortion vs Frequency

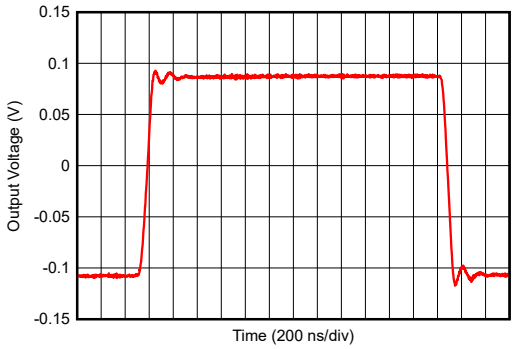


图 7-33. Small-Signal Transient Response

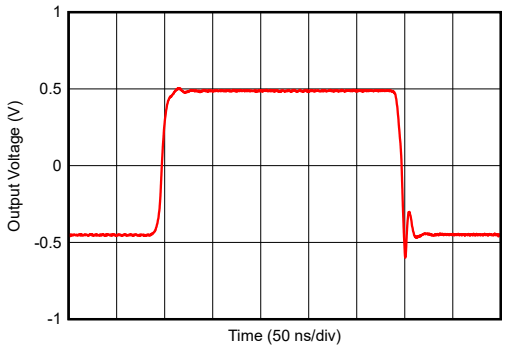
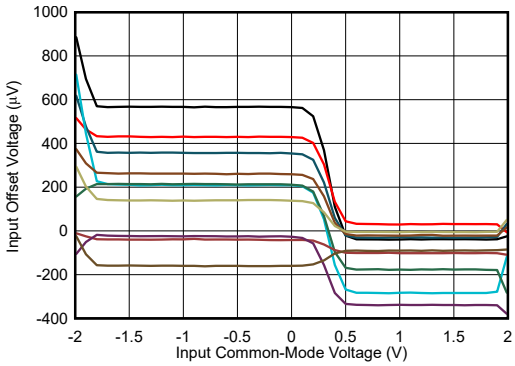


图 7-34. Large-Signal Transient Response



Measured for 10 units

图 7-35. Input Offset Voltage vs Input Common-Mode Voltage

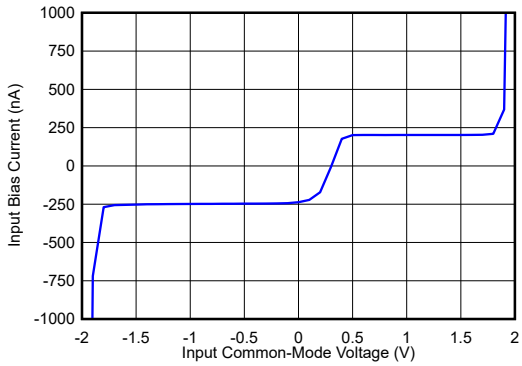


图 7-36. Input Bias Current vs Input Common-Mode Voltage

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7.10 Typical Characteristics: V_S = 3 V (continued)

at V_{S+} = 3 V, V_{S-} = 0 V, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ connected to 1 V, G = 1 V/V, input and output V_{CM} = 1 V, and T_A ≅ 25°C (unless otherwise noted)

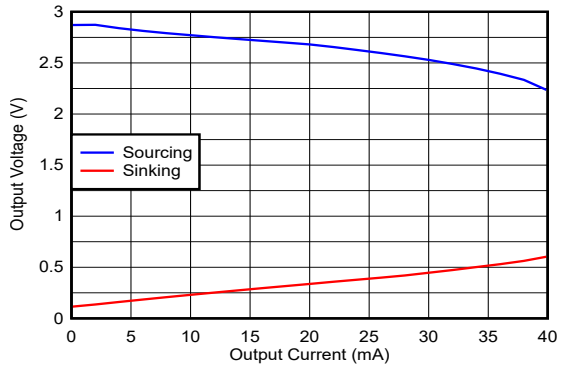
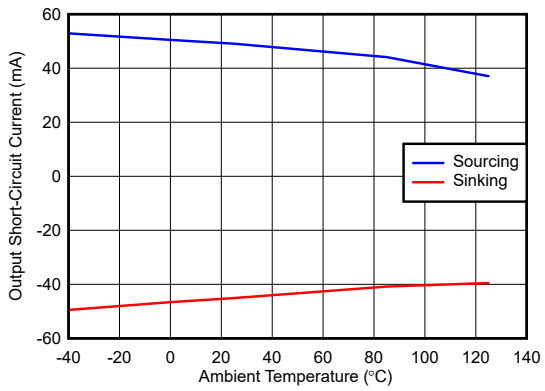


图 7-37. Output Voltage vs Load Current



Output saturated and then short-circuited to other supply

图 7-38. Output Short-Circuit Current vs Ambient Temperature

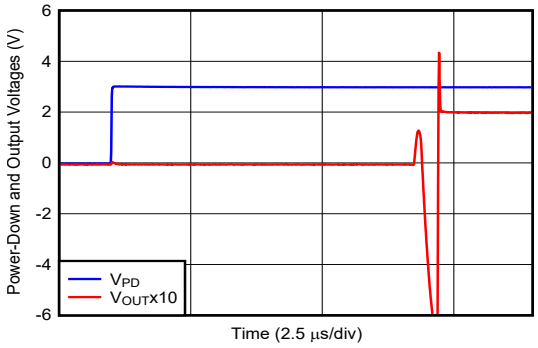


图 7-39. Turn-On Time to DC Input

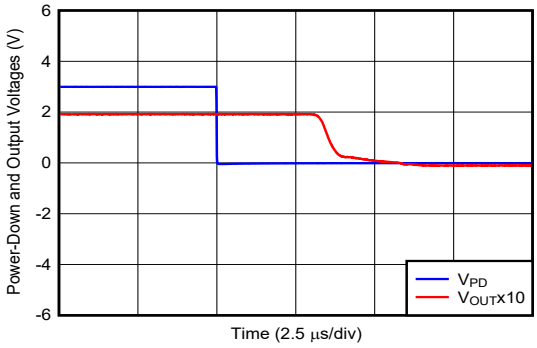
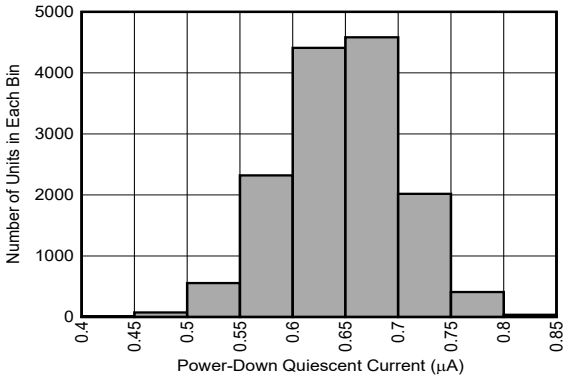


图 7-40. Turn-Off Time to DC Input



µ = 0.64 µA, σ = 0.056 µA

图 7-41. Power-Down Quiescent Current Distribution

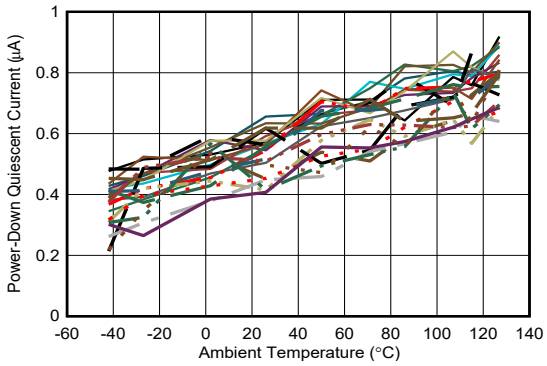
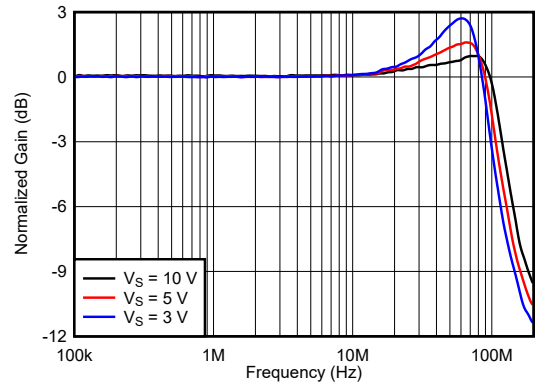


图 7-42. Power-Down I_Q vs. Ambient Temperature

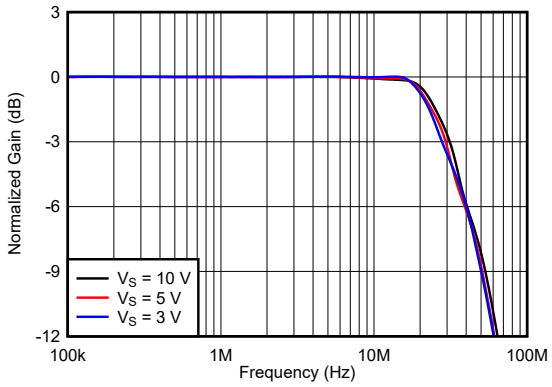
7.11 Typical Characteristics: V_S = 3 V to 10 V

at V_{OUT} = 2 V_{PP}, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)



V_{OUT} = 20 mV_{PP}

图 7-43. Frequency Response vs Supply Voltage



V_{OUT} = 1 V_{PP}

图 7-44. Frequency Response vs Supply Voltage

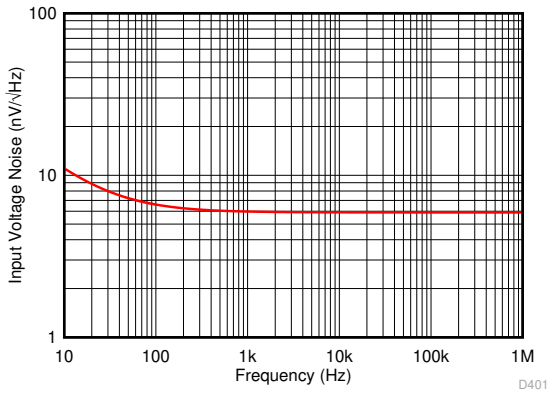


图 7-45. Input Voltage Noise Density vs Frequency

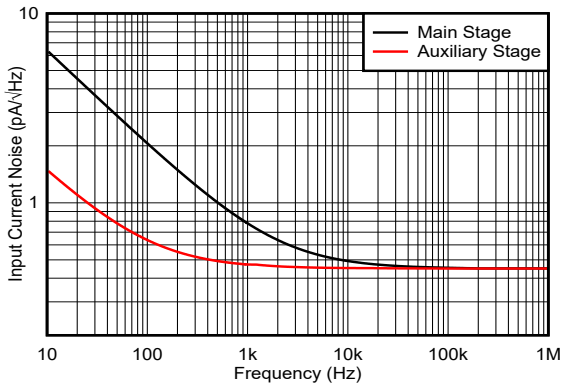


图 7-46. Input Current Noise Density vs Frequency

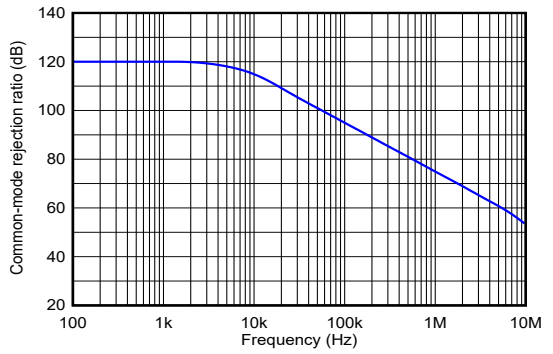


图 7-47. Common-Mode Rejection Ratio vs Frequency

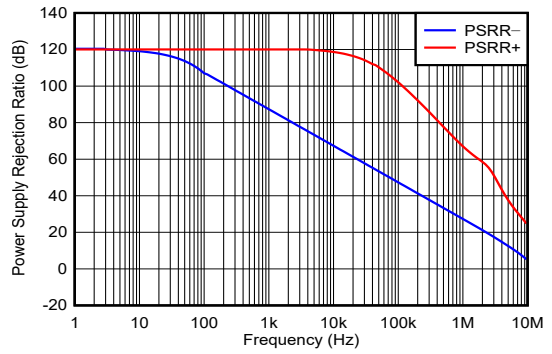


图 7-48. Power Supply Rejection Ratio vs Frequency

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7.11 Typical Characteristics: V_S = 3 V to 10 V (continued)

at V_{OUT} = 2 V_{PP}, R_F = 0 Ω for Gain = 1 V/V, otherwise R_F = 1 kΩ for other gains, C_L = 1 pF, R_L = 2 kΩ referenced to mid-supply, G = 1 V/V, input and output referenced to mid-supply, and T_A ≅ 25°C (unless otherwise noted)

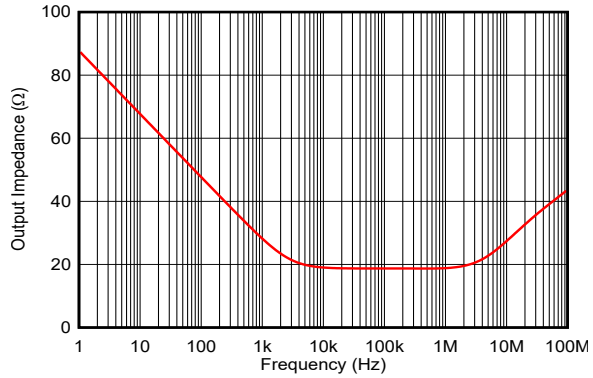
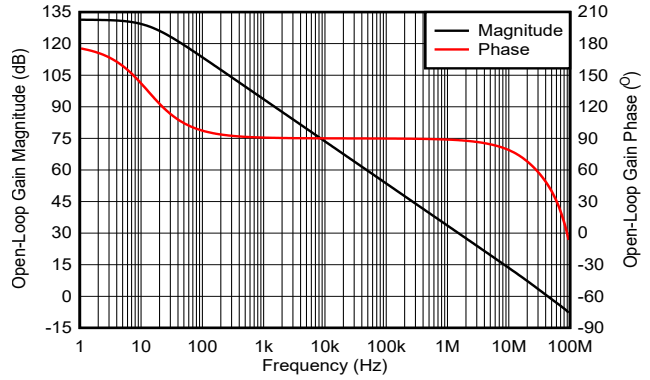
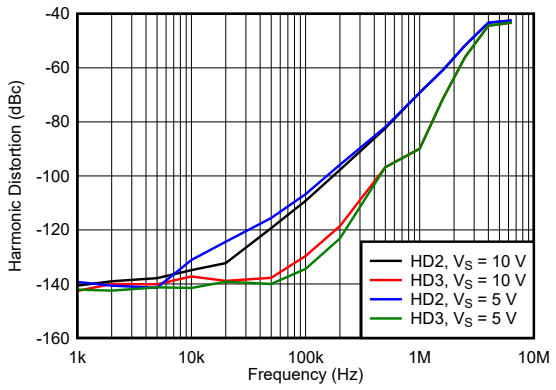


图 7-49. Open-Loop Output Impedance vs Frequency



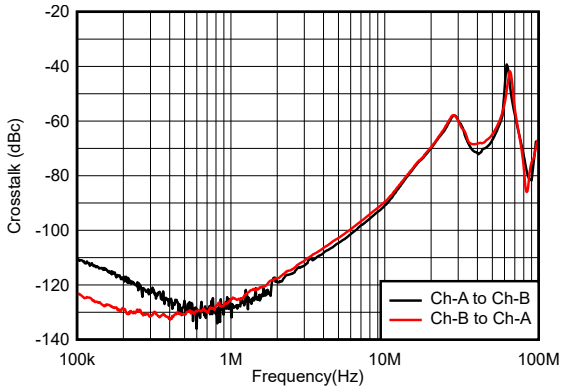
Small-signal response

图 7-50. Open-Loop Gain and Phase vs Frequency



V_{OUT} = 2 V_{PP}

图 7-51. Harmonic Distortion vs Supply Voltage



DGK package

图 7-52. Crosstalk vs Frequency

8 Detailed Description

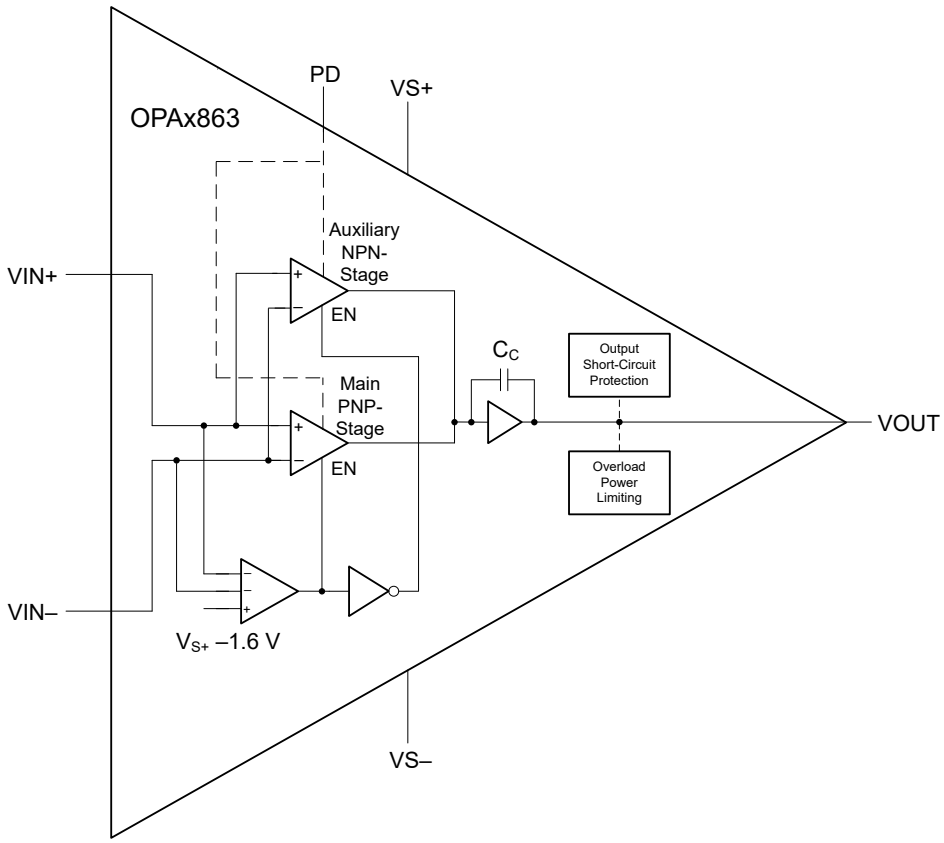
8.1 Overview

The OPAx863 devices are low-power, 50 MHz, rail-to-rail input and output (RRIO) bipolar voltage-feedback operational amplifiers with a voltage noise density of 5.9 nV/ √ Hz and 1/f noise corner at 25 Hz. The OPAx863 devices work in a wide-supply voltage range from 2.7 V to 12.6 V and consumes only 700 μ A quiescent current. The OPAx863 devices operate with 2.7 V supply, are RRIO capable, consume low-power, and offer a power-down mode, which makes them ideal amplifiers for 3.3-V or lower voltage applications that need superior AC performance. The amplifier's main and auxiliary input stages are matched for gain bandwidth product (GBW), noise and offset voltage suitable for applications which require wide dynamic input range and good SNR.

The device includes an overload power limit feature which limits the increase in quiescent current with over-driven and saturated outputs to either of the supply rails. For more details of this overload power limit feature, see 节 8.3.2.1. The amplifier's output is protected against short-circuit fault conditions.

The OPAx863 devices feature a power-down mode (PD) with a PD quiescent current of 1.5 μA (maximum) with a 3 V supply, with turn-on and turn-off time within less than 6.5 μs.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Stage

The OPAx863 devices include a rail-to-rail input stage. The main stage differential pair using PNP bipolar transistors operates for common-mode input voltages from V_{S-} – 0.2 V till V_{S+} – 1.6 V. The amplifier inputs transition into the auxiliary stage using NPN transistors for common-mode input voltages from V_{S+} – 1.6 V till V_{S+} + 0.2 V. The PNP and NPN input stages offer a gain-bandwidth product of 50 MHz and a voltage noise density of 5.9 nV/ √ Hz. The offset voltage for the two input stages is matched to lie within the device specifications. The auxiliary NPN input stage does not use the slew boost circuit during large-signal transient response. The input bias current for the PNP and NPN input stages is opposite in polarity, which adds an additional offset based on the values of the gain-setting and feedback resistors. A common-mode input voltage transition between these input stages will cause a crossover distortion which needs to be considered in high-frequency applications requiring superior linearity. Limit the common-mode input voltage to V_{S+} – 1.6 V (maximum) for main-stage operation across process and ambient temperature.

Since the OPAx863 devices are bipolar amplifiers, the two inputs are protected with anti-parallel back-to-back diodes between them, which limits the maximum input differential voltage to 1 V. The amplifier is slew limited, and the two inputs are pulled apart up to 1 V when the anti-parallel diodes begin to conduct in very fast input or output transient conditions. Care must be taken to use gain-setting and feedback resistors large enough to limit the current through these diodes in such conditions.

8.3.2 Output Stage

The OPAx863 devices feature a rail-to-rail output stage with possible signal swing from V_{S-} + 0.2 V to V_{S+} – 0.2 V. Violating the output headroom to either of the supplies will cause output signal clipping and introduce distortion.

The OPAx863 devices integrate an output short-circuit protection circuit, which makes the device rugged for use in real-world applications.

8.3.2.1 Overload Power Limit

The OPAx863 devices include overload power limiting which limits the increase in device quiescent current with output saturated to either of the supplies. Typically, when an amplifier's output saturates, its two inputs are pulled apart which may enable the slew boost circuit. The input differential voltage is an error voltage in negative feedback, which the amplifier core nullifies by engaging the slew boost circuit and driving the output stage deeper into saturation. Once the input to an amplifier attains a value large enough to saturate its output, any further increase in this input excitation results in a finite input differential voltage. As the output stage transistor is pushed deeper into saturation, its h_{FE} (base-to-collector current gain) drops with increase in its base and collector current, increasing the device quiescent current. This may cause a catastrophic failure in multi-channel, high-gain, high-density front-end designs and reduce operating lifetime in portable battery powered systems.

The OPAx863 devices overload power limiting includes an intelligent output saturation detection circuit which limits the device's quiescent current to 2.2-mA per channel under DC overload conditions. This increase in quiescent current is smaller with AC input or output and output saturation duration for only a fraction of the overall signal time period. Table 8-1 compares the increase in quiescent current with 50 mV input overdrive for OPAx863 devices and other voltage feedback amplifiers without overload power limit.

表 8-1. Quiescent Current with Saturated Outputs

Device	Input Differential Voltage	Quiescent Current during overload	Increase in I_Q from steady-state condition
OPAx863 with overload power limit	50 mV	1.1 mA	1.57x
Competitor amplifier without overload power limit	50 mV	1.96 mA	3.43x

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8.3.3 ESD Protection

As 图 8-1 shows, all device pins are protected with internal ESD protection diodes to the power supplies. These diodes provide moderate protection to input overdrive voltages above the supplies. The protection diodes can typically support 10-mA continuous input and output currents. Use series current limiting resistors if input voltages exceeding the supply voltages occur at the amplifier inputs, which ensures the current through the ESD diodes remains within their rated value. Since OPAx863 is a bipolar amplifier, the two inputs are protected with anti-parallel back-to-back diodes between them which limits the maximum input differential voltage to approximately 1 V. Care must be taken to use gain-setting and feedback resistors large enough to limit the current through these diodes in fast slewing conditions.

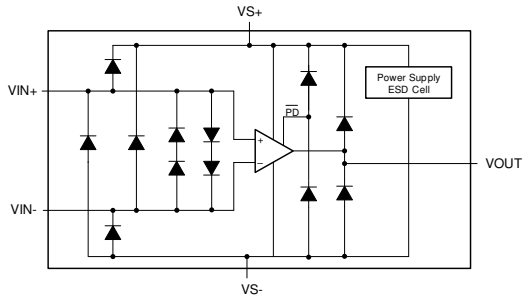

图 8-1. Internal ESD Protection

8.4 Device Functional Modes

8.4.1 Power-Down Mode

The OPAx863 includes a power-down mode for low-power standby operation with a quiescent current of only 1.5 μA (maximum) with a 3-V supply and high output impedance. Many low-power systems are active for only a small time interval when the parameters of interest are measured and remain in low-power standby mode for a majority of the time and an overall small average power consumption. The OPAx863 enables such a low-power operation with quick turn-on within less than 6.5 μs. Refer to the *Electrical Characteristics* tables for power-down pin control thresholds.

The $\overline{PD}$ pin always needs to be driven to avoid false triggering and oscillations. If it is not necessary to use the power-down mode, then the $\overline{PD}$ pin should be connected to V_{S+}. For applications which need the power-down mode, an external pull-up resistor from the $\overline{PD}$ pin to V_{S+} (driven with an open-collector power-down control logic) may be used.

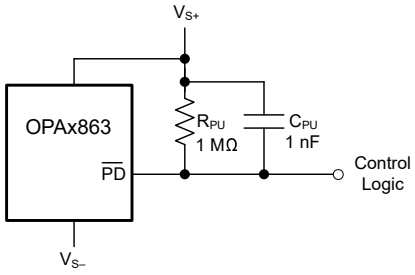

图 8-2. Power Down Control

图 8-2 shows the choice of value of the pull-up resistor RPU, which impacts the current consumption in power-down mode. Using a large RPU reduces the power consumption, but increases the noise at the PD pin which could cause the amplifier to power-down. A 1 nF capacitor may be used in parallel with RPU to avoid coupling of external noise and false triggering. For the case of $\overline{PD}$ pin driven to V_{S-}, the current I_{PU} through R_{PU} is given as,

$$I_{PU} = \frac{V_{S+} - V_{S-}}{R_{PU}} \quad (1)$$

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9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

9.2 Low-Side Current Sensing

Power converters use current-mode feedback control for superior transient response and multi-phase load sharing. Inverter stages control the phase currents for torque control in motor drives. Due to its simplicity and low-cost, many of these topologies use difference amplifier based low-side current sensing. 图 9-1 shows the use of OPAx863 in a difference amplifier circuit for low-side current sensing.

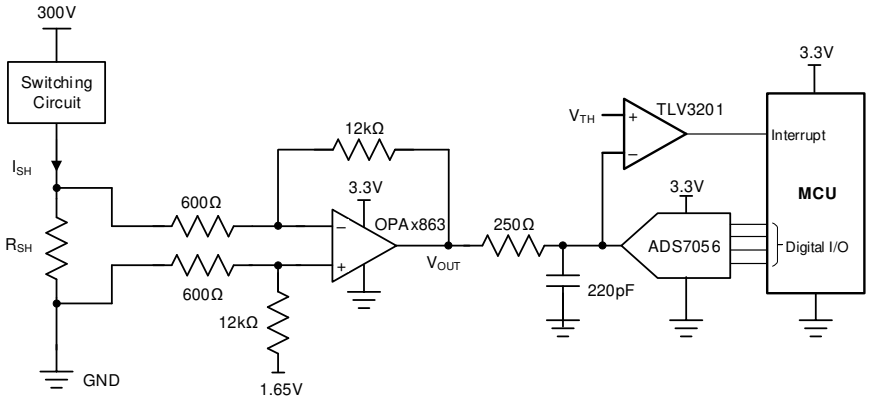

图 9-1. Low-Side Current Sensing in Power Converters

9.2.1 Design Requirements

表 9-1. Design Requirements

PARAMETER	DESIGN REQUIREMENT
Shunt resistor	10 mΩ
Input current	15 A_{PP}
Output voltage	3 V_{PP}
Switching frequency	50 kHz
Data acquisition	1 MSPS with 0.1% accuracy
Input voltage due to ground bounce	10 Vpk

In a difference amplifier circuit, the output voltage is given by,

$$V_O = \frac{R_F}{R_G} I_{SH} R_{SH} + V_{REF} \quad (2)$$

For lowest system noise, small values of R_F and R_G are preferred. The smallest value of R_G is limited by the input transient voltage (10 V here) seen by the circuit, and is given by,

$$R_G = \frac{V_{IN(max.)} - V_D - V_S}{I_{D(max.)}} \quad (3)$$

Where,

- $V_{IN(maximum)}$ is the maximum input transient voltage seen by the circuit
- V_D is the forward voltage drop of ESD diodes at the amplifier input
- $I_{D(maximum)}$ is the maximum current rating of the ESD diodes at the amplifier input

For a difference amplifier gain of 20 V/V, R_F and R_G of 12 kΩ and 600 Ω are used, respectively. With a clock frequency of 40 MHz and ADS7056 sampling at 1 MSPS, the available acquisition time for amplifier output settling is 550 ns. 图 9-2 shows the simulation results for the circuit in 图 9-1. The worst-case peak-to-peak input transient condition is simulated. The output of the OPAx863 device settles to within 0.1% accuracy within 543 ns. If using a slower clock frequency with the ADC is desired, then the acquisition time reduces with the same sampling rate, which degrades measurement accuracy. Alternatively, the sampling rate may be reduced to recover the required acquisition time and 0.1% accuracy.

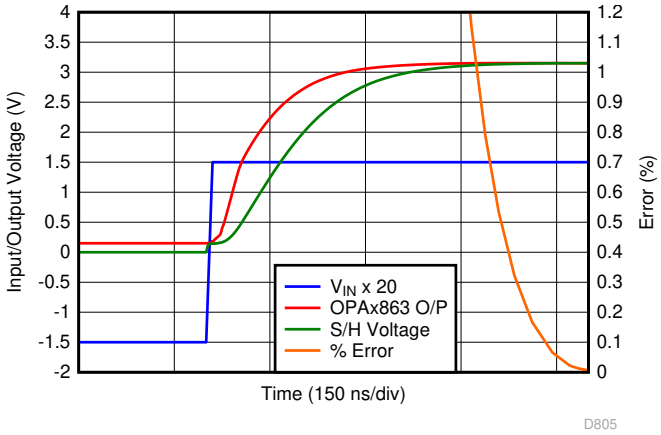

图 9-2. 0.1% Settling Performance

9.3 Front-End Gain and Filtering

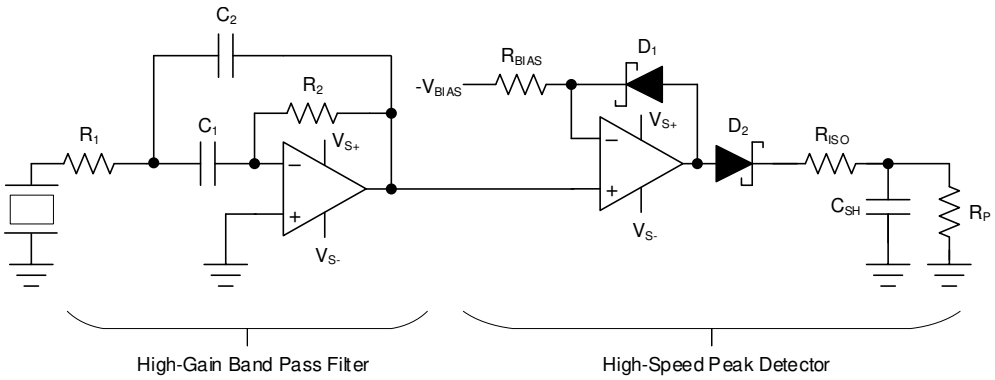

图 9-3. High-Gain Narrow Bandpass Filter and Peak Detector Circuit

Ultrasonic signaling is used for proximity and obstacle detection, level sensing, sonars, and so forth. Such signal chains detect the amplitude of received ultrasonic signal at a particular center frequency. 图 9-3 shows a high-gain narrow bandpass filter and peak detector circuit using any of the OPAx863 devices. The signal at the frequency of interest is filtered out, gained, and peak detected to report the amplitude at the output of this circuit. The phase information is lost in this circuit. The OPAx863 devices are used with its 50-MHz GBW to add a single-stage gain and filtering, and the peak detection capability is easily made with the RRIO capability of these amplifiers.

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9.4 Low-Power SAR ADC Driver and Reference Buffer

图 9-4 shows the use of the OPAx863 devices as a SAR ADC input driver and reference buffer driving the ADS7945. Sensors, which are used for interface with the physical environment, exhibit high output impedance and cannot drive SAR ADC inputs directly. A wide-GBW amplifier like the OPAx863 devices are needed to charge the switching capacitors at the SAR ADC input and to settle fast to the required accuracy within the given acquisition time. The ADC core draws transient current from the reference input during the conversion (digitization) phase, which needs to be driven with a wide-GBW amplifier to offer fast settling and maintain a stable reference voltage for superior digitization performance. The OPAx863 devices reference buffer is used in a composite loop with the OPA378 precision amplifier due to limitations in precision performance of wide-GBW amplifiers. The precision amplifier maintains low-offset output, whereas the OPAx863 devices provide the output drive and fast-settling performance.

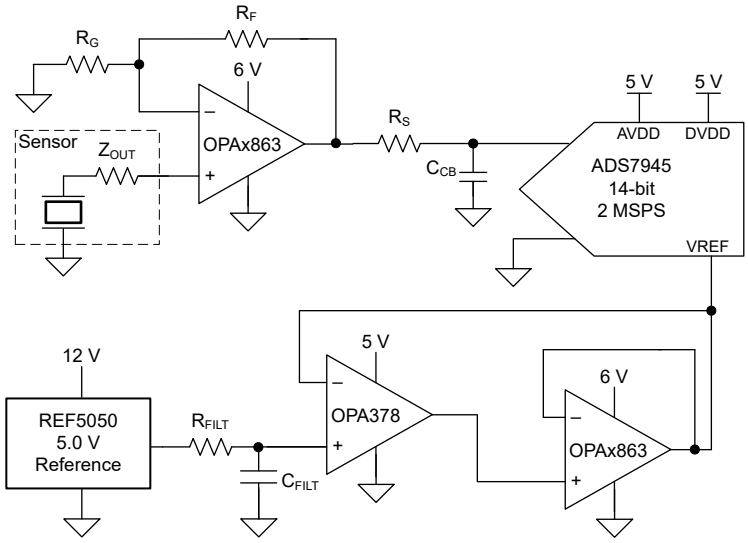

图 9-4. OPAx863 as Low-Power SAR ADC Driver

9.5 Variable Reference Generator Using MDAC

High-speed amplifiers may be used as a voltage buffer at MDAC output to generate a fast settling variable reference voltage. 图 9-5 shows a representative circuit using DAC8801 and OPAx863.

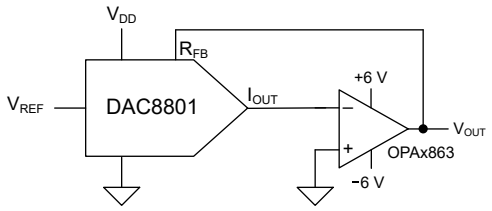

图 9-5. Variable Reference Generator Using MDAC and OPAx863

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9.6 Clamp-On Ultrasonic Flow Meter

图 9-6 shows how ultrasonic flow meters measure the rate of flow of a liquid using transit-time difference (t_{12} – t_{21}), which depends on the flow rate. 图 9-6 shows a representative schematic for a non-intrusive ultrasonic flow meter using the OPAx863 devices and 12-V transducer excitation. The OPAx863 devices are used for the forward path as a unity-gain buffer for 12-V pulsed transducer excitation at Node 1. At the same time, the receiver circuit at Node 2 (which also uses the OPAx863 devices) first provides an AC-gain followed by a DC-level shift to lead to the PGA, ADC, and processor within the MSP430 microcontroller.

Node 2 and Node 1 use similar transmit and receive circuits (discussed previously) for the reverse path. The OPAx863 devices wide GBW of 50 MHz introduces minimal phase-delay and low-noise for superior flow rate measurement. The amplifier stays in power-down mode for a majority of the time in battery powered systems, resulting in very small average system-level power consumption and prolonged battery lifetime with its 1.5 µA (maximum) power-down mode quiescent current with a 3-V supply. Since the transmit and receive signal chains are connected to the same point at the respective node transducers, the OPAx863's 12.6-V supply voltage capability enables 12-V transducer excitation without any damage to the front-end or need for external switches which makes a compact solution. This makes the OPAx863 devices suitable for flow measurements in large diameter pipes and non-intrusive flow meters. The TIDM-02003 reference design discusses an ultrasonic gas flow sensing subsystem which uses high-speed amplifiers for front-end amplification.

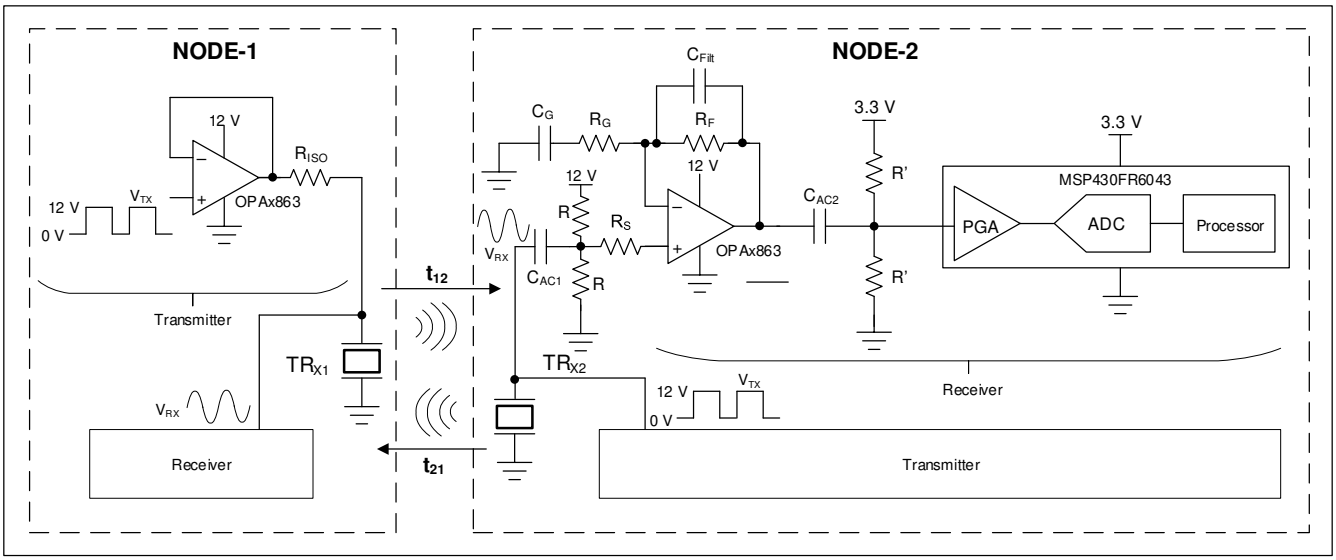

图 9-6. Non-Intrusive Ultrasonic Flow Meter

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10 Power Supply Recommendations

The OPAx863 devices are intended to operate on supplies ranging from 2.7 V to 12.6 V. The OPAx863 devices may operate on single-sided supplies, split and balanced bipolar supplies, or unbalanced bipolar supplies. Operating from a single supply can have numerous advantages. The DC errors, due to the –PSRR term, can be minimized with the negative supply at ground. Typically, AC performance improves slightly at 10-V operation with minimal increase in supply current. Minimize the distance (< 0.1 in) from the power supply pins to high-frequency, 0.01-µF decoupling capacitors. A larger capacitor (2.2 µF typical) is used along with a high-frequency, 0.01-µF supply-decoupling capacitor at the device supply pins. Only the positive supply has these capacitors for single-supply operation. Use these capacitors from each supply to ground when a split-supply is used. If necessary, place the larger capacitors further from the device and share these capacitors among several devices in the same area of the printed circuit board (PCB). An optional supply decoupling capacitor across the two power supplies (for split-supply operation) reduces second harmonic distortion.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier (like the OPAx863 devices) require careful attention to board layout parasitics and external component types. The *OPA2863 DGK Evaluation Module* user's guide can be used as a reference when designing the circuit board. Recommendations that optimize performance includes the following:

1. **Minimize parasitic capacitance** to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability on the noninverting input and can react with the source impedance to cause unintentional band-limiting. Open a window around the signal I/O pins in all of the ground and power planes around those pins to reduce unwanted capacitance. Otherwise, ground and power planes must be unbroken elsewhere on the board.
2. **Minimize the distance** (< 0.1 in) from the power-supply pins to high-frequency 0.01-µF decoupling capacitors. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must also be used on the supply pins. These can be placed somewhat farther from the device and shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserve the high frequency performance of the OPAx863 devices.** Resistors must be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Keep resistor values as low as possible and consistent with load driving considerations. Lowering the resistor values keep the resistor noise terms low and minimize the effect of its parasitic capacitance; lower resistor values, however, increase the dynamic power consumption because R_F and R_G become part of the amplifiers output load network.

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11.1.1 Thermal Considerations

The OPAx863 does not require heat sinking or airflow in most applications. The maximum allowed junction temperature sets the maximum allowed internal power dissipation. Do not allow the maximum junction temperature to exceed 150°C.

Operating junction temperature (T_J) is given by,

$$T_J = T_A + P_D \times R_{\Theta JA} \quad (4)$$

where,

- T_A is the ambient temperature
- P_D is the total power dissipation internal to the amplifier
- $R_{\Theta JA}$ is the junction-to-ambient thermal resistance

The total power dissipation $P_D = P_{DQ} + P_{DL}$

where, $P_{DQ} = (V_{S+} - V_{S-}) \times I_Q$, is the power dissipation due to amplifier's quiescent current

and $P_{DL}(max) = V_S{}^2 / (4 \times R_L)$, is the internal power dissipation due to output load current

As a worst-case example, compute the maximum T_J using an OPA2863-DGK (VSSOP package) configured as a unity gain buffer, operating on ±6-V supplies at an ambient temperature of 25°C and driving a grounded 500-Ω load.

$$P_D = 12\ V \times 2\ mA + 6^2 / (4 \times 500\ \Omega) = 42\ mW \quad (5)$$

Maximum T_J = 25°C + (0.042 W × 180.3°C/W) = 33°C, which is well below the maximum allowed junction temperature of 150°C.

11.2 Layout Example

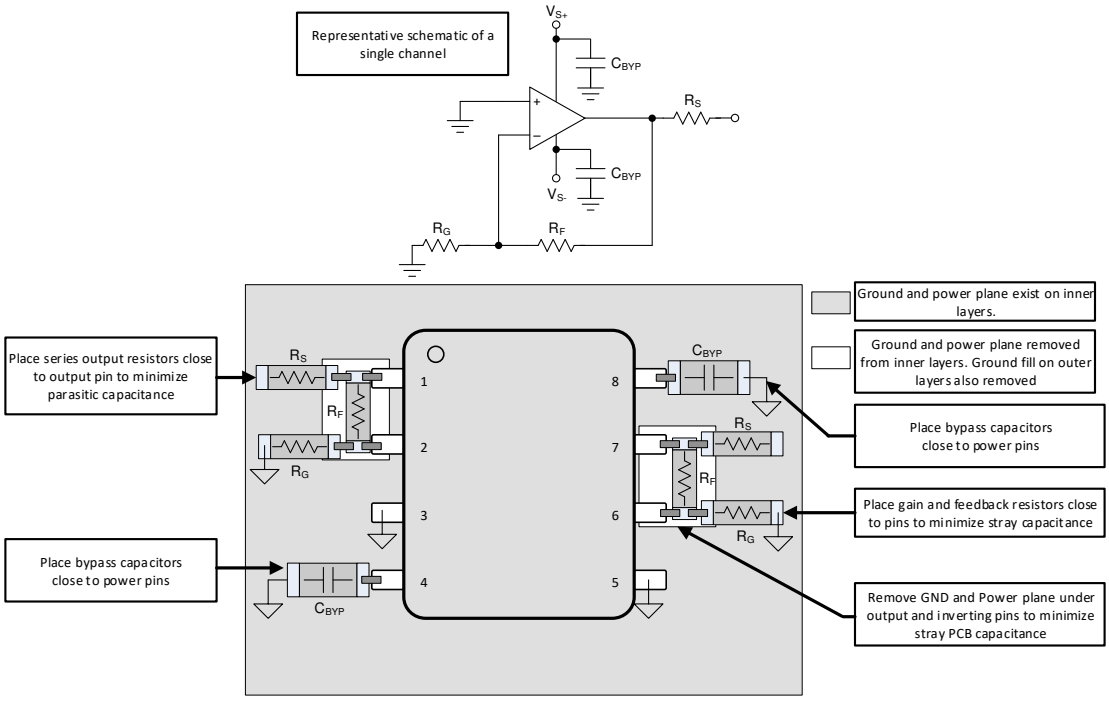

图 11-1. Layout Recommendation for Dual-Channel DGK Package

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *OPA2863ADGK Evaluation Module* user's guide
- Texas Instruments, *Single-Supply Op Amp Design Techniques* application report

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2863DR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O2863D	Samples
OPA2863IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	2FJ4	Samples
OPA2863RUNR	ACTIVE	QFN	RUN	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	O263	Samples
OPA863SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	O863	Samples
POPA2863DR	ACTIVE	SOIC	D	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XOPA2863RUNR	ACTIVE	QFN	RUN	10	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XOPA4863IPWR	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		Samples
XOPA863IDBVR	ACTIVE	SOT-23	DBV	6	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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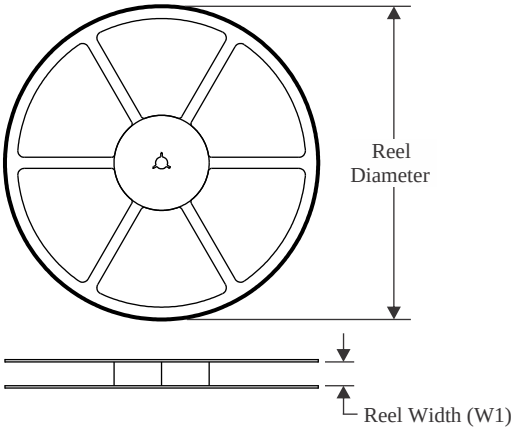
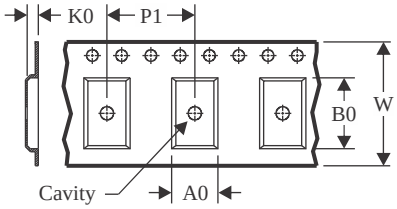
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

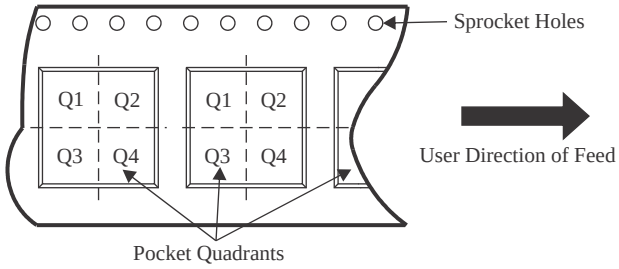


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

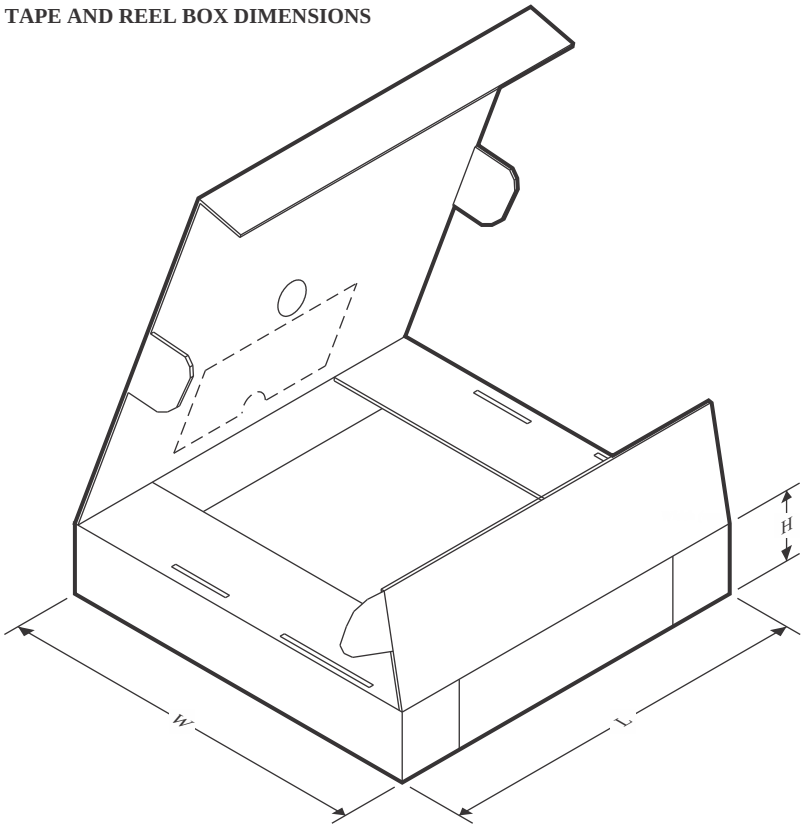
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2863DR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2863IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2863RUNR	QFN	RUN	10	3000	180.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
OPA863SIDBVR	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

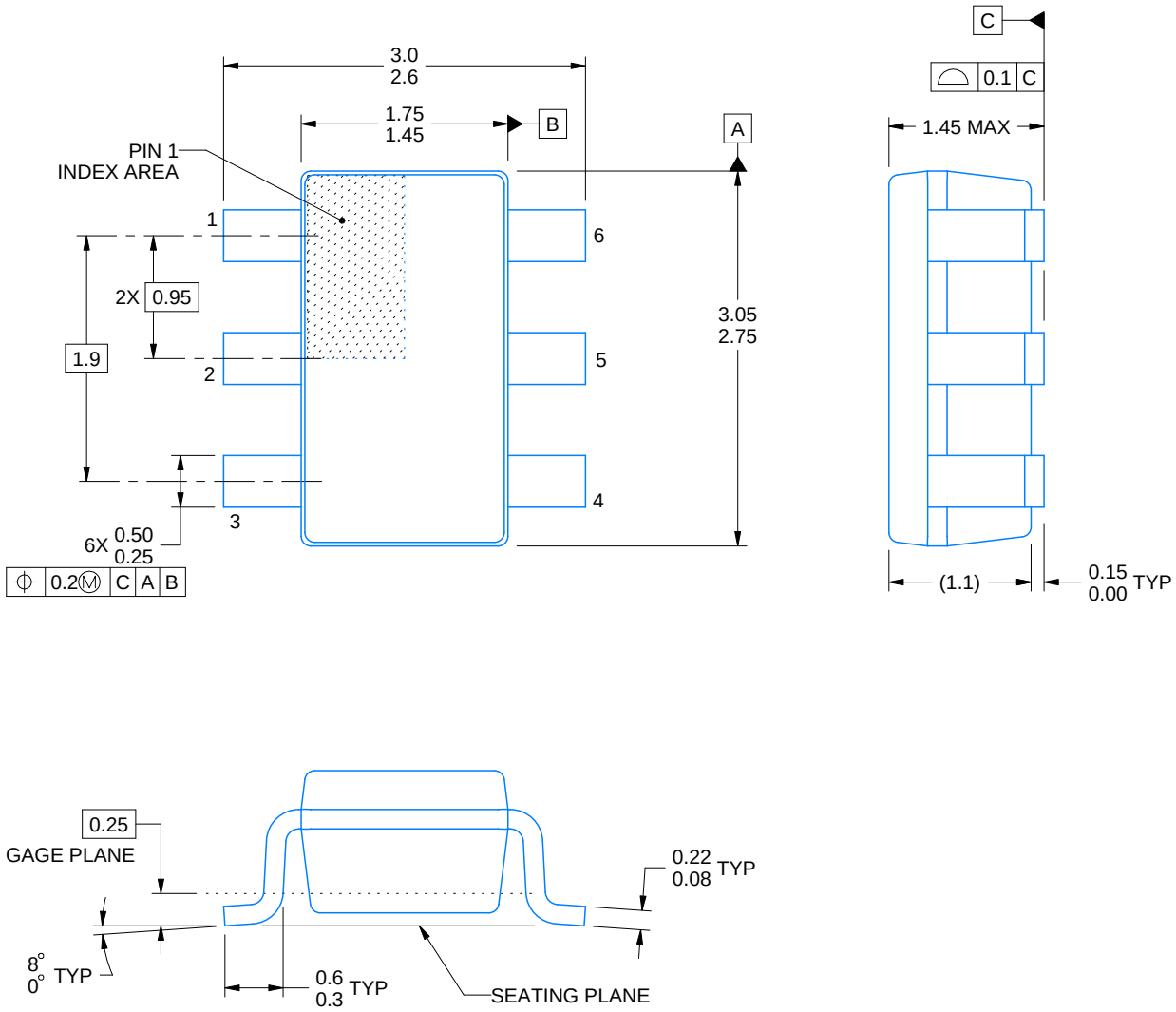
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2863DR	SOIC	D	8	3000	356.0	356.0	35.0
OPA2863IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2863RUNR	QFN	RUN	10	3000	213.0	191.0	35.0
OPA863SIDBVR	SOT-23	DBV	6	3000	190.0	190.0	30.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

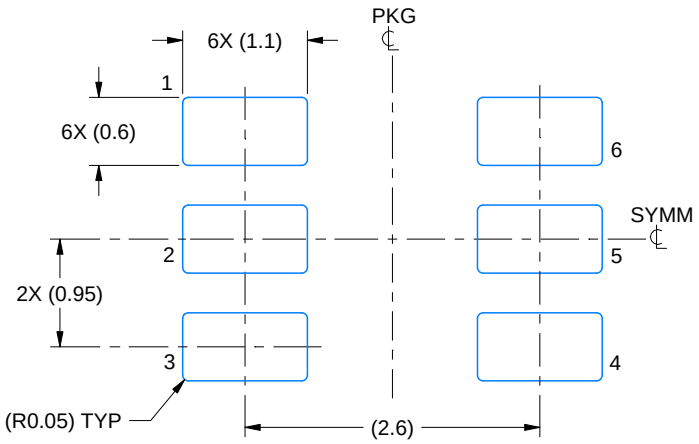
SMALL OUTLINE TRANSISTOR



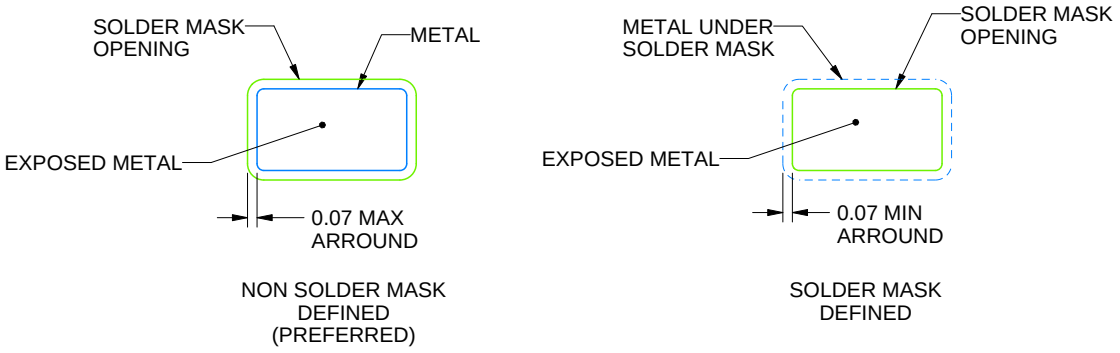
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

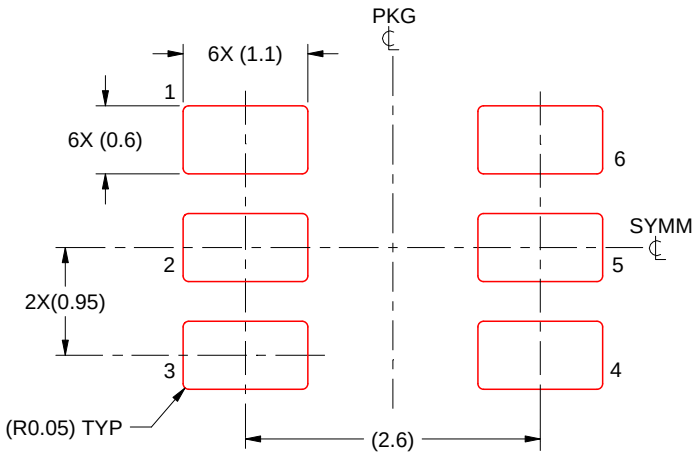


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



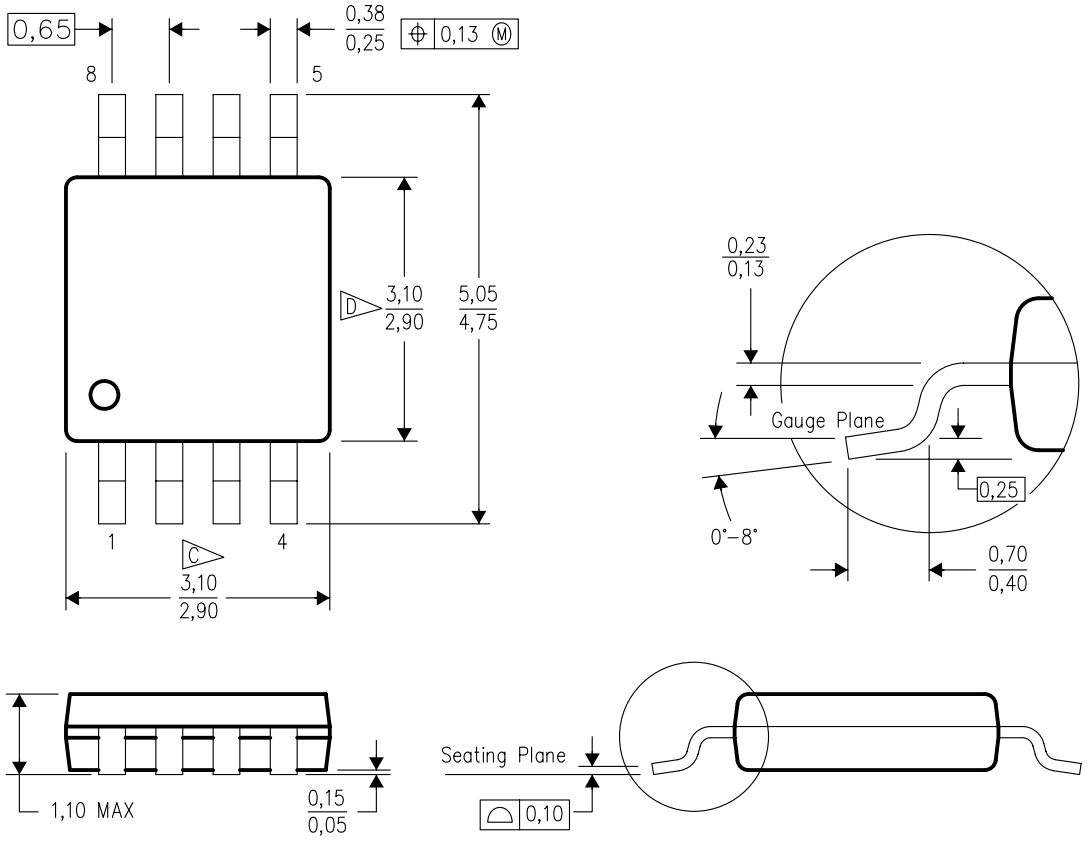
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

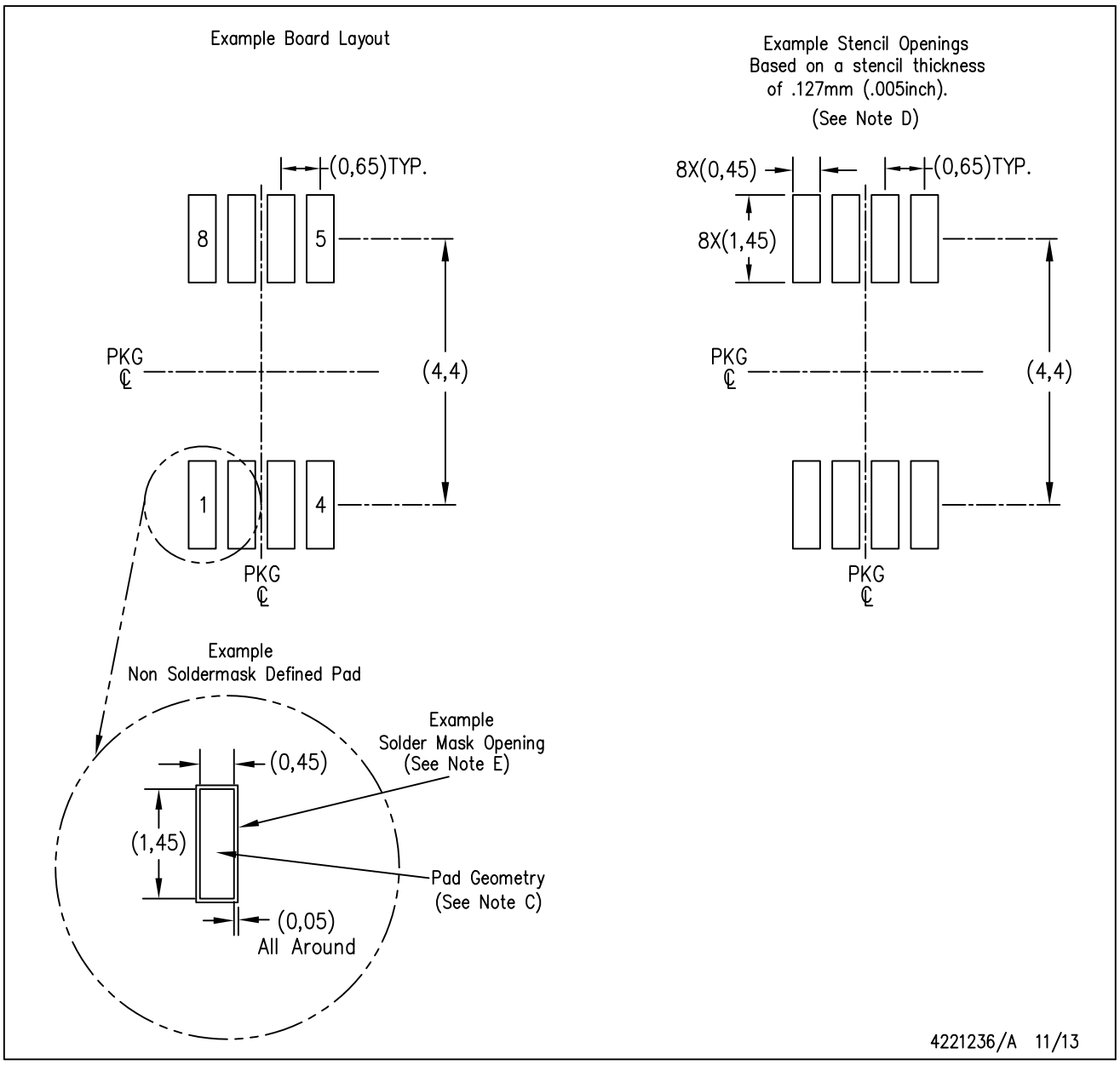
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

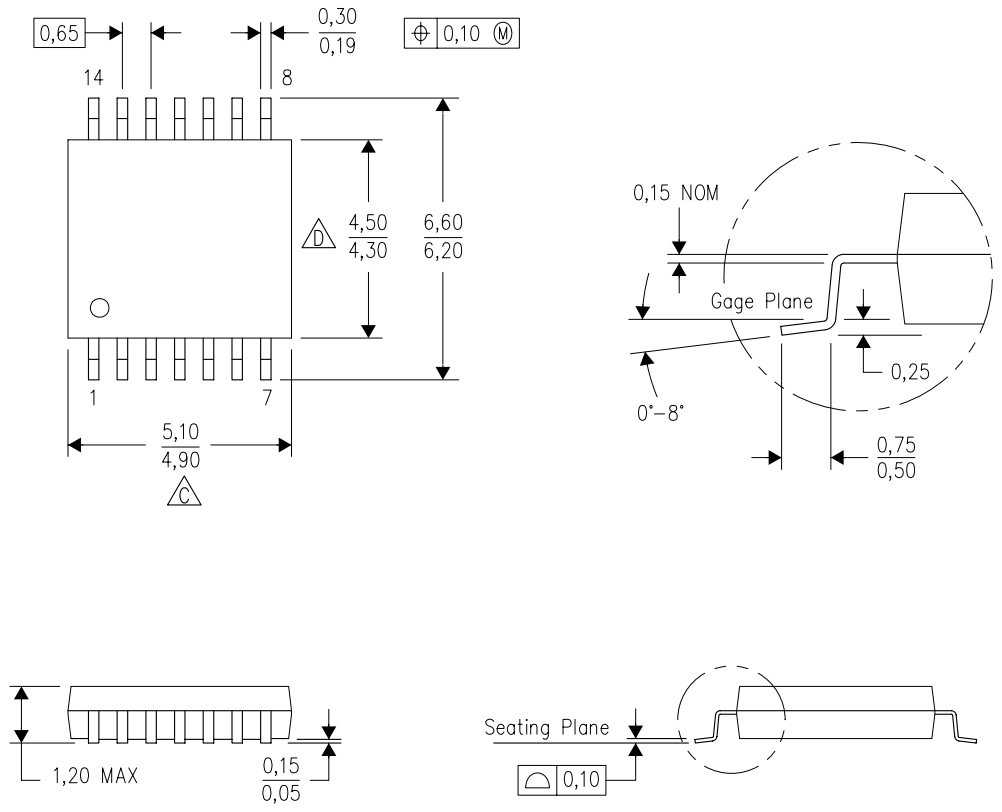
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

GENERIC PACKAGE VIEW

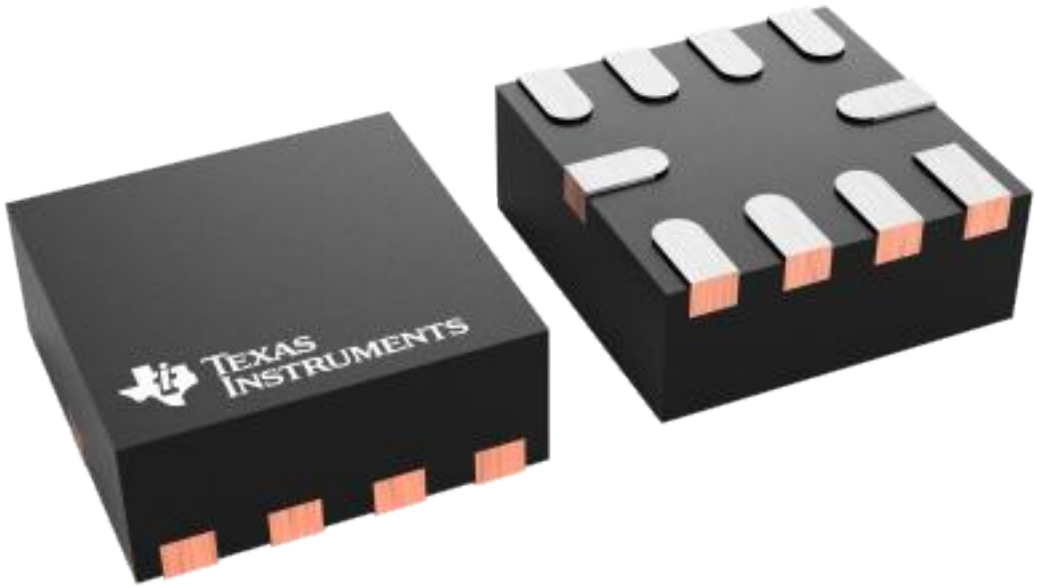
RUN 10

WQFN - 0.8 mm max height

2 X 2, 0.5 mm pitch

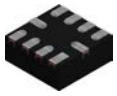
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4228249/A

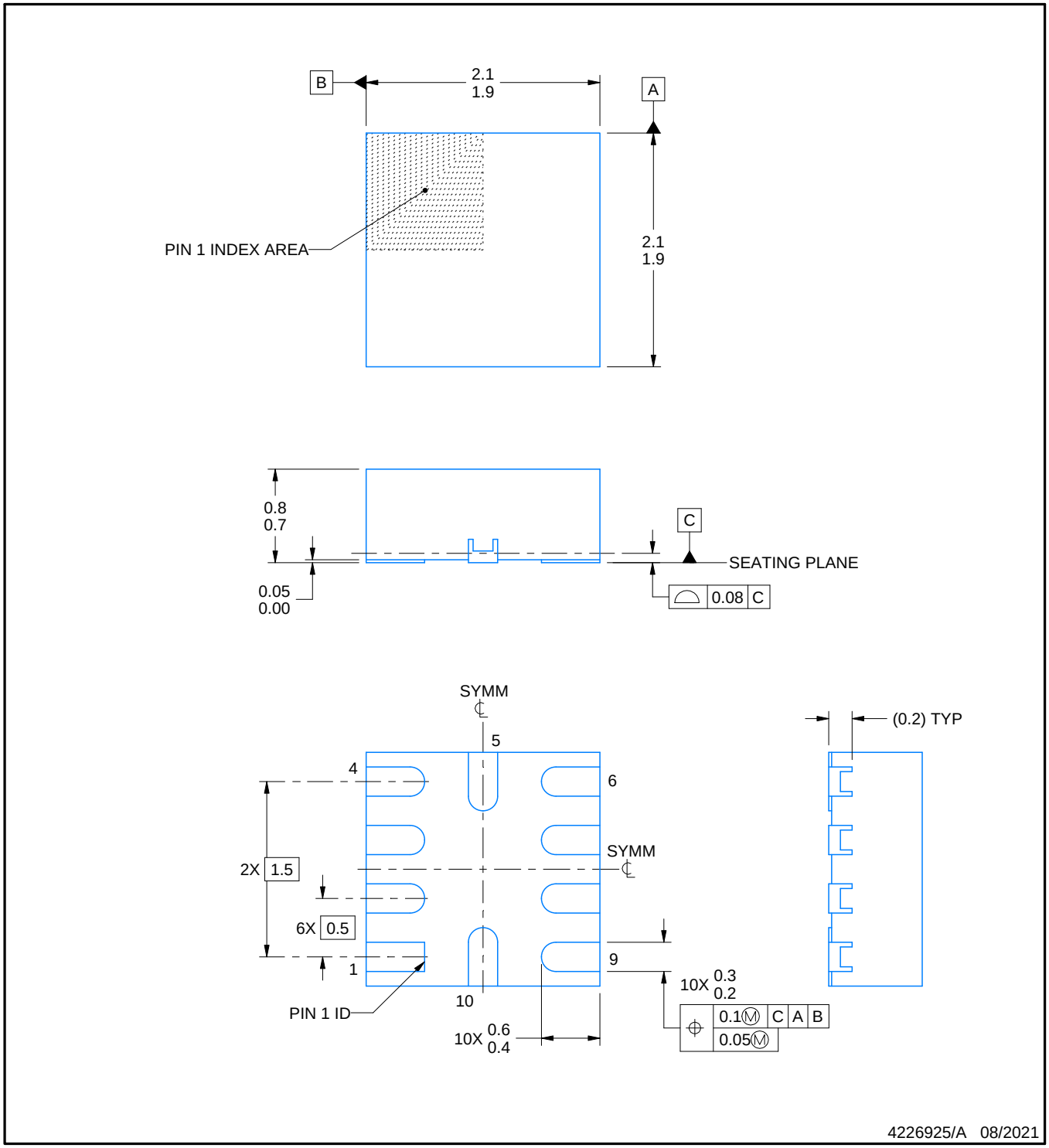
RUN0010B



PACKAGE OUTLINE

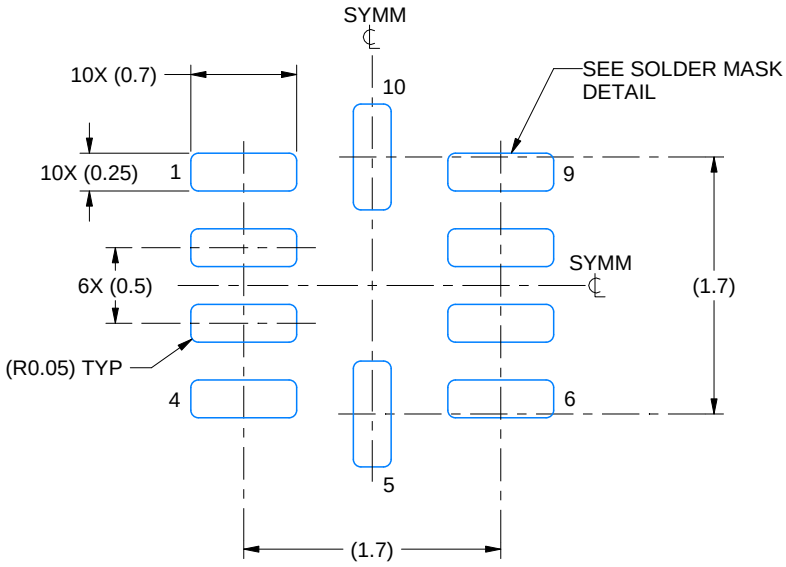
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

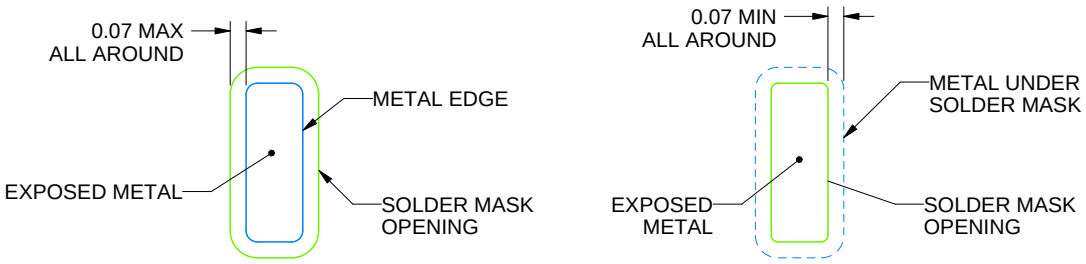


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4226925/A 08/2021

NOTES: (continued)

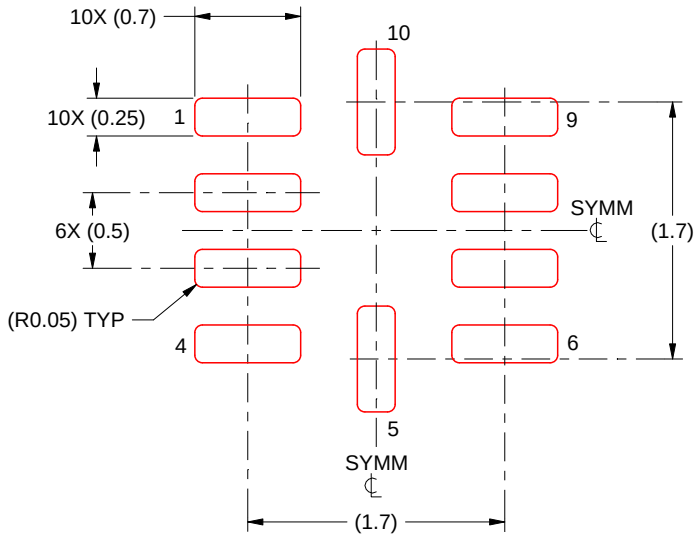
3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUN0010B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

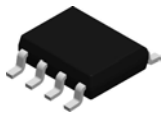


SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4226925/A 08/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

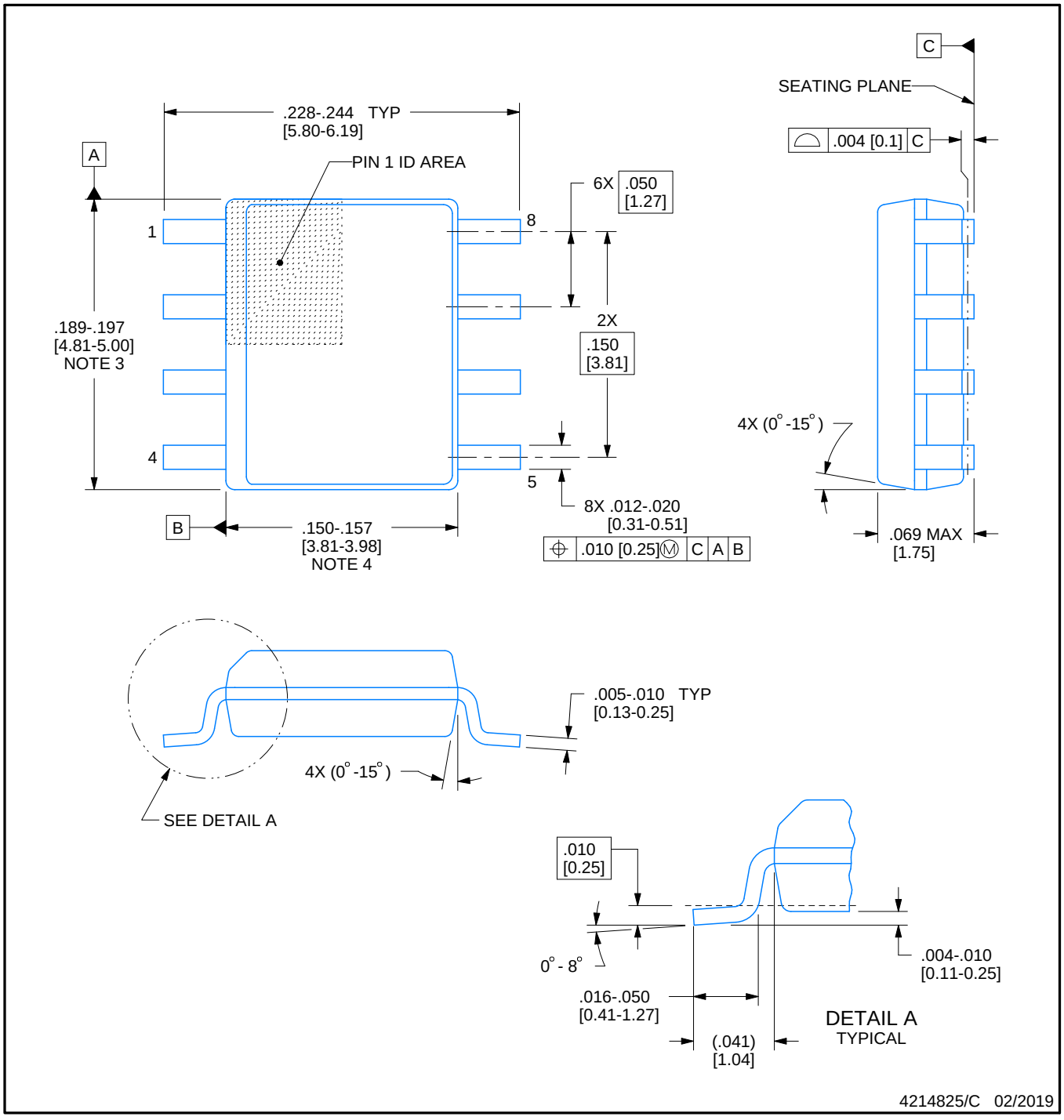


PACKAGE OUTLINE

D0008A

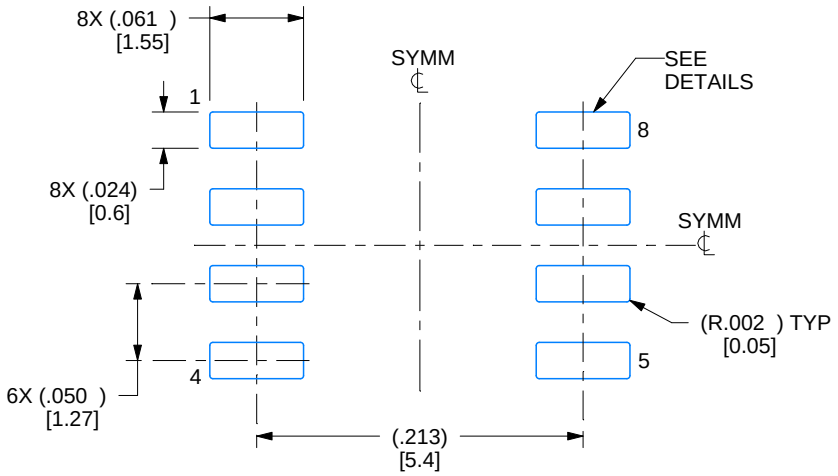
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

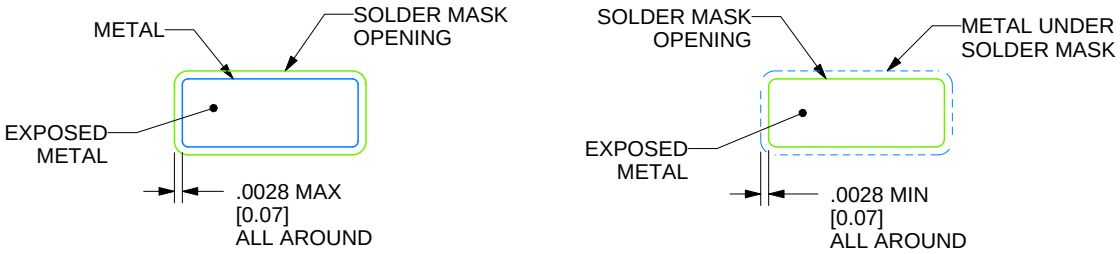


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

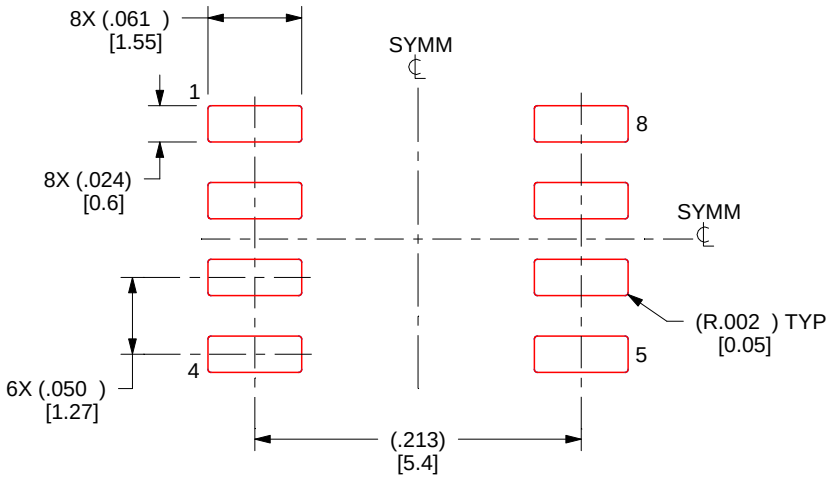
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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