

REF1112 10ppm/°C、1μA、1.25V 分流器电压基准

1 特性

- 小型封装：SOT23-3
- 1.25V 固定反向击穿电压
- 主要技术规格
 - 输出电压容差：±0.2%（最大值）
 - 低输出噪声（0.1Hz 至 10Hz）：25μV_{pp}（典型值）
 - 温度范围：-40°C 至 +125°C
 - 工作电流范围：1.2μA 至 5mA
 - 0°C 至 +70°C 的低温度系数：30ppm/°C（最大值）
 - -40°C 至 +85°C 的低温度系数：50ppm/°C（最大值）

2 应用

- 电池供电仪器
- 楼宇安防传感器
- 医疗设备
- 现场发送器
- 校准仪

3 说明

REF1112 器件是一种两端并联基准，适用于对功耗和空间敏感的应用供电的绝佳器件。REF1112 在 SOT23-3 封装中的工作电流为 1μA，是当前在较大封装（如 REF1004 和 LT1004）中使用电压基准的设计所适用的改进型低功耗解决方案。REF1112 的额定工作温度范围是 -40°C 至 +85°C，扩展工作温度范围是 -40°C 至 +125°C。

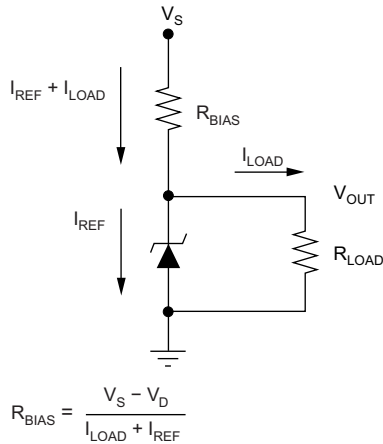
REF1112 完善了德州仪器 (TI) 的其他 1μA 组件（包括 OPA349 和 TLV240x 低功耗运算放大器以及 TLV349x 微功耗电压比较器）。

器件信息⁽¹⁾

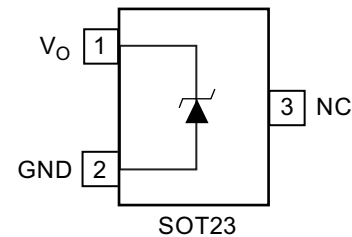
器件型号	封装	封装尺寸（标称值）
REF1112	SOT-23 (3)	2.92mm × 1.3mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

并联基准应用原理图



引脚分配



(1) NC 表示引脚应该保持未连接状态或连接至 GND



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4 修订历史记录

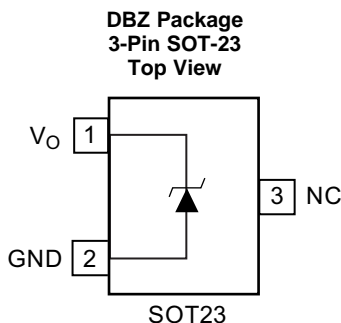
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (March 2008) to Revision D

Page

• 添加了器件信息表、引脚配置和功能部分、绝对最大额定值表、ESD 额定值表、建议运行条件表、热性能信息表、特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。	1
• 已更改特性部分	1
• 将重要图形文本注意事项从“NC 表示引脚应该保持未连接状态”更改为“NC 表示引脚应该保持未连接状态或连接至 GND”	1
• 删除了封装/订购信息表，并将该信息移到机械、封装和可订购信息部分	13

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V _O	1	I/O	Shunt Current/Voltage input
GND	2	O	Ground connection
NC	3	-	Must float or connect to GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Reverse breakdown current		10	mA
Forward current		10	mA
Operating temperature	-55	125	°C
Junction temperature		150	°C
Storage temperature, T _{stg}	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT	
I _{REF}	Reverse current	0.0012	5	mA
T _A	Operating temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		REF1112	
		DBZ (SOT-23)	
		3 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	219	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	79.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

$V_R = 1.25\text{ V}$, $T_A = +25^\circ\text{C}$, $I_{REF} = 1.2\ \mu\text{A}$ and $C_{LOAD} = 10\ \text{nF}$, unless otherwise noted.

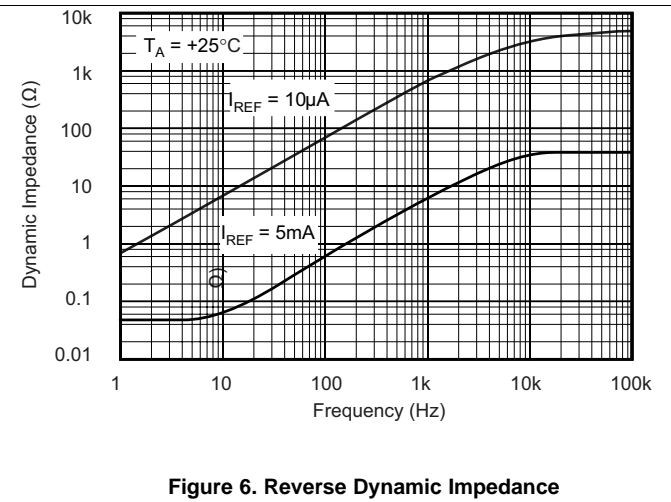
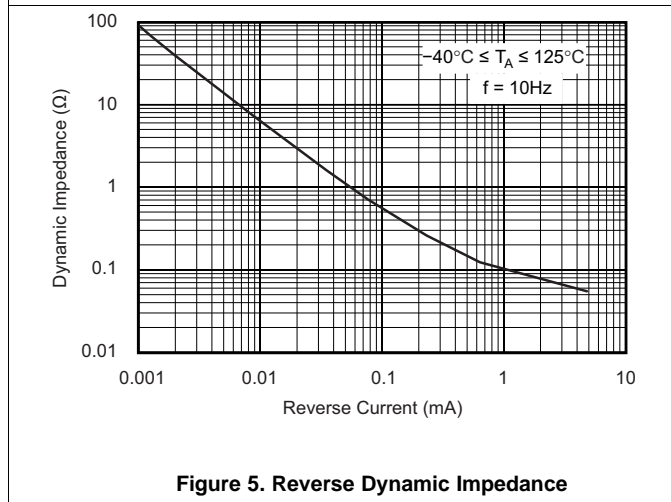
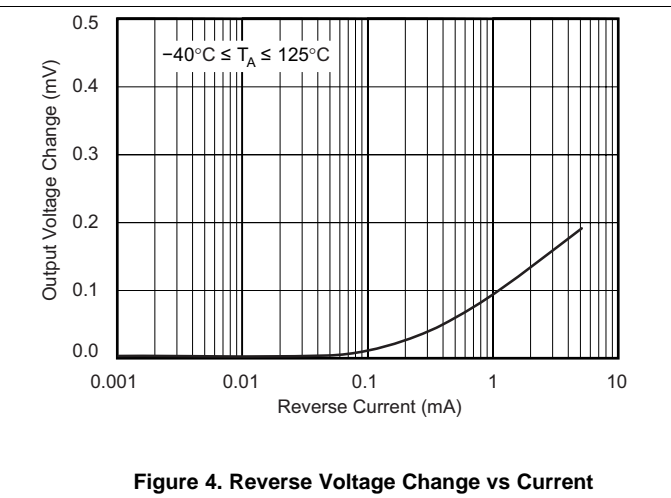
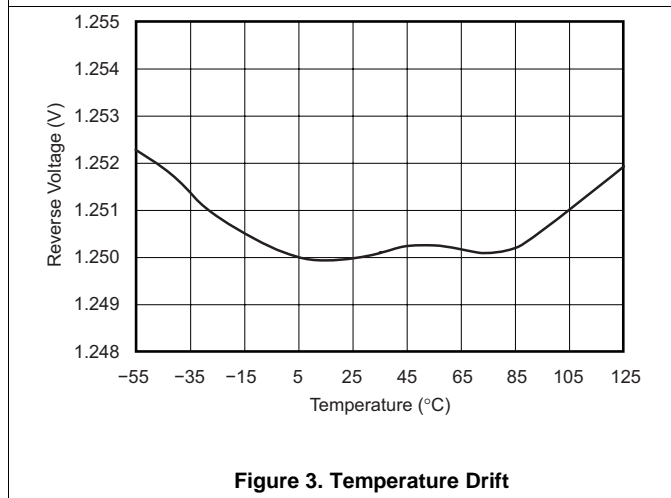
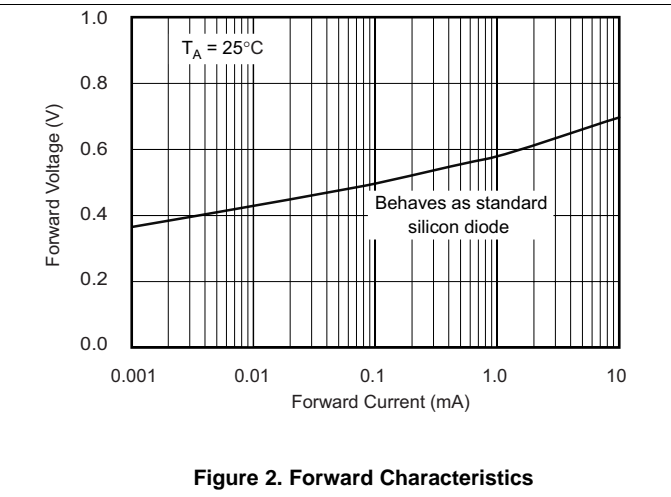
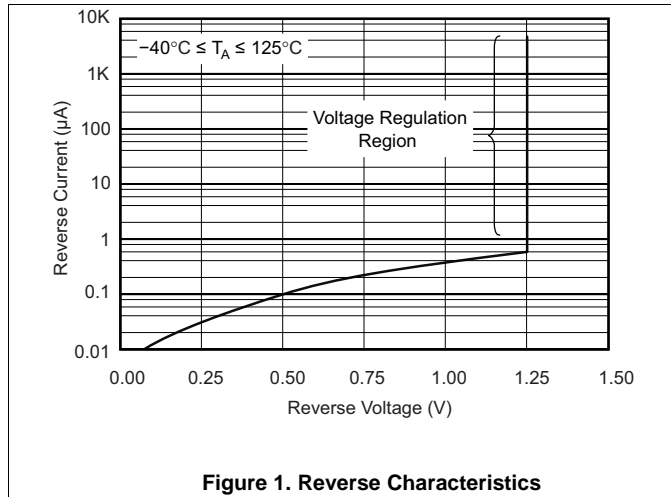
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_R	Reverse breakdown voltage	$I_{REF} = 1.2\ \mu\text{A}$	1.2475	1.25	1.2525	V
			-0.2%		0.2%	
ΔV_R	Temperature coefficient	$1.2\ \mu\text{A} \leq I_{REF} \leq 5\ \text{mA}$, $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$		10	30	ppm/°C
		$1.5\ \mu\text{A} \leq I_{REF} \leq 5\ \text{mA}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		15	50	
		$1.5\ \mu\text{A} \leq I_{REF} \leq 5\ \text{mA}$, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		15		
I_{RMIN}	Minimum operating current			1	1.2	μA
$\Delta V_R / \Delta I_R$	Reverse breakdown voltage change with current	$1.2\ \mu\text{A} \leq I_{REF} \leq 5\ \text{mA}$		30	100	ppm/mA
Z_R	Reverse dynamic impedance	$1.2\ \mu\text{A} \leq I_{REF} \leq 5\ \text{mA}$		0.037	0.125	Ω
e_N	Low-frequency noise ⁽¹⁾	$0.1\ \text{Hz} \leq I_{REF} \leq 10\ \text{Hz}$		25		μV_{PP}
V_{HYST}	Thermal hysteresis ⁽²⁾			100		ppm
ΔV_R	Long-term stability	$+25^\circ\text{C} \pm 0.1^\circ\text{C}$		60		ppm/kHr

(1) Peak-to-peak noise is measured with a 2-pole high-pass filter at 0.1 Hz and a 4-pole, low-pass Chebyshev filter at 10 Hz.

(2) Thermal hysteresis is defined as the change in output voltage after operating the device at $+25^\circ\text{C}$, cycling the device through the specified temperature range, and returning to $+25^\circ\text{C}$.

6.6 Typical Characteristics

At $T_A = +25^\circ\text{C}$, $I_{\text{REF}} = 10 \mu\text{A}$ and $C_{\text{LOAD}} = 10 \text{ nF}$, unless otherwise noted.



Typical Characteristics (continued)

At $T_A = +25^\circ\text{C}$, $I_{REF} = 10 \mu\text{A}$ and $C_{LOAD} = 10 \text{ nF}$, unless otherwise noted.

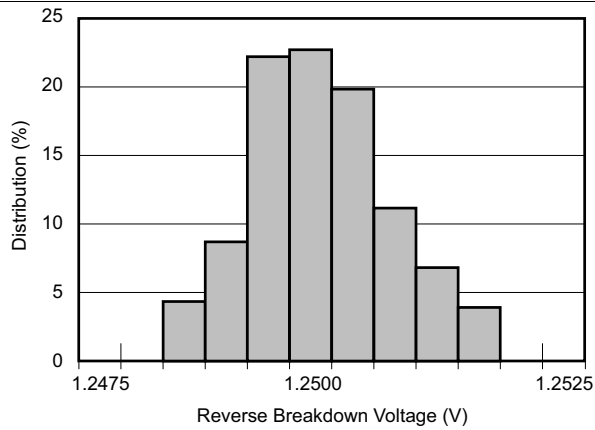


Figure 7. Reverse Breakdown Voltage Distribution

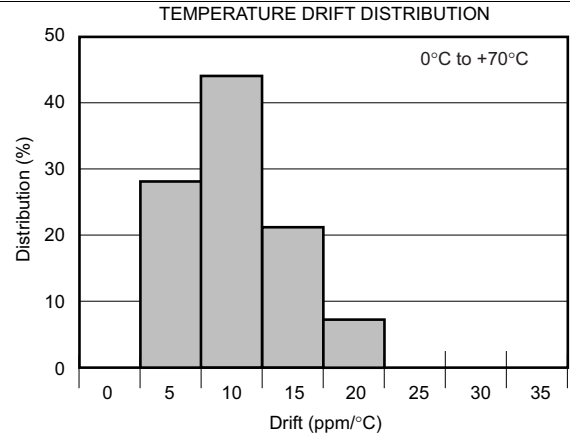


Figure 8. Temperature Drift Distribution

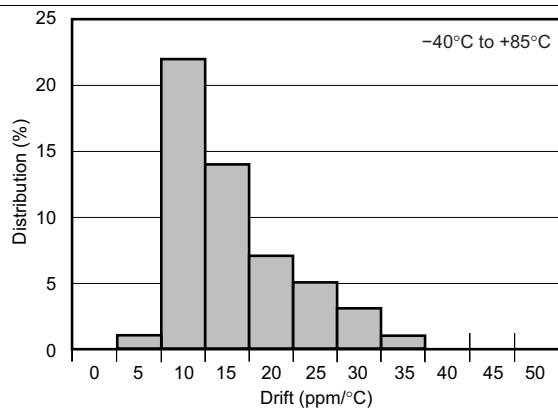


Figure 9. Temperature Drift Distribution

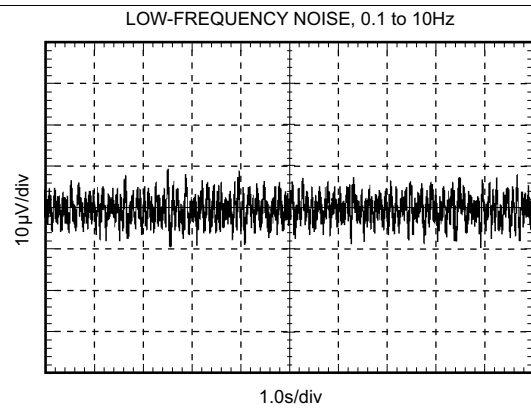


Figure 10. Low-Frequency Noise, 0.1 to 10Hz

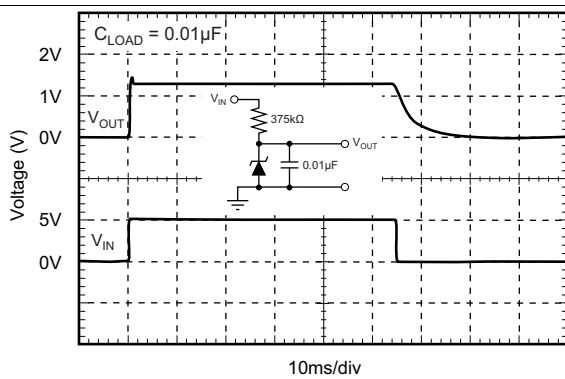


Figure 11. Response Time

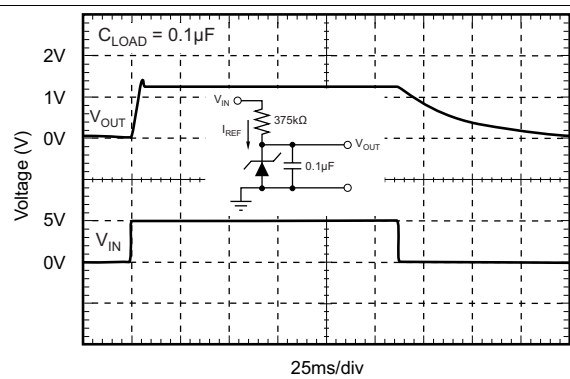


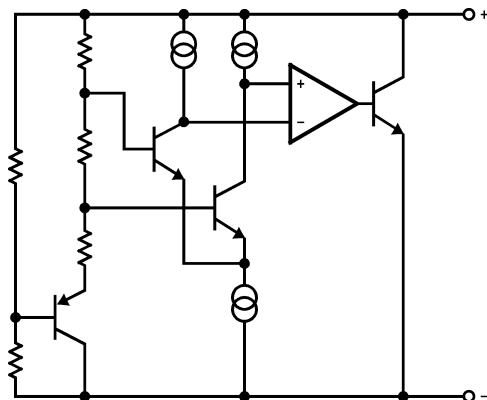
Figure 12. Response Time

7 Detailed Description

7.1 Overview

The REF1112 is a 2-terminal bandgap reference diode designed for high accuracy with outstanding temperature characteristics at low operating currents. Precision thin-film resistors result in 0.2% initial voltage accuracy and 50ppm/°C maximum temperature drift. The REF1112 is specified from –40°C to +85°C, with operation from –40°C to +125°C, and is offered in a SOT23-3 package.

7.2 Functional Block Diagram



7.3 Feature Description

The REF1112 device is effectively a precision Zener diode. The part requires a small quiescent current for regulation, and regulates the output voltage by shunting more or less current to ground, depending on input voltage and load. The only external component requirements are a resistor between the cathode and the input voltage to set the input current and an external capacitor at the output to maintain stability under varying loads.

7.4 Device Functional Modes

The REF1112 device is a fixed output voltage part where the feedback is internal. Therefore, the part can only operate in a closed-loop mode and the output voltage cannot be adjusted. The output voltage will remain in regulation as long as I_{REF} is between I_{REFMIN} (see [Electrical Characteristics](#)) and I_{REFMAX} is 5 mA. A proper selection of the external resistor for input voltage range and load current range will ensure these conditions are met.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Typical connections for the REF1112 are shown in [Figure 13](#). A minimum 1- μ A bias current is required to maintain a stable output voltage and can be provided with a resistor connected to the supply voltage. I_{BIAS} depends on the values selected for R_{BIAS} and V_S , and will vary as a sum of the minimum operating current and the load current. To maintain stable operation, the value of R_{BIAS} must be low enough to maintain the minimum operating current at the minimum and maximum load and supply voltage levels.

A 0.1- μ F load capacitor is recommended to maintain stability under varying load conditions. A minimum 0.01- μ F load capacitor is required for stable operation. Start-up time for the REF1112 will be affected, depending on the value of load capacitance and the bias currents being used. A 1- μ F power-supply bypass capacitor is recommended to minimize supply noise within the circuit. The REF1112 shunt voltage reference provides a versatile function for low power and space-conservative applications.

8.2 Typical Applications

8.2.1 Shunt Regulator

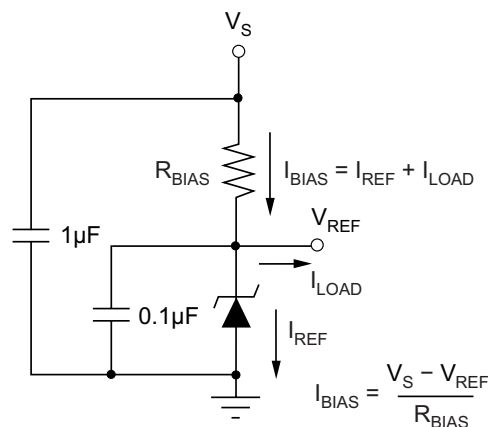


Figure 13. Typical Connections

8.2.1.1 Design Requirements

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage	3 V
Cathode current (I_{REF})	1.2 μ A
Load Current (I_{LOAD})	50 μ A

8.2.1.2 Detailed Design Procedure

When using the REF1112 as a reference, determine the following:

- Supply voltage range
- Current source resistance
- Reference voltage accuracy

To design using the REF1112, is it important to ensure that the V_S is larger than V_{REF} .

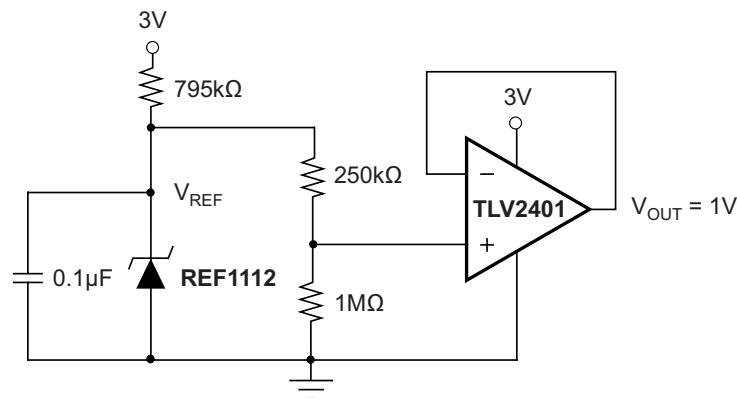
The resistor R_{BIAS} sets the cathode current of the REF1112, I_R . Ensure that this current remains in the operational region of the part for the entire V_S and load range.

Using this information, select a R_{BIAS} such that:

$$I_{REFMIN} < I_{REF} < I_{REFMAX} \text{ where } I_{REFMAX} = 5 \text{ mA.}$$

In this application the I_{REF} is the operating current of the REF1112 plus the maximum possible I_{LOAD} under no-load conditions.

8.2.2 MicroPOWER 3- μ A, 1-V Voltage Reference



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Figure 14. MicroPOWER 3- μ A, 1-V Voltage Reference

8.2.2.1 Design Requirements

The REF1112 can be scaled to provide extremely low power reference voltages. [Figure 14](#) shows the REF1112 used as a 1-V V_{OUT} , 3- μ A voltage reference.

8.2.2.2 Detailed Design Procedure

Set R_{BIAS} such that the current through the shunt reference, I_{REF} , is greater than $I_{REFMIN} + I_{LOAD}$.

Use a resistor divider to set the required voltage to the input of the amplifier. The TLV2401 requires an input bias current maximum of 350 pA which allows the use of larger resistor values to save power.

8.2.3 2.5-V Reference on 1 μA

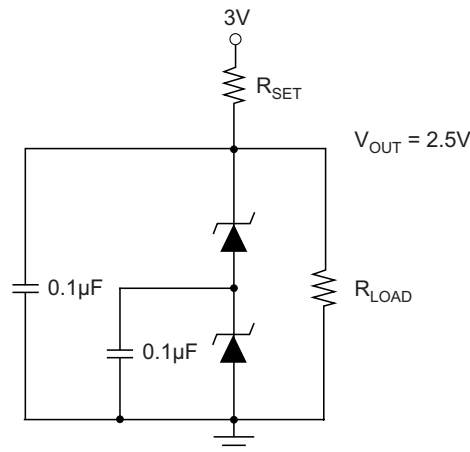


Figure 15. 2.5-V Reference on 1 μA

8.2.3.1 Design Requirements

Create a 2.5-V reference that consumes 1 μA of I_{REF} .

8.2.3.2 Detailed Design Procedure

Figure 15 shows the REF1112 used as a 2.5-V reference on 1 μA . This is done by stacking the REF1112 in series.

$$V_{\text{OUT}} = 2 \times V_{\text{REF}}$$

where

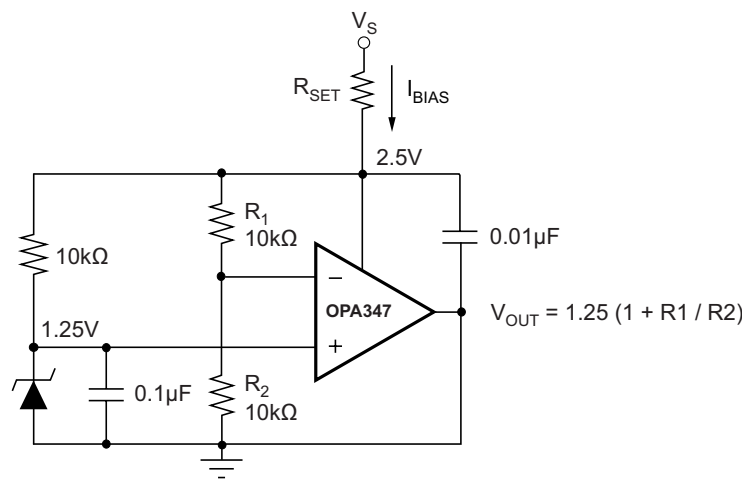
- V_{REF} is the reference voltage (1)

In this case, $V_{\text{OUT}} = 2 \times 1.25 \text{ V} = 2.5 \text{ V}$

The I_{BIAS} is still 1 μA because the stacked REF1112 are in series.

8.2.4 Adjustable Voltage Shunt Reference

For applications requiring a stable voltage reference capable of sinking higher than 5 mA of current, a REF1112 combined with an OPA347 can sink up to 10 mA of current. This configuration is shown in Figure 16, and through appropriate selection of R_1 and R_2 , can be used to provide a wide range of stable reference voltages.



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Figure 16. Adjustable Voltage Shunt Reference

8.2.5 Level Shift to Achieve Full ADC Input Range

The REF1112 is also useful for level shifting, and as shown in Figure 17, can be used to achieve the full input range of an analog-to-digital converter (ADC).

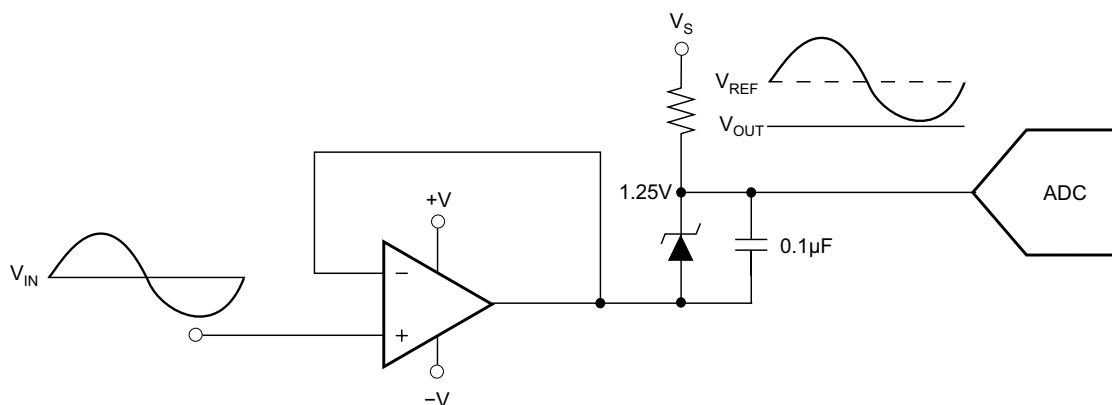


Figure 17. REF1112 Provides a Level Shift to Achieve Full ADC Input Range

8.2.6 Stable Current Source

The REF1112 can be configured with an additional diode and NPN transistor to provide a temperature compensated current reference as shown in Figure 18.

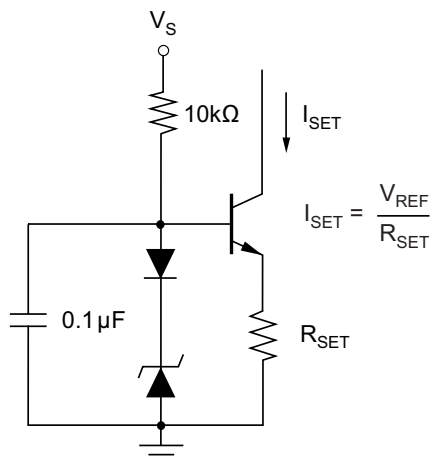


Figure 18. REF1112 as a Stable Current Source

9 Power Supply Recommendations

While a bypass capacitor is not required on the input voltage line, TI recommends reducing noise on the input which could affect the output. A 0.1- μ F ceramic capacitor or larger is recommended.

10 Layout

10.1 Layout Guidelines

Place decoupling capacitors as close to the device as possible. Use appropriate widths for traces when shunting high currents to avoid excessive voltage drops.

10.2 Layout Example

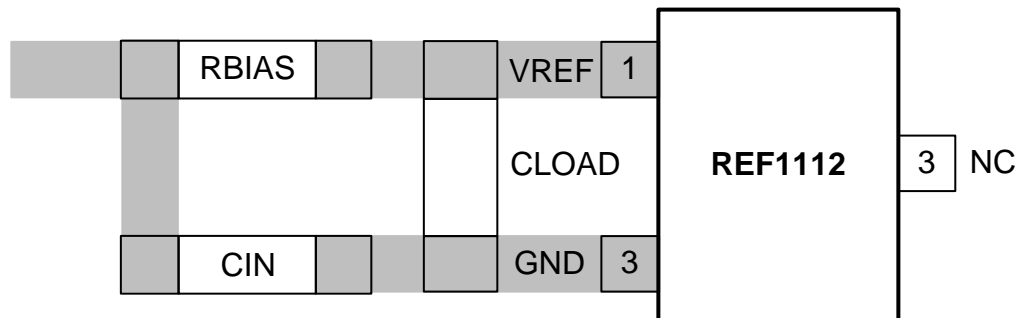


Figure 19. Layout Example

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。请单击右上角的 **提醒我** 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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11.3 商标

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11.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，也不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF1112AIDBZR	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R11A	Samples
REF1112AIDBZRG4	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R11A	Samples
REF1112AIDBZT	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R11A	Samples
REF1112AIDBZTG4	ACTIVE	SOT-23	DBZ	3	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	R11A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF1112AIDBZR	SOT-23	DBZ	3	3000	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3
REF1112AIDBZT	SOT-23	DBZ	3	250	179.0	8.4	3.15	2.95	1.22	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

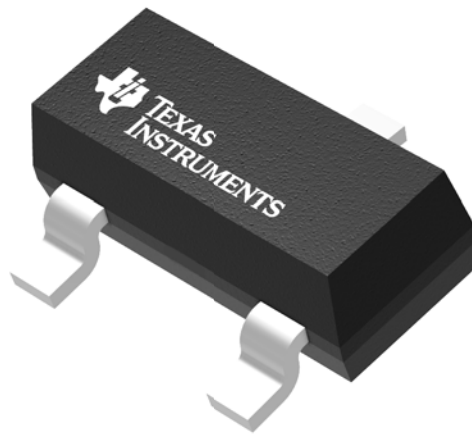
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF1112AIDBZR	SOT-23	DBZ	3	3000	200.0	183.0	25.0
REF1112AIDBZT	SOT-23	DBZ	3	250	200.0	183.0	25.0

GENERIC PACKAGE VIEW

DBZ 3

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203227/C

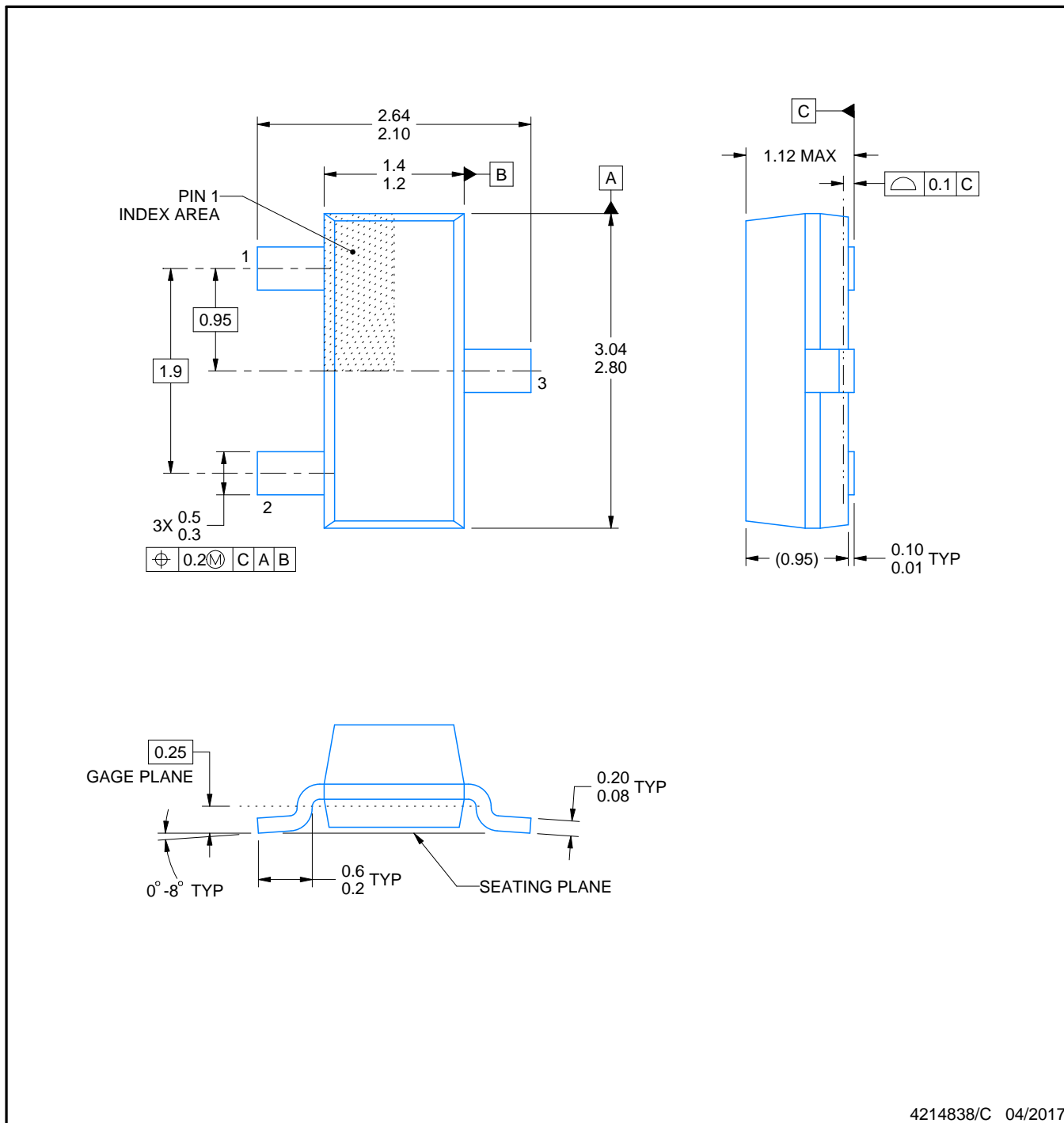
DBZ0003A



PACKAGE OUTLINE

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



4214838/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.

EXAMPLE BOARD LAYOUT

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214838/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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