

具有施密特触发输入的 SN74HCS02-Q1 汽车类四路双输入或非门

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
 - 器件温度等级 1: -40°C 至 $+125^{\circ}\text{C}$, T_A
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C6
- 宽工作电压范围: 2V 至 6V
- 施密特触发输入可实现慢速或高噪声输入信号
- 低功耗
 - I_{CC} 典型值为 100nA
 - 输入泄漏电流典型值为 $\pm 100\text{nA}$
- 电压为 5V 时, 输出驱动为 $\pm 7.8\text{mA}$

2 应用

- 警报/篡改检测电路
- S-R 锁存

3 说明

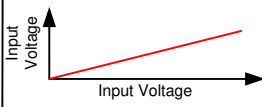
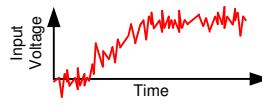
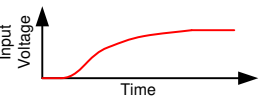
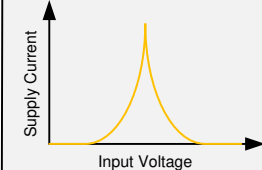
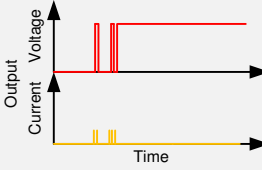
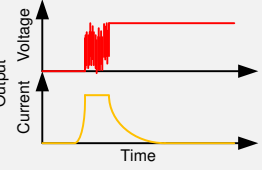
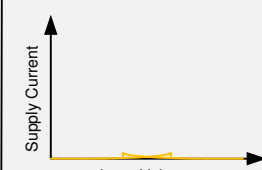
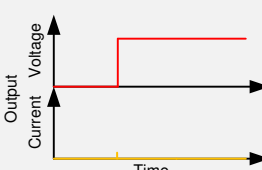
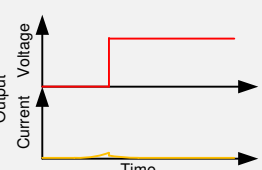
此器件包含四个具有施密特触发输入的独立双输入或非门。每个逻辑门以正逻辑执行布尔函数 $Y = \overline{A + B}$ 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN02HCS74QDRQ1	SOIC (14)	8.70mm × 3.90mm
SN02HCS74QPWRQ1	TSSOP (14)	5.00mm × 4.40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

施密特触发输入的优势

	Low Power	Noise Rejection	Supports Slow Inputs
Input Voltage Waveforms			
Standard CMOS Input Response Waveforms			
Schmitt-trigger CMOS Input Response Waveforms			

目录

1	特性	1	8.3	Feature Description	7
2	应用	1	8.4	Device Functional Modes	8
3	说明	1	9	Application and Implementation	9
4	修订历史记录	2	9.1	Application Information	9
5	Pin Configuration and Functions	3	9.2	Typical Application	9
6	Specifications	3	10	Power Supply Recommendations	12
6.1	Absolute Maximum Ratings	3	11	Layout	12
6.2	ESD Ratings	4	11.1	Layout Guidelines	12
6.3	Recommended Operating Conditions	4	11.2	Layout Example	12
6.4	Thermal Information	4	12	器件和文档支持	13
6.5	Electrical Characteristics	4	12.1	文档支持	13
6.6	Switching Characteristics	5	12.2	相关链接	13
6.7	Typical Characteristics	5	12.3	社区资源	13
7	Parameter Measurement Information	6	12.4	商标	13
8	Detailed Description	7	12.5	静电放电警告	13
8.1	Overview	7	12.6	Glossary	13
8.2	Functional Block Diagram	7	13	机械、封装和可订购信息	13

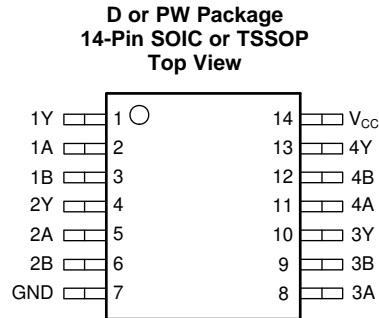
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (August 2019) to Revision B	Page
• Changed the recommended ambient temp from -55 to 125 C to -40 to 125 C	4
• Added D package column to <i>Thermal Information</i> table	4

Changes from Original (July 2019) to Revision A	Page
• Deleted "I _{CC} " and "output" from "Continuous current through V _{CC} or GND" row for clarity	3

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1Y	1	Output	Channel 1, Output Y
1A	2	Input	Channel 1, Input A
1B	3	Input	Channel 1, Input B
2Y	4	Output	Channel 2, Output Y
2A	5	Input	Channel 2, Input A
2B	6	Input	Channel 2, Input B
GND	7	—	Ground
3A	8	Input	Channel 3, Input A
3B	9	Input	Channel 3, Input B
3Y	10	Output	Channel 3, Output Y
4A	11	Input	Channel 4, Input A
4B	12	Input	Channel 4, Input B
4Y	13	Output	Channel 4, Output Y
V _{CC}	14	—	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		–0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < –0.5 or V _I > V _{CC} + 0.5		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _O < –0.5 or V _O > V _{CC} + 0.5		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature ⁽³⁾			150	°C
T _{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed. Do not exceed the absolute maximum voltage supply rating.

(3) Guaranteed by design.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2		6	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise and fall rate			Unlimited	ns/V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		SN74HCS02-Q1		UNIT
		PW (TSSOP)	D (SOIC)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	151.7	133.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.4	89.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94.7	89.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	25.2	45.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	94.1	89.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$	2 V to 6 V	$V_{CC} - 0.1$	$V_{CC} - 0.002$		V
			$I_{OH} = -6\ \text{mA}$	4.5 V	4.0	1.3		
			$I_{OH} = -7.8\ \text{mA}$	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$	2 V to 6 V		0.002	0.1	V
			$I_{OL} = 6\ \text{mA}$	4.5 V		0.18	0.30	
			$I_{OL} = 7.8\ \text{mA}$	6 V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6 V		±100	±1000	nA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V		0.1	2	μA
C_i	Input capacitance			2 V to 6 V			5	pF

Electrical Characteristics (continued)

over operating free-air temperature range; typical ratings measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance per gate	No load		10		pF

6.6 Switching Characteristics

over operating free-air temperature range; typical ratings measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	A or B	Y	2 V		16	36	ns
			4.5 V		7	13	
			6 V		6	12	
t_t	A or B	Y	2 V		7.7	13	ns
			4.5 V		4	6.1	
			6 V		3.5	5.1	

6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$

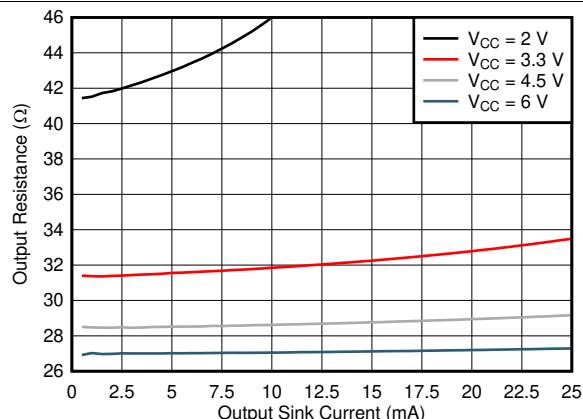


图 1. Output driver resistance in Low state

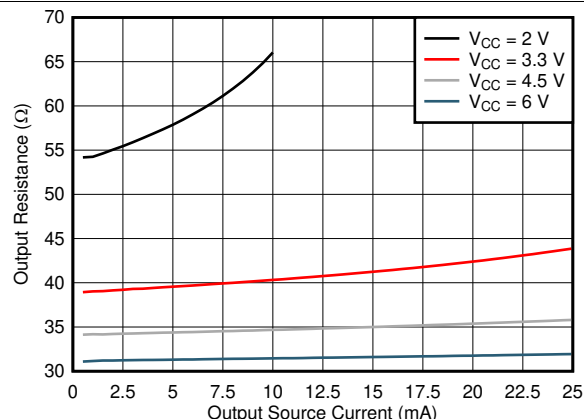


图 2. Output driver resistance in High state

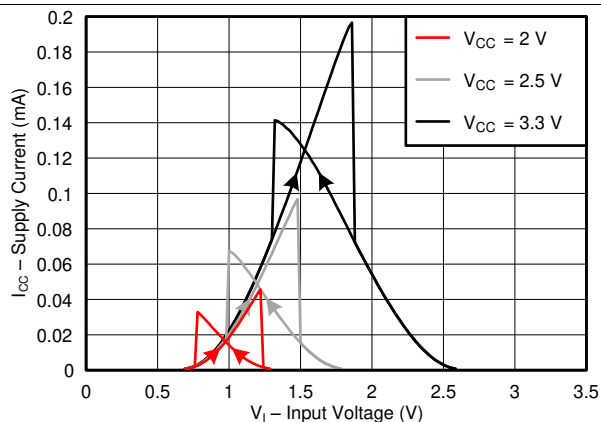


图 3. Typical supply current versus input voltage across common supply values (2 V to 3.3 V)

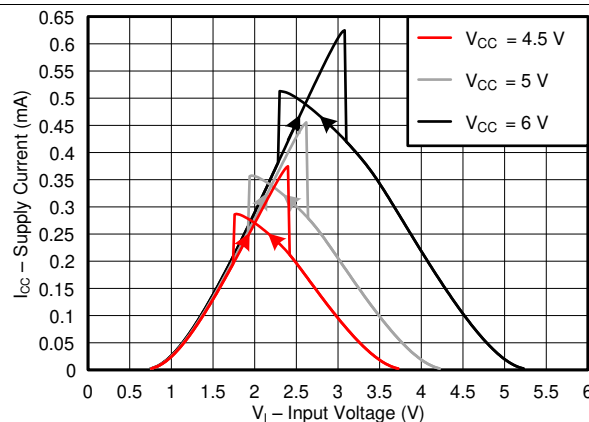
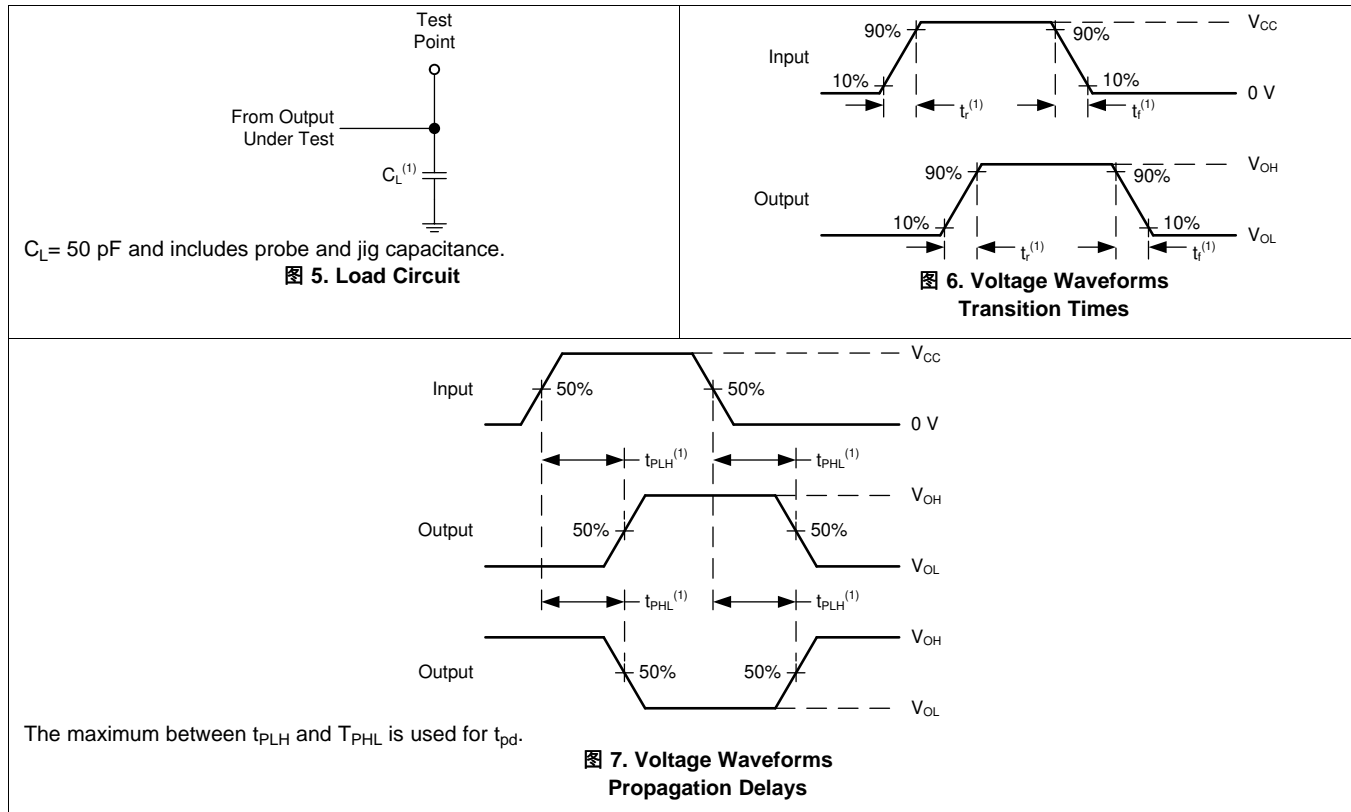


图 4. Typical supply current versus input voltage across common supply values (4.5 V to 6 V)

7 Parameter Measurement Information

- Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 2.5 \text{ ns}$.
- The outputs are measured one at a time, with one input transition per measurement.

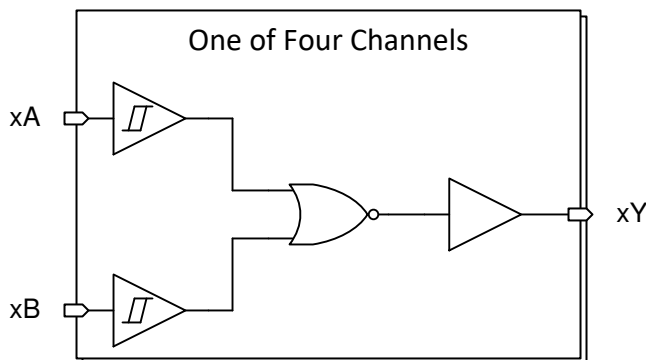


8 Detailed Description

8.1 Overview

This device contains four independent 2-input NOR Gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = A + B$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

8.3.2 CMOS Schmitt-Trigger Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the [Electrical Characteristics](#). The worst case resistance is calculated with the maximum input voltage, given in the [Absolute Maximum Ratings](#), and the maximum input leakage current, given in the [Electrical Characteristics](#), using ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the [Electrical Characteristics](#), which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs slowly will also increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Figure 8](#).

CAUTION

Voltages beyond the values specified in the [Absolute Maximum Ratings](#) table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

Feature Description (接下页)



图 8. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

表 1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	H
H	X	L
X	H	L

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In this application, two 2-input NOR gates are used to create an SR latch as shown in 图 9. The two additional gates can be used for a second SR latch, or the inputs can be grounded and both channels left unused.

The SN74HCS02-Q1 is used to drive the tamper indicator LED and provide one bit of data to the system controller. When the tamper switch outputs HIGH, the output Q becomes HIGH. This output remains HIGH until the system controller addresses the event and sends a HIGH signal to the R input which returns the Q output back to LOW.

The user can add a small RC to the feedback path of the NOR gates to default the output to a certain state, which can create slow transition rates. This fact makes the SN74HCS02-Q1 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

9.2 Typical Application

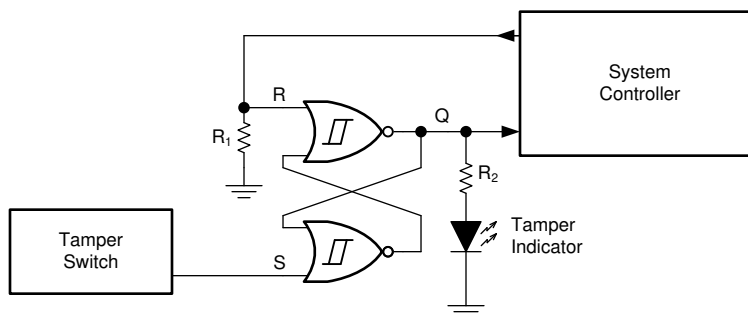


图 9. Typical application block diagram

9.2.1 Design Requirements

- All signals in the system operate at 5 V
- Avoid unstable state by not having HIGH signals on both inputs
- Q output is HIGH when S is HIGH
 - Q output remains High until R is HIGH

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the [Recommended Operating Conditions](#). The supply voltage sets the device's electrical characteristics as described in the [Electrical Characteristics](#).

The supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS02-Q1 plus the maximum supply current, I_{CC} , listed in the [Electrical Characteristics](#). The logic device can only source or sink as much current as it is provided at the supply and ground pins, respectively. Be sure not to exceed the maximum total current through GND or V_{CC} listed in the [Absolute Maximum Ratings](#).

The SN74HCS02-Q1 can drive a load with a total capacitance less than or equal to 50 pF connected to a high-impedance CMOS input while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 70 pF.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and \$C_{pd}\$ Calculation](#).

Typical Application (接下页)

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_J(\text{max})$ listed in the [Absolute Maximum Ratings](#), is an *additional limitation* to prevent damage to the device. Do not violate any values listed in the [Absolute Maximum Ratings](#). These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t(\text{min})}$ to be considered a logic LOW, and $V_{t(\text{max})}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the [Absolute Maximum Ratings](#).

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS02-Q1, as specified in the [Electrical Characteristics](#), and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HCS02-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_T(\text{min})$ in the [Electrical Characteristics](#). This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the [Typical Characteristics](#).

Refer to the [Feature Description](#) for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the [Electrical Characteristics](#). Similarly, the ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the [Electrical Characteristics](#). The plots in and provide a typical relationship between output voltage and current for this device.

Unused outputs can be left floating.

Refer to [Feature Description](#) for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the [Layout](#).
2. Ensure the capacitive load at the output is ≤ 70 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS02-Q1 to the receiving device.
3. Ensure the resistive load at the output is larger than $(V_{CC} / 25 \text{ mA}) \Omega$. This will ensure that the maximum output current from the [Absolute Maximum Ratings](#) is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#)

Typical Application (接下页)

9.2.3 Application Curves

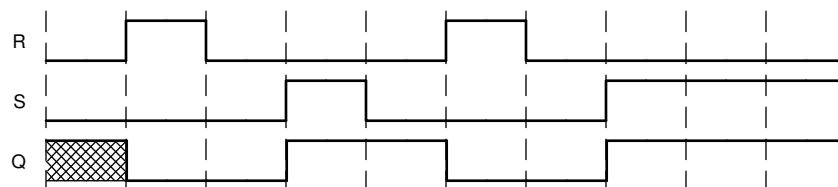


图 10. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [Recommended Operating Conditions](#). Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in [Figure 11](#).

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

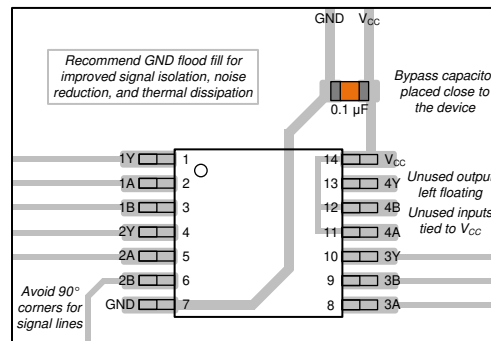


图 11. Example layout for the SN74HCS02-Q1

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

请参阅如下相关文档：

- [《HCMOS 设计注意事项》](#)
- [《CMOS 功耗与 CPD 计算》](#)
- [《使用逻辑器件进行设计》](#)

12.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

12.3 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS02QBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS02Q	Samples
SN74HCS02QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS02Q1	Samples
SN74HCS02QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS02Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74HCS02-Q1 :

- Catalog : [SN74HCS02](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



WQFN - 0.8 mm max height

The drawing illustrates the mechanical specifications of a 15-pin connector. It includes three main views: a top view, a side view, and a detail view of the pin index area.

Top View: Shows the overall footprint of the connector. The total width is 2.6 (2.4) and the total height is 3.1 (2.9). A shaded region indicates the "PIN 1 INDEX AREA". The pin layout is symmetrical about a vertical centerline (SYM). Pin numbers 1 through 15 are labeled. Dimensions include 1.1 (0.9) for the central pin spacing, 2X 0.5 for the central pin width, 8X 0.5 for the side pin spacing, 2X 2 for the side pin width, and 1.6 (1.4) for the pin pitch. A "PIN 1 ID (OPTIONAL)" feature is indicated.

Side View: Shows the profile of the connector. The total height is 0.8 (0.7). The base thickness is 0.05 (0.00). The "SEATING PLANE" is indicated. A detail callout shows a semi-circular feature with a radius of 0.08 (C).

Detail View: Shows the pin index area with dimensions 14X 0.3 (0.2) and 14X 0.5 (0.3). A feature control frame specifies a positional tolerance of 0.1 (M) C A B and a circular runout tolerance of 0.05 (M) C.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

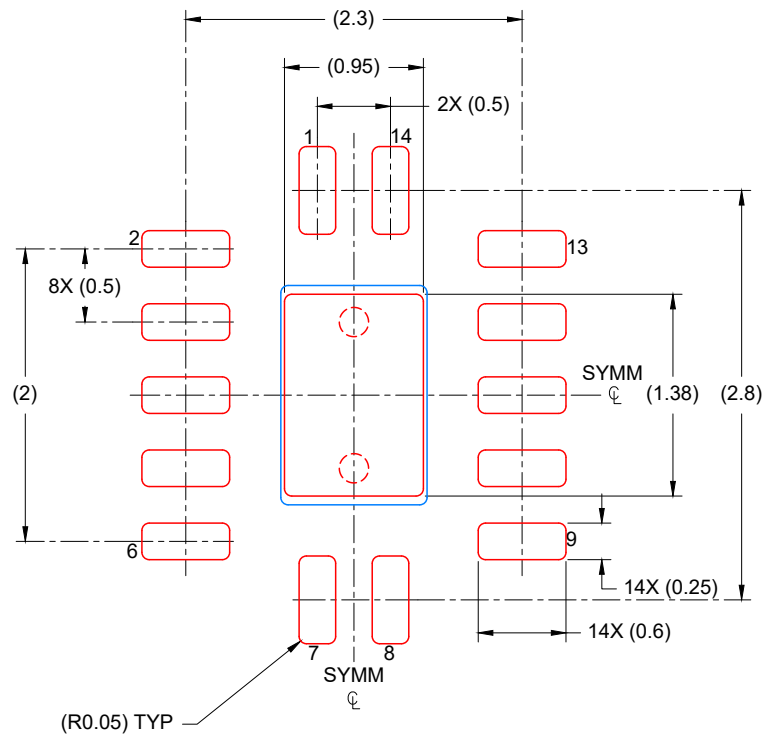
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

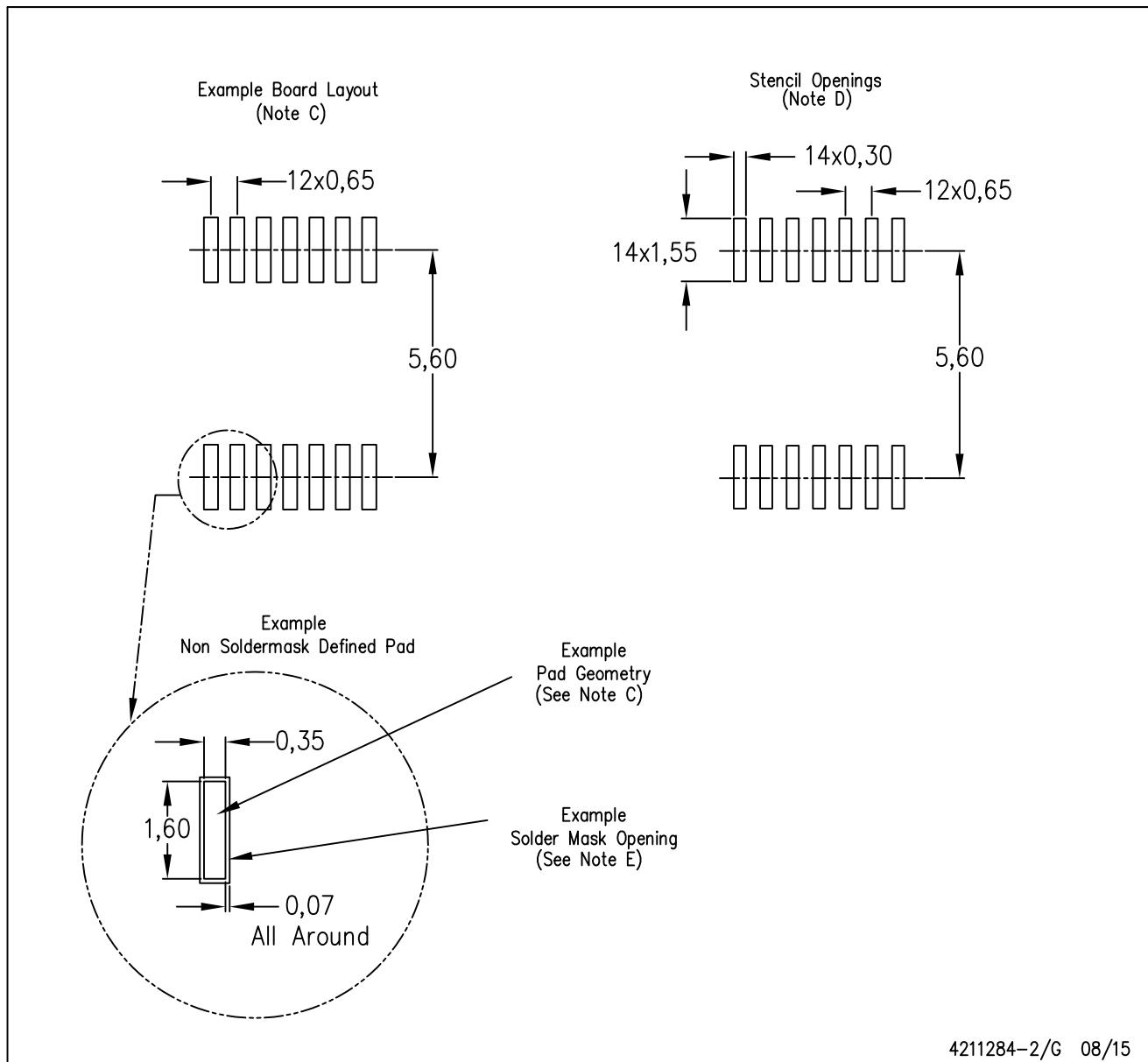
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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