SN74LVC2G66-Q1 汽车类双路双边模拟开关

1 特性

- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 +125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C3B
- 1.65V 至 5.5V V_{CC} 运行
- 输入电压高达 5.5V
- 高开关输出电压比
- 高度线性
- 高速，典型值为 0.5ns（V_{CC} = 3V，C_L = 50pF）
- 轨到轨输入/输出
- 低通态电阻，典型值为 ≠6Ω (V_{CC} = 4.5V)

2 应用

- 无线设备
- 音频和视频信号路由
- 便携式计算
- 可穿戴设备
- 信号门控、斩波、调制或解调（调制解调器）
- 适用于模数和数模转换系统的信号多路复用

3 说明

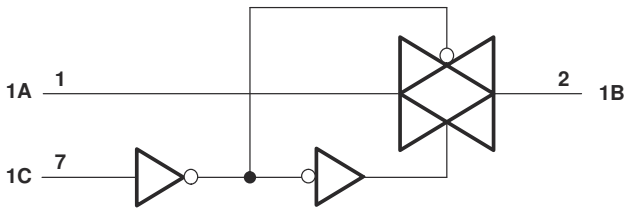
这个双路双向模拟开关的设计适用于 1.65V 至 5.5V V_{CC} 运行环境。SN74LVC2G66-Q1 能够处理模拟和数字信号。这个器件可在两个方向上传输高达 5.5V（峰值）振幅的信号。每个开关部分有其自己的输入使能控制 (C)。应用到 C 上的一个高电平电压开启相关开关部分。

应用包括信号选通、斩波、调制或者解调 (modem)，以及针对模数和数模转换系统的信号复用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
SN74LVC2G66-Q1	VSSOP (8)	2.30mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图、每次转换（正逻辑）

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (July 2012) to Revision B (October 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 向数据表添加了功能安全文本	1
• Added the *Detailed Description* sections	14
• Added the *Application and Implementation* sections	15
• Added the *Power Supply Reccommendations* section	16
• Added the *Layout* sections	17
• Added the *Device and Documentation* sections	18

5 Ordering Information

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 125°C	VSSOP – DCU	Reel of 3000	SN74LVC2G66QDCURQ1	CAY_

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) DCU: The actual top-side marking has one additional character that designates the assembly/test site.

6 Pin Configuration and Functions

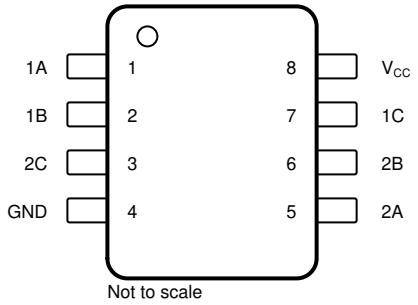


图 6-1. DCU Package 8-Pin VSSOP Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NAME		
1A	1	I/O	Bidirectional signal to be switched
1B	2	I/O	Bidirectional signal to be switched
2C	3	I	Controls the switch (L = OFF, H = ON)
GND	4	—	Ground pin
2A	5	I/O	Bidirectional signal to be switched
2B	6	I/O	Bidirectional signal to be switched
1C	7	I	Controls the switch (L = OFF, H = ON)
V_{CC}	8	—	Power Pin

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)		– 0.5	6.5	V
V_I	Input voltage range(2) (3)		– 0.5	6.5	V
V_O	Switch I/O voltage range(2) (3) (4)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_I < 0		– 50	mA
$I_{I/OK}$	I/O port diode current	$V_{I/O}$ < 0 or $V_{I/O}$ > V_{CC}		– 50	mA
I_T	On-state switch current	$V_{I/O}$ = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Exceeding the input and output negative-voltage ratings is permitted when in observance of the input and output clamp-current ratings.
(4) This limit on this value is limited 5.5 V maximum.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	2000	V
		Charged-device model (CDM), per AEC Q100-011	750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Thermal Information

THERMAL METRIC(1)		SN74LVC2G66-Q1 DCU (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	77	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	83.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.7	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.4 Recommended Operating Conditions

See (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
$V_{I/O}$	I/O port voltage		0	V_{CC}	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	V_{CC} × 0.65		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		

7.4 Recommended Operating Conditions (continued)

See (1)

			MIN	MAX	UNIT
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V		V_{CC} × 0.35	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Control input voltage		0	5.5	V
$\Delta t/\Delta v$	Input transition rise/fall time	V_{CC} = 1.65 V to 1.95 V		20	ns/V
		V_{CC} = 2.3 V to 2.7 V		20	
		V_{CC} = 3 V to 3.6 V		10	
		V_{CC} = 4.5 V to 5.5 V		10	
T_A	Operating free-air temperature		–40	125	°C

(1) Hold all unused inputs of the device at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
r_{on}	On-state switch resistance	V_I = V_{CC} or GND, V_C = V_{IH} (see 图 8-1 and 图 7-1)	I_S = 4 mA	1.65 V		12.5	35	Ω
			I_S = 8 mA	2.3 V		9	30	
			I_S = 24 mA	3 V		7.5	20	
			I_S = 32 mA	4.5 V		6	15	
$r_{on(p)}$	Peak on-state resistance	V_I = V_{CC} to GND, V_C = V_{IH} (see 图 8-1 and 图 7-1)	I_S = 4 mA	1.65 V		85	120(1)	Ω
			I_S = 8 mA	2.3 V		22	30(1)	
			I_S = 24 mA	3 V		12	25	
			I_S = 32 mA	4.5 V		7.5	20	
Δr_{on}	Difference of on-state resistance between switches	V_I = V_{CC} to GND, V_C = V_{IH} (see 图 8-1 and 图 7-1)	I_S = 4 mA	1.65 V			10	Ω
			I_S = 8 mA	2.3 V			8	
			I_S = 24 mA	3 V			6	
			I_S = 32 mA	4.5 V			5	
$I_{S(off)}$	Off-state switch leakage current	V_I = V_{CC} and V_O = GND or V_I = GND and V_O = V_{CC}, V_C = V_{IL} (see 图 8-2)		5.5 V			±2	μA
							±0.1(1)	
$I_{S(on)}$	On-state switch leakage current	V_I = V_{CC} or GND, V_C = V_{IH}, V_O = Open (see 图 8-3)		5.5 V			±2	μA
							±0.1(1)	
I_I	Control input current	V_C = V_{CC} or GND		5.5 V			±1	μA
							±0.1(1)	
I_{CC}	Supply current	V_C = V_{CC} or GND		5.5 V			15	μA
							1(1)	
ΔI_{CC}	Supply-current change	V_C = V_{CC} – 0.6 V		5.5 V			500	μA
C_{ic}	Control input capacitance			5 V		3.5		pF
$C_{io(off)}$	Switch input/output capacitance			5 V		6		pF
$C_{io(on)}$	Switch input/output capacitance			5 V		14		pF

(1) T_A = 25°C

7.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 图 8-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{en} (1)	C	A or B	2.3	12	1.6	7.5	1.5	6.4	1.3	5.9	ns
t_{dis} (2)	C	A or B	2.2	12.5	1.2	7.9	2	9.2	1.1	8.3	ns

(1) t_{PZL} and t_{PZH} are the same as t_{en}.
(2) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

7.7 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (switch on)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = sine wave (see 图 8-5)	1.65 V	35	MHz
				2.3 V	120	
				3 V	175	
				4.5 V	195	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = sine wave (see 图 8-5)	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk(1) (between switches)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see 图 8-6)	1.65 V	– 58	dB
				2.3 V	– 58	
				3 V	– 58	
				4.5 V	– 58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see 图 8-6)	1.65 V	– 42	
				2.3 V	– 42	
				3 V	– 42	
				4.5 V	– 42	
Crosstalk (control input to signal output)	C	A or B	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (square wave) (see 图 8-7)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feedthrough attenuation (switch off)	A or B	B or A	C_L = 50 pF, R_L = 600 Ω, f_{in} = 1 MHz (sine wave) (see 图 8-8)	1.65 V	– 58	dB
				2.3 V	– 58	
				3 V	– 58	
				4.5 V	– 58	
			C_L = 5 pF, R_L = 50 Ω, f_{in} = 1 MHz (sine wave) (see 图 8-8)	1.65 V	– 42	
				2.3 V	– 42	
				3 V	– 42	
				4.5 V	– 42	

7.7 Analog Switch Characteristics (continued)

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Sine-wave distortion	A or B	B or A	C_L = 50 pF, R_L = 10 kΩ, f_{in} = 1 kHz (sine wave) (see 图 8-9)	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	
			C_L = 50 pF, R_L = 10 kΩ, f_{in} = 10 kHz (sine wave) (see 图 8-9)	1.65 V	0.15%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

(1) Adjust f_{in} voltage to obtain 0 dBm at input.

7.8 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V	V_{CC} = 2.5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	UNIT
			TYP	TYP	TYP	TYP	
C_{pd}	Power-dissipation capacitance	f = 10 MHz	8	9	9.5	11	pF

7.9 Typical Characteristics

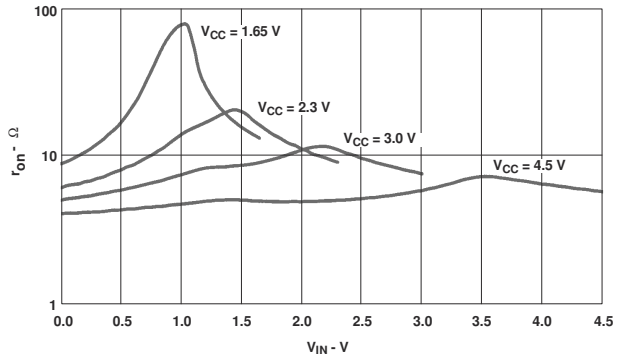


图 7-1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I = 0 to V_{CC}

8 Parameter Measurement Information

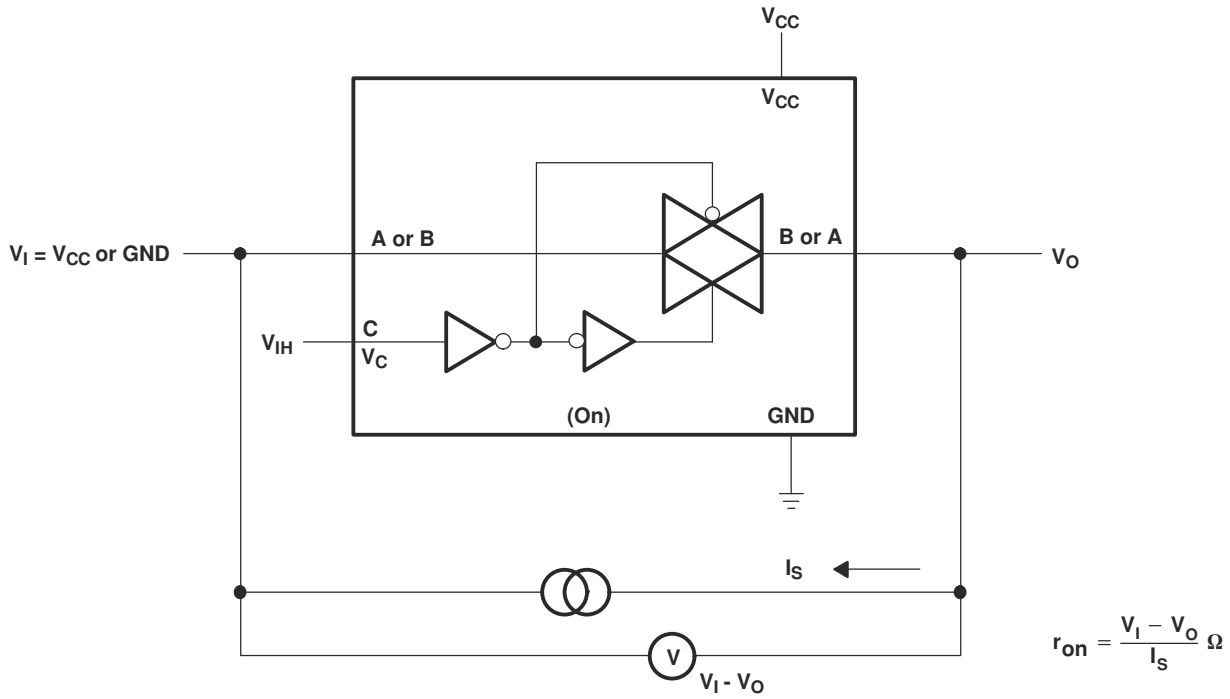


图 8-1. On-State Resistance Test Circuit

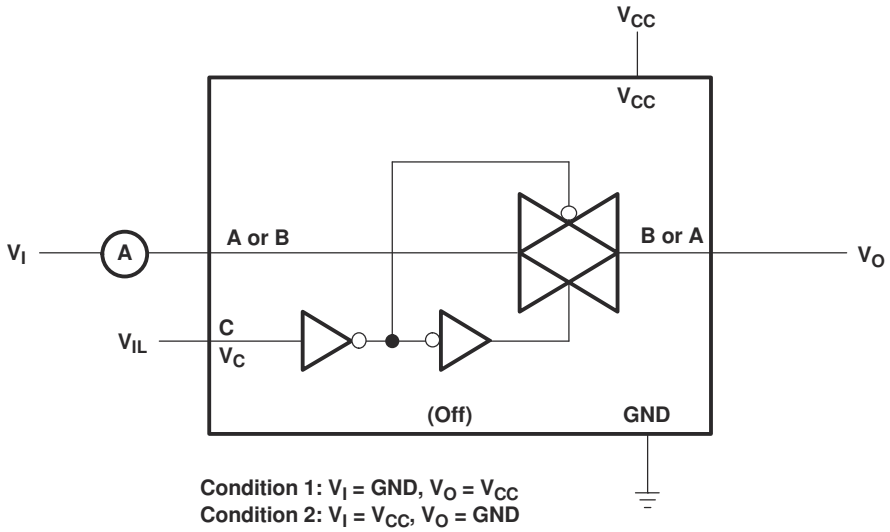


图 8-2. Off-State Switch Leakage-Current Test Circuit

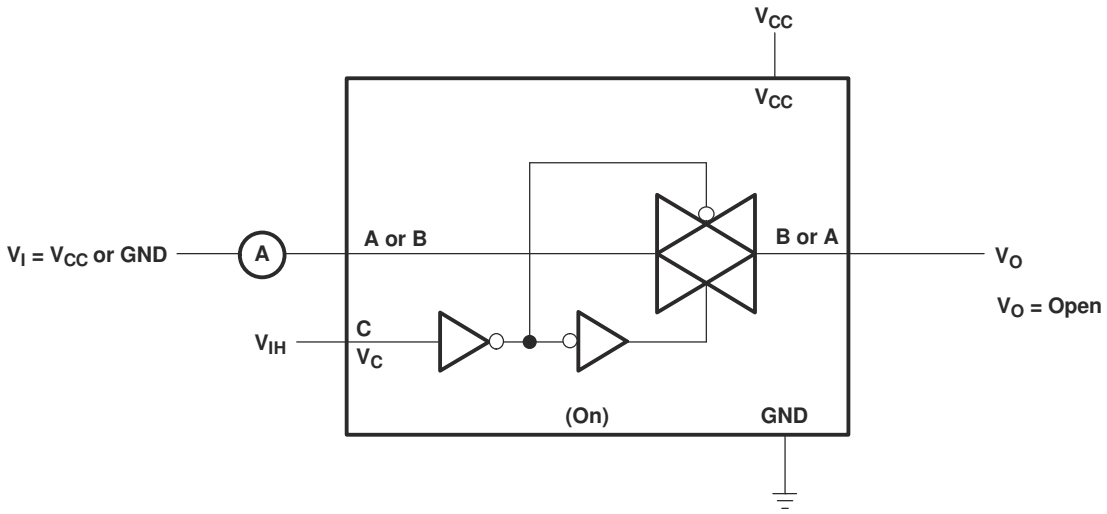
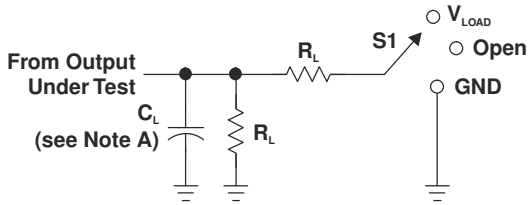


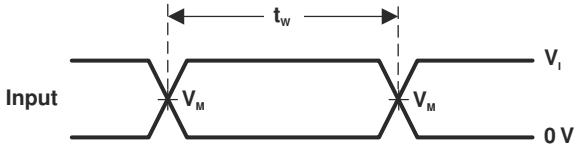
图 8-3. On-State Leakage-Current Test Circuit



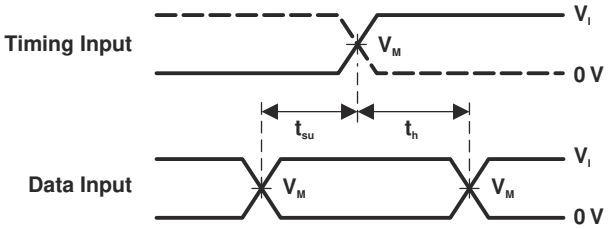
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

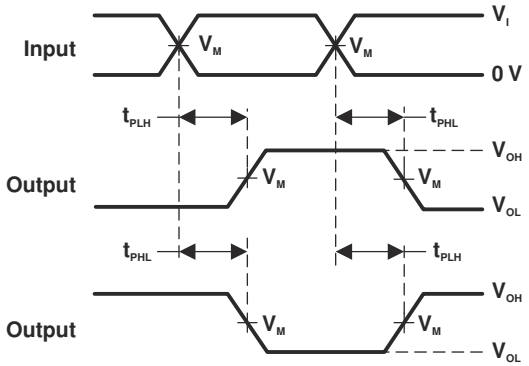
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V



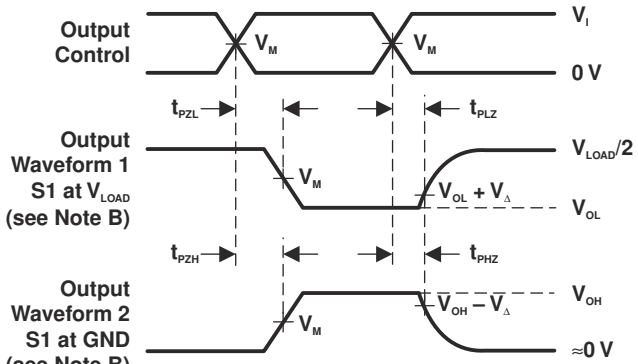
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators have the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 8-4. Load Circuit and Voltage Waveforms

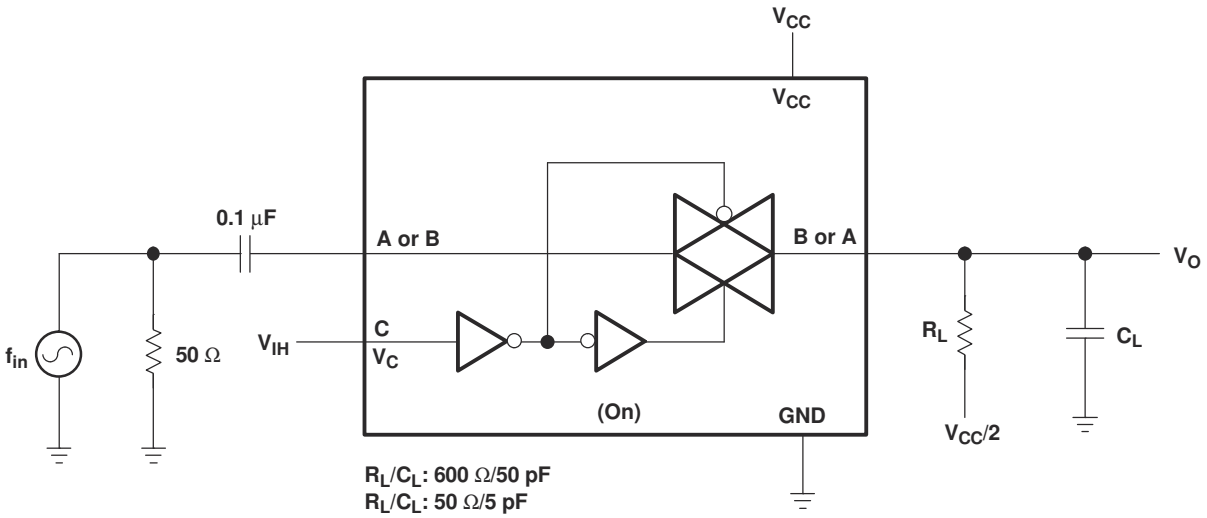


图 8-5. Frequency Response (Switch On)

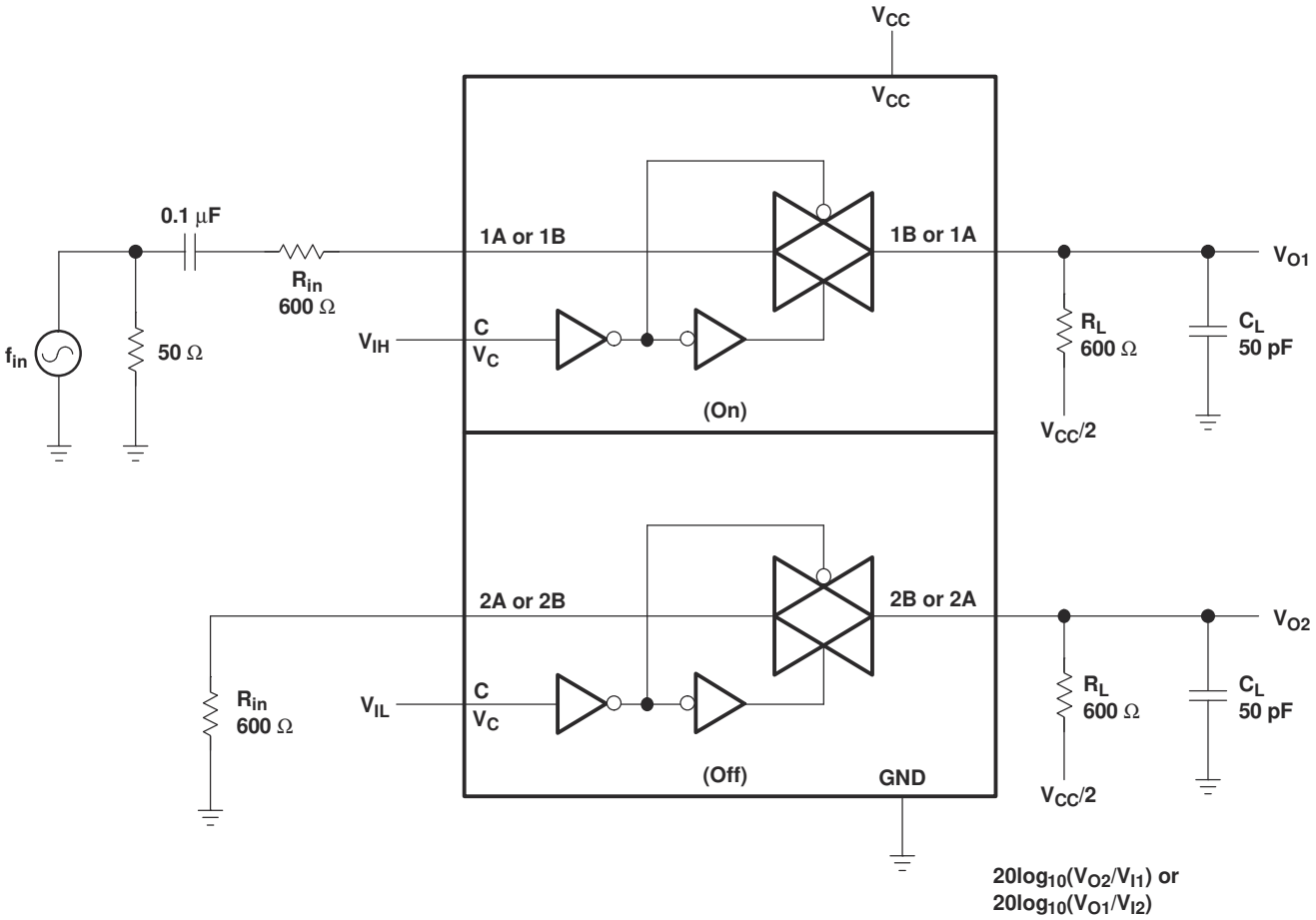


图 8-6. Crosstalk (Between Switches)

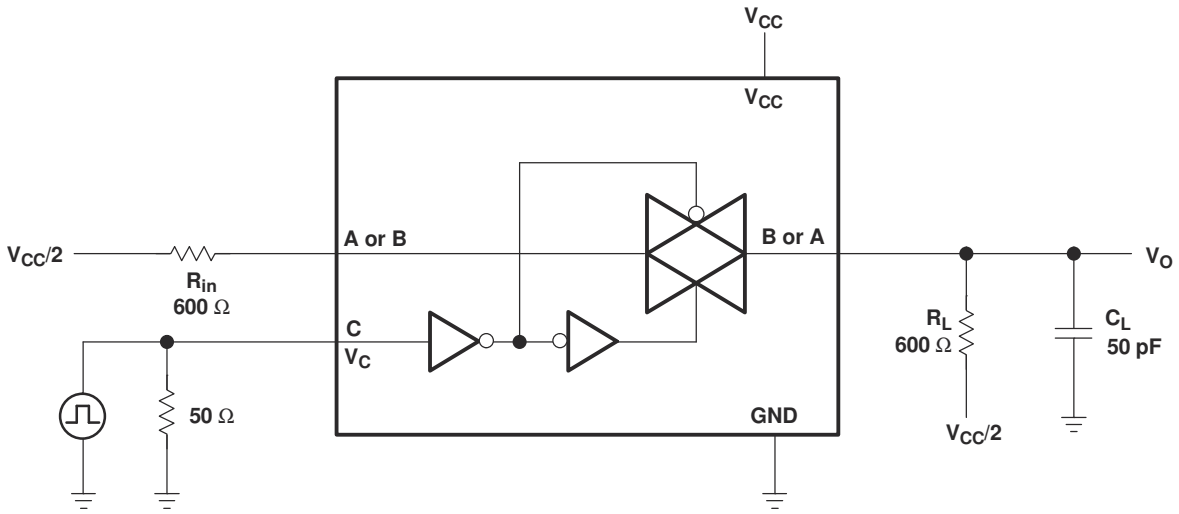


图 8-7. Crosstalk (Control Input, Switch Output)

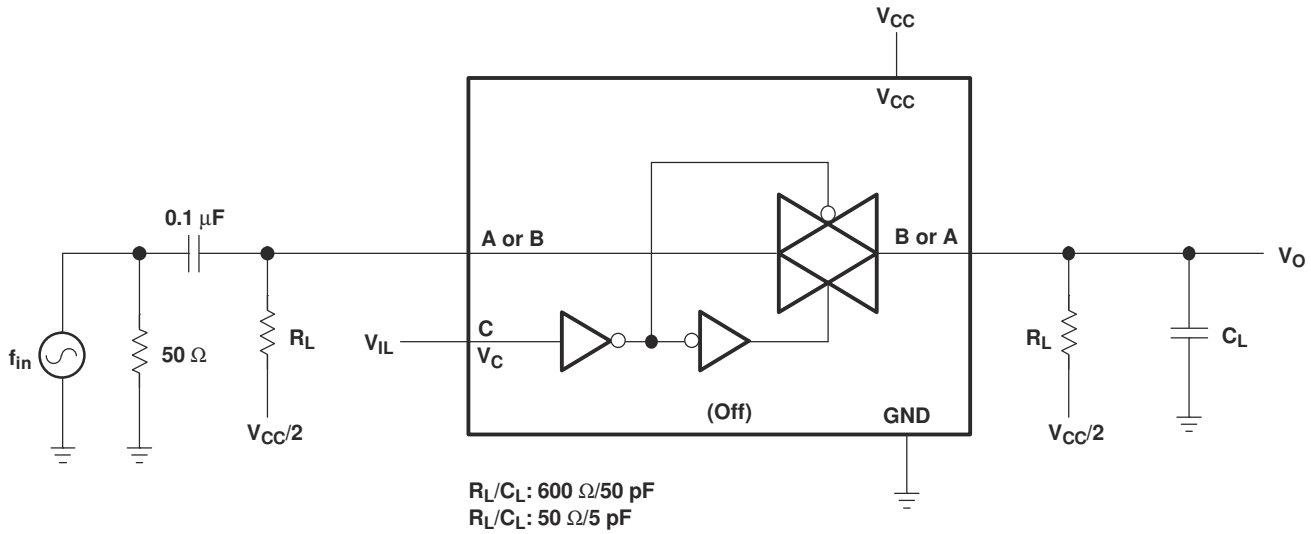


图 8-8. Feedthrough (Switch Off)

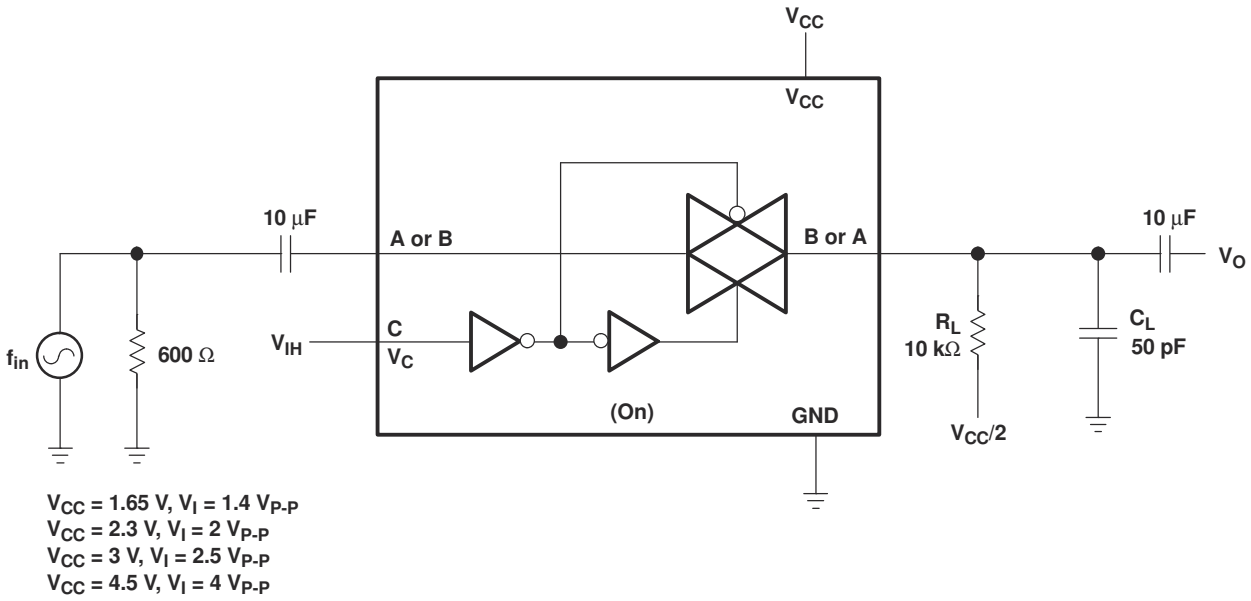


图 8-9. Sine-Wave Distortion

9 Detailed Description

9.1 Overview

This dual bilateral analog switch is designed for 1.65-V to 5.5-V V_{CC} operation. Robust LVC family technology allows this device to accept input voltages without connecting power to V_{CC}.

The SN74LVC2G66-Q1 device permits signals with amplitudes of up to 5.5 V (peak) to be transmitted in either direction. A high-level voltage applied to the control pin C enables the respective switch to begin propagating signals across the device. A low-level voltage disables this transmission. Each device incorporates two switches with independent control and operation.

9.2 Functional Block Diagram

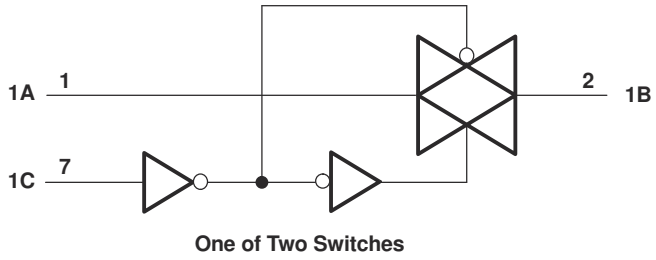


图 9-1. Logic Diagram, Each Switch (Positive Logic)

9.3 Feature Description

Each switch section has its own enable-input control (C). A high-level voltage applied to C turns on the associated switch section. When C is this Signals can pass through A to B or B to A. Low ON-resistance of 6 Ω at 4.5-V V_{CC} is ideal for analog signal conditioning systems. The control signals can accept voltages up to 5.5 V without V_{CC} connected in the system. Combination of lower t_{pd} of 0.8 ns at 3.3 V and low enable and disable time make this part suitable for high-speed signal switching applications.

9.4 Device Functional Modes

表 9-1 shows the functional modes of the SN74LVC2G66-Q1.

表 9-1. Function Table (Each Section)

CONTROL INPUT (C)	SWITCH
L	Off
H	On

10 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

The SN74LVC2G66-Q1 can be used in any situation where an Dual SPST switch would be used and a solid-state, voltage controlled version is preferred.

10.2 Typical Application

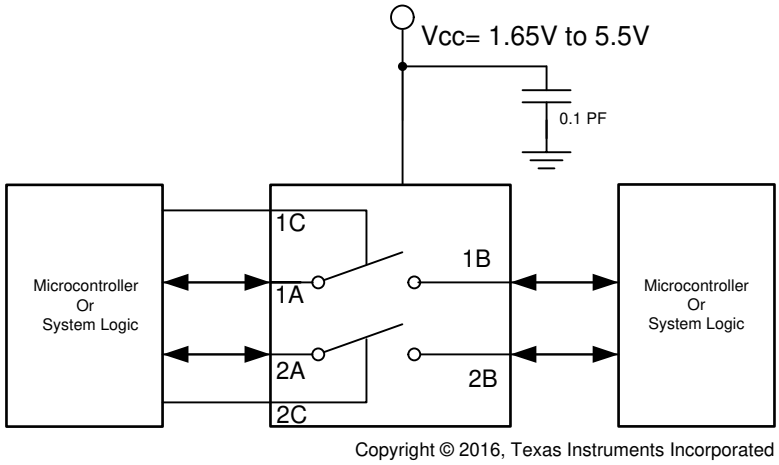


图 10-1. Typical Application Schematic

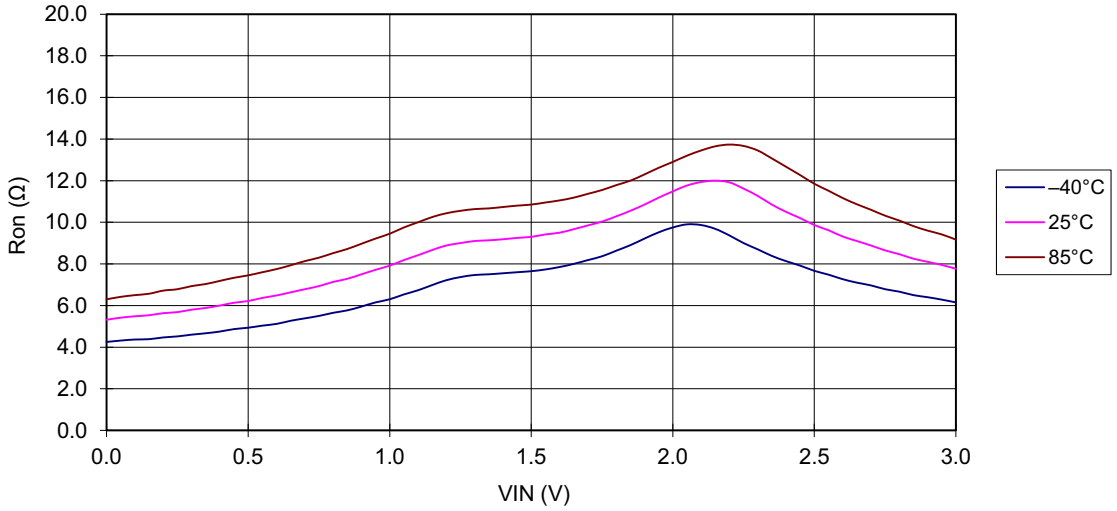
10.2.1 Design Requirements

The SN74LVC2G66-Q1 allows on/off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and V_{CC} for optimal operation.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see $\Delta t/\Delta v$ in the *Recommended Operating Conditions* table.
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs and outputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed ±50 mA.
3. Frequency Selection Criterion:
   - Maximum frequency tested is 150 MHz.
   - Added trace resistance or capacitance can reduce maximum frequency capability; use layout practices as directed in the *Layout* section.

10.2.3 Application Curve



Pin: A – B, V_{CC} = 3 V, I_S = 24 mA

图 10-2. r_{on} vs V_I

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the VCC pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

12 Layout

12.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self – inductance of the trace — resulting in the reflection.

Note

Not all PCB traces can be straight, and so they will have to turn corners. 图 12-1 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

12.2 Layout Example

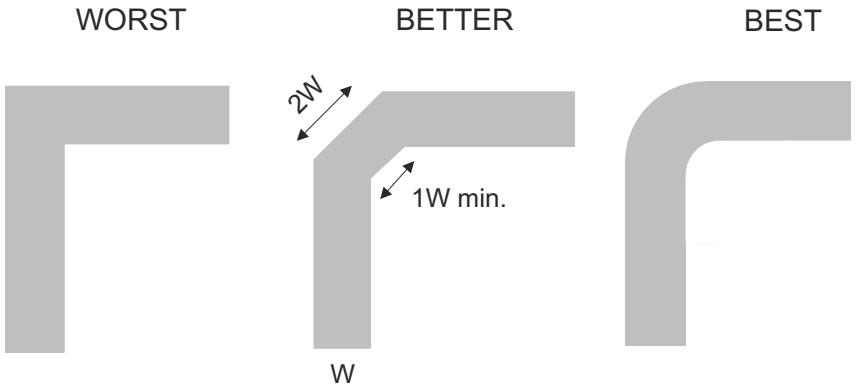


图 12-1. Trace Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, SN74LVC2G66-Q1 Functional Safety, FIT Rate, Failure Mode Distribution and Pin FMA

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G66QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CAYR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC2G66-Q1 :

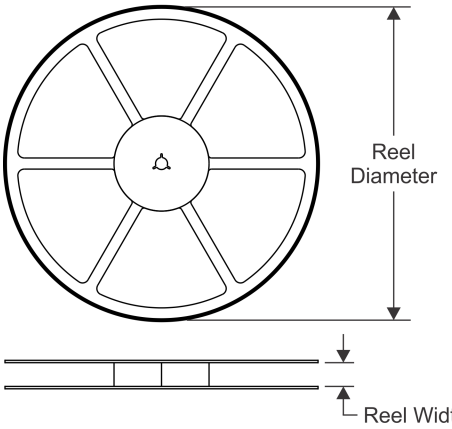
- Catalog : SN74LVC2G66

NOTE: Qualified Version Definitions:

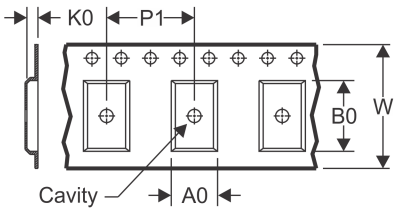
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

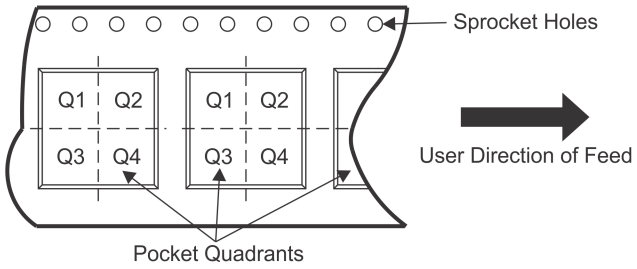


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

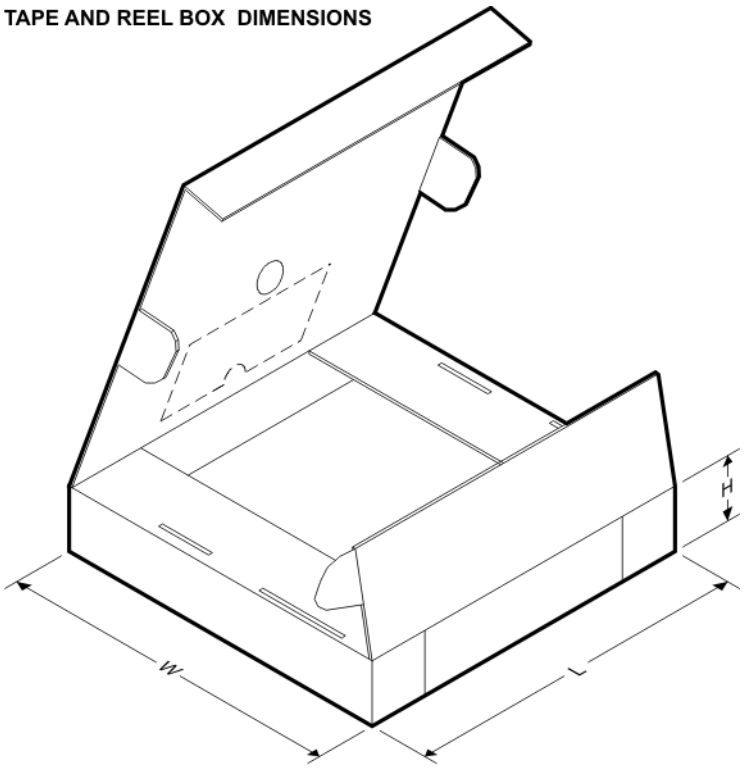
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G66QDCURQ1	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

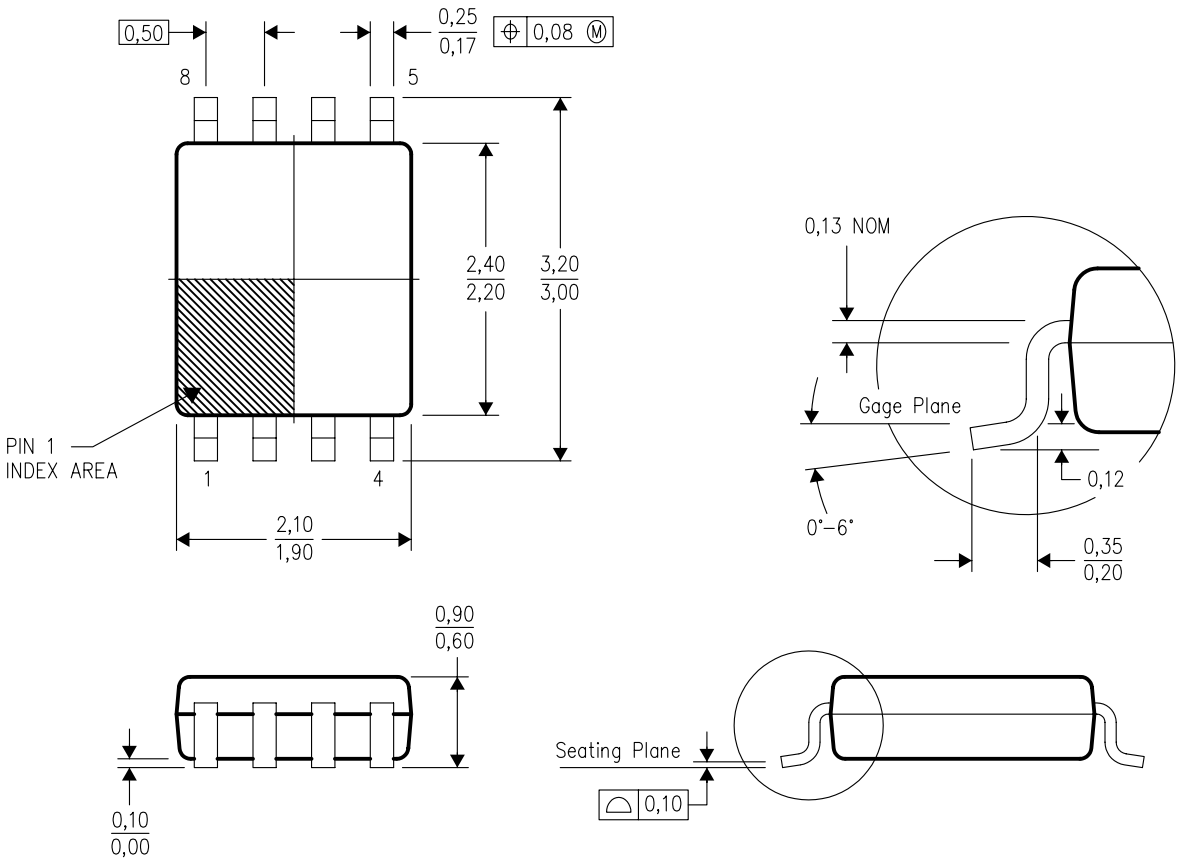
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G66QDCURQ1	VSSOP	DCU	8	3000	202.0	201.0	28.0

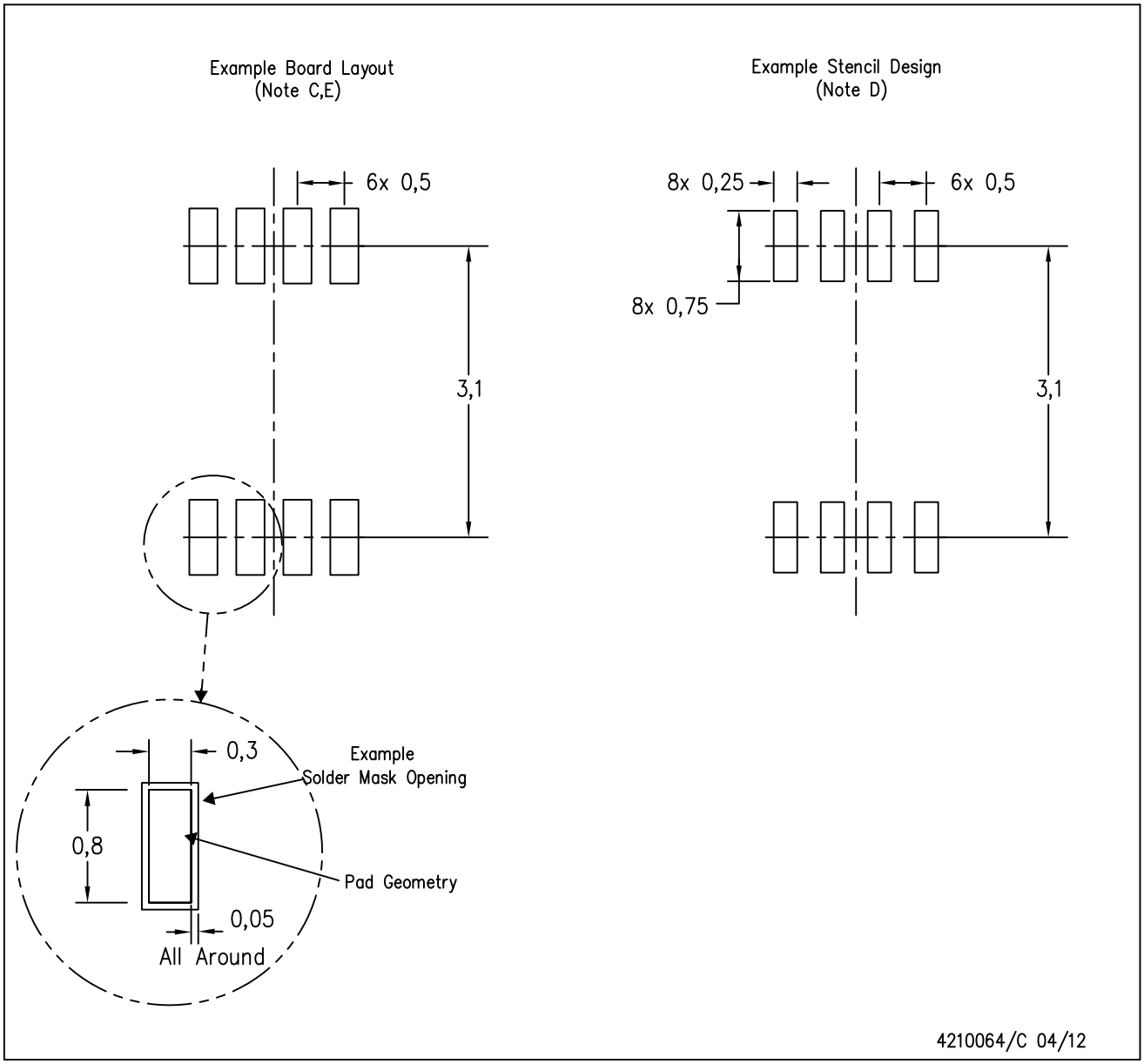
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



4200503/F 07/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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