

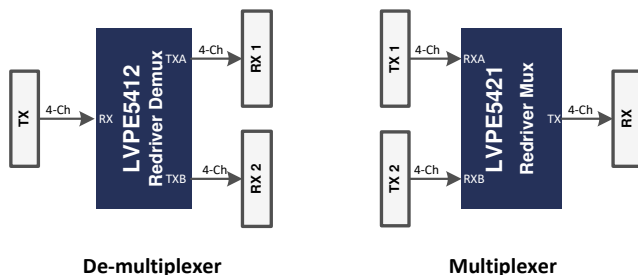
SN75LVPE5412 具有 1:2 多路信号分离器的 PCIe® 5.0 32Gbps 4 通道线性转接驱动器

1 特性

- 具有集成式 1:2 多路信号分离器的四通道 PCIe 5.0 线性转接驱动器或中继器
- 此线性转接驱动器与协议无关，可兼容 PCIe、UPI、CCIX、NVLink、DisplayPort、SAS、SATA 和 XFI
- 单个 3.3V 电源，可使用 PCIe 电源轨
- 4 通道运行时，有功功率低至 720mW
- 无需散热器
- 频率为 16GHz 时，支持高达 24dB 的均衡功能
- 出色的 RX/TX 差分 RL (8-16GHz 时，为 -10dB)
- 55fs RMS 的低附加随机抖动 (带 PRBS 数据)
- 90ps 低延迟
- 自动接收器检测和无缝支持 PCIe 链路训练
- 通过引脚控制或 SMBus/I²C 进行器件配置。
- 通过引脚选择多路信号分离器
- 内部稳压器具有抗电源噪声能力
- 高速量产测试可确保制造可靠性
- 通过一个或多个器件支持 x4、x8 和 x16 总线宽度
- 可提供配套多路复用器产品 [SN75LVPE5421](#)
- 0°C 至 85°C 温度范围
- 3.5mm × 9mm 42 引脚 0.5mm 间距 WQFN 封装

2 应用

- 台式计算机和主板
- 显示面板、游戏机
- 机架式服务器、微服务器和塔式服务器
- 高性能计算、硬件加速器
- 数据存储、网络附加存储
- 存储区域网络 (SAN) 和主机总线适配器 (HBA) 卡
- 网络接口卡 (NIC)



3 说明

SN75LVPE5412 是一款具有集成式多路信号分离器的四通道线性转接驱动器。这款低功耗高性能线性转接驱动器专为支持 PCIe 5.0 和其他速率高达 32Gbps 的接口而设计。

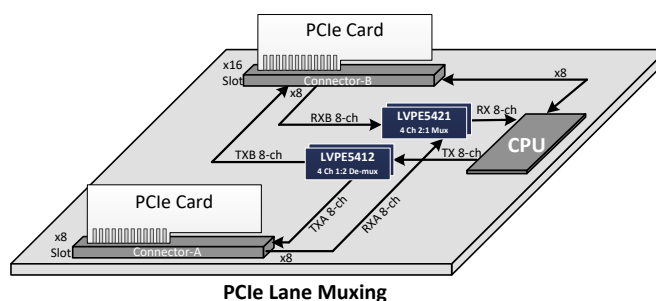
SN75LVPE5412 接收器部署了连续时间线性均衡器 (CTLE)，可提供高频增强。均衡器可以打开由于 PCB 布线或电缆等互连介质引起的码间串扰 (ISI) 而完全关闭的输入眼图。在 PCIe 链路训练期间，线性转接驱动器与根复合体 (RC) 和端点 (EP) 之间的无源通道作为一个整体接受训练，以达到理想的发送和接收均衡设置，从而实现出色的电气链路。该器件具有低通道间串扰、低附加抖动和极低的回波损耗，因此在链路中几乎可作为无源元件。这款器件具有内部线性稳压器，对板上电源噪声具有高抗扰度，从而为高速数据路径提供纯净电源。

SN75LVPE5412 在量产期间实施了高速测试，从而确保可靠的高产量制造。此器件还具有低交流和直流增益变化，可在各种平台部署中提供一致的均衡功能。

器件信息(1)

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|--------------|-----------|-----------------|
| SN75LVPE5412 | WQFN (42) | 3.5 mm × 9.0 mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



应用用例



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4 Revision History

| DATE | REVISION | NOTES |
|---------------|----------|-----------------|
| December 2021 | * | Initial Release |

5 Pin Configuration and Functions

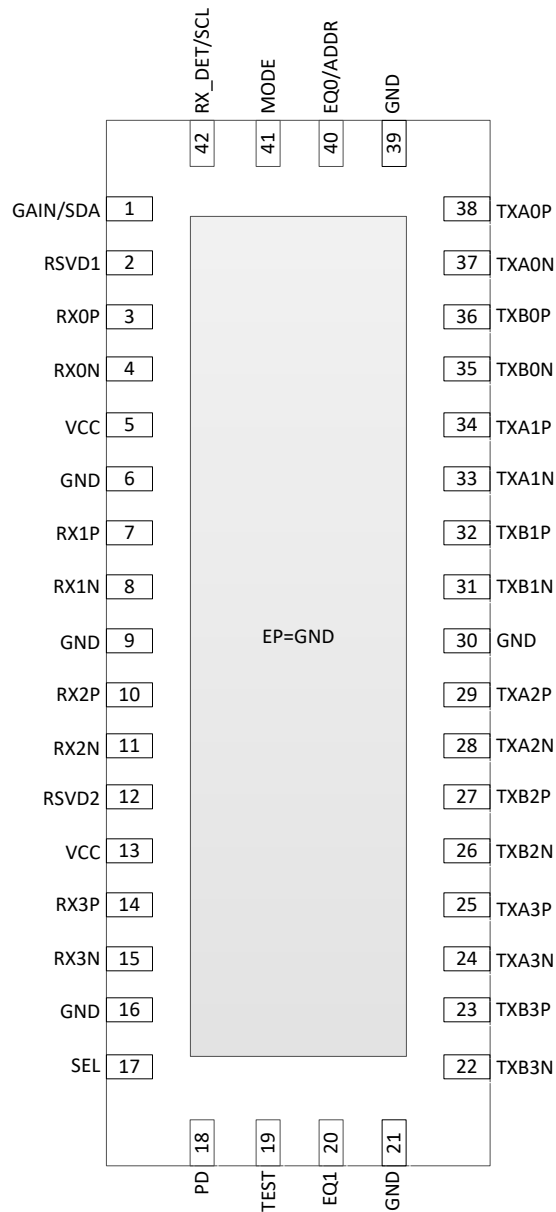


图 5-1. RUA Package 42-Pin WQFN Top View

表 5-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------------|--------------------------|---------------------|---|
| NAME | NO. | | |
| MODE | 41 | I, 5-level | Sets device control configuration modes. The 5-level IO pin is defined in 表 7-1. The pin can be exercised at device power up or in normal operation mode. L0: Pin Mode – device control configuration is done solely by strap pins. L1 or L2: SMBus/I²C Mode – device control configuration is done by an external controller with SMBus/I ² C primary. This pin along with ADDR pin sets devices secondary address. L3 and L4 (Float): RESERVED – TI internal test modes. |
| EQ0 /ADDR | 40 | I, 5-level | In Pin Mode: The EQ0 and EQ1 pins sets receiver linear equalization CTLE (AC gain) for all channels according to 表 7-2. These pins are sampled at device power-up only. |
| EQ1 | 20 | I, 5-level | In SMBus/I²C Mode: The ADDR pin in conjunction with MODE pin sets SMBus / I ² C secondary address according to 表 7-5. The pin is sampled at device power-up only. |
| GAIN /SDA | 1 | I, 5-level / IO | In Pin Mode: Flat gain (broadband gain – DC and AC) from the input to the output of the device for all channels. Note: the device also provides AC (high frequency) gain in the form of equalization controlled by EQ pins or SMBus/I ² C registers. The pin is sampled at device power-up only. In SMBus/I²C Mode: 3.3 V SMBus/I ² C data. External pullup resistor such as 4.7 kΩ required for operation. |
| GND | EP, 6, 9, 16, 21, 30, 39 | P | Ground reference for the device. EP: the Exposed Pad at the bottom of the QFN package. It is used as the GND return for the device. The EP should be connected to one or more ground planes through the low resistance path. A via array provides a low impedance path to GND. The EP also improves thermal dissipation. |
| PD | 18 | I, 3.3-V LVCMOS | 2-level logic controlling the operating state of the redriver. Active in both Pin Mode and SMBus/I²C Mode . The pin is used part of PCIe RX_DET state machine as outlined in 表 7-4. High: power down for all channels Low: power up, normal operation for all channels |
| RSVD1, 2 | 2, 12 | — | Reserved pins – for best signal integrity performance connect the pins to GND. Alternate option would be 0 Ω resistors from pins to GND. |
| RX_DET /SCL | 42 | I, 5-level / IO | In Pin Mode: Sets receiver detect state machine options according to 表 7-4. The pin is sampled at device power-up only. In SMBus/I²C Mode: 3.3 V SMBus/I ² C clock. External pullup resistor such as 4.7 kΩ required for operation. |
| RX0N | 4 | I | Inverting differential RX inputs. Channel 0. |
| RX0P | 3 | I | Noninverting differential RX inputs. Channel 0. |
| RX1N | 8 | I | Inverting differential RX inputs. Channel 1. |
| RX1P | 7 | I | Noninverting differential RX inputs. Channel 0. |
| RX2N | 11 | I | Inverting differential RX inputs. Channel 2. |
| RX2P | 10 | I | Noninverting differential RX inputs. Channel 2. |
| RX3N | 15 | I | Inverting differential RX inputs. Channel 3. |
| RX3P | 14 | I | Noninverting differential RX inputs. Channel 3. |
| SEL | 17 | I, 3.3 V LVCMOS | Selects the mux path. Active in both Pin Mode and SMBus/I²C Mode . The pin has a weak internal pull-down resistor. Note: the SEL pin must be exercised in system implementations for mux selection between Port A vs Port B. The pin is used for PCIe RX_DET state machine as outlined in 表 7-4. L: Port A selected. H: Port B selected. |
| TXA0N | 37 | O | Inverting differential TX output – Port A, Channel 0. |
| TXA0P | 38 | O | Non-inverting differential TX output – Port A, Channel 0. |

表 5-1. Pin Functions (continued)

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|-------|-------|---------------------|--|
| NAME | NO. | | |
| TXA1N | 33 | O | Inverting differential TX output - Port A, Channel 1. |
| TXA1P | 34 | O | Non-inverting differential TX output - Port A, Channel 1. |
| TXA2N | 28 | O | Inverting differential TX output - Port A, Channel 2. |
| TXA2P | 29 | O | Non-inverting differential TX output - Port A, Channel 2. |
| TXA3N | 24 | O | Inverting differential TX output - Port A, Channel 3. |
| TXA3P | 25 | O | Non-inverting differential TX output - Port A, Channel 3. |
| TXB0N | 35 | O | Inverting differential TX output - Port B, Channel 0. |
| TXB0P | 36 | O | Non-inverting differential TX output - Port B, Channel 0. |
| TXB1N | 31 | O | Inverting differential TX output - Port B, Channel 1. |
| TXB1P | 32 | O | Non-inverting differential TX output - Port B, Channel 1. |
| TXB2N | 26 | O | Inverting differential TX output - Port B, Channel 2. |
| TXB2P | 27 | O | Non-inverting differential TX output - Port B, Channel 2. |
| TXB3N | 22 | O | Inverting differential TX output - Port B, Channel 3. |
| TXB3P | 23 | O | Non-inverting differential TX output - Port B, Channel 3. |
| TEST | 19 | O | TI internal test pin. Keep no connect. |
| VCC | 5, 13 | P | Power supply, VCC = 3.3 V ± 10%. The VCC pins on this device should be connected through a low-resistance path to the board VCC plane. |

(1) I = input, O = output, P = power, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------------|---|-------|------|------|
| VCC_ABSMAX | Supply Voltage (VCC) | - 0.5 | 4.0 | V |
| VIO_CMOS_ABSMAX | 3.3 V LVCMOS and Open Drain I/O voltage | - 0.5 | 4.0 | V |
| VIO_5LVL_ABSMAX | 5-level Input I/O voltage | - 0.5 | 2.75 | V |
| VIO_HS-RX_ABSMAX | High-speed I/O voltage (RXnP, RXnN) | - 0.5 | 3.2 | V |
| VIO_HS-TX_ABSMAX | High-speed I/O voltage (TXnP, TXnN) | - 0.5 | 2.75 | V |
| T _{J,ABS} MAX | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature range | - 65 | 150 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2 kV may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|-----------------------|---|---|-------|-----|------|------|
| VCC | Supply voltage, VCC to GND | DC plus AC power should not exceed these limits | 3.0 | 3.3 | 3.6 | V |
| N _{VCC} | Supply noise tolerance | DC to <50 Hz, sinusoidal ¹ | | | 250 | mVpp |
| | | 50 Hz to 500 kHz, sinusoidal ¹ | | | 100 | mVpp |
| | | 500 kHz to 2.5 MHz, sinusoidal ¹ | | | 33 | mVpp |
| | | Supply noise, >2.5 MHz, sinusoidal ¹ | | | 10 | mVpp |
| T _{RampVCC} | VCC supply ramp time | From 0 V to 3.0 V | 0.150 | | 100 | ms |
| T _J | Operating junction temperature | | 0 | | 115 | °C |
| T _A | Operating ambient temperature | | 0 | | 85 | °C |
| PW _{LVCMOS} | Minimum pulse width required for the device to detect a valid signal on LVCMOS inputs | PD and SEL | 200 | | | μs |
| VCC _{SMBUS} | SMBus/I ² C SDA and SCL Open Drain Termination Voltage | Supply voltage for open drain pull-up resistor | | | 3.6 | V |
| F _{SMBus} | SMBus/I ² C clock (SCL) frequency in SMBus secondary mode | | 10 | | 400 | kHz |
| VID _{LAUNCH} | Source differential launch amplitude | | 800 | | 1200 | mVpp |
| DR | Data rate | | 1 | | 32 | Gbps |

6.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN75LVPE54 12 | UNIT |
|-------------------------------|--|------------------|------|
| | | RUA, 42 Pins | |
| $R_{\theta JA}$ -High K | Junction-to-ambient thermal resistance | 26.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 14.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 8.7 | °C/W |
| ψ_{JT} | Junction-to-top characterization parameter | 1.6 | °C/W |
| ψ_{JB} | Junction-to-board characterization parameter | 8.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 2.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics application report](#).

6.4 DC Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|------|-----|------|------------------|
| Power | | | | | | |
| P_{ACT} | Device active power | All channels enabled (PD = L) | | 720 | 970 | mW |
| P_{STBY} | Device power consumption in standby power mode | All channels disabled (PD = H) | | 23 | 36 | mW |
| Control IO | | | | | | |
| V_{IH} | High level input voltage | SDA, SCL, PD, SEL pins | 2.1 | | | V |
| V_{IL} | Low level input voltage | SDA, SCL, PD, SEL pins | | | 1.08 | V |
| V_{OH} | High level output voltage | $R_{pull-up} = 4.7\text{ k}\Omega$ (SDA, SCL pins) | 2.1 | | | V |
| V_{OL} | Low level output voltage | $I_{OL} = -4\text{ mA}$ (SDA, SCL pins) | | | 0.4 | V |
| $I_{IH,SEL}$ | Input high leakage current for SEL pins | $V_{Input} = VCC$, for SEL pin | | | 100 | μA |
| I_{IH} | Input high leakage current | $V_{Input} = VCC$, (SCL, SDA, PD pins) | | | 10 | μA |
| I_{IL} | Input low leakage current | $V_{Input} = 0\text{ V}$, (SCL, SDA, PD, SEL pins) | -10 | | | μA |
| $I_{IH,FS}$ | Input high leakage current for fail safe input pins | $V_{Input} = 3.6\text{ V}$, $VCC = 0\text{ V}$, (SCL, SDA, PD, SEL pins) | | | 200 | μA |
| $C_{IN-CTRL}$ | Input capacitance | SCL, SDA, PD, SEL pins | | 1.6 | | pF |
| 5 Level IOs (MODE, GAIN, EQ1, EQ0, RX_DET pins) | | | | | | |
| I_{IH_5L} | Input high leakage current, 5 level IOs | $V_{IN} = 2.5\text{ V}$ | | | 10 | μA |
| I_{IL_5L} | Input low leakage current for all 5 level IOs except MODE. | $V_{IN} = GND$ | -10 | | | μA |
| $I_{IL_5L,MODE}$ | Input low leakage current for MODE pin | $V_{IN} = GND$ | -200 | | | μA |
| Receiver | | | | | | |
| $V_{RX-DC-CM}$ | RX DC Common Mode Voltage | Device is in active or standby state | | 1.4 | | V |
| Z_{RX-DC} | Rx DC Single-Ended Impedance | | | 50 | | Ω |
| $Z_{RX-HIGH-IMP-DC-POS}$ | DC input CM input impedance during Reset or power-down | Inputs are at $V_{RX-DC-CM}$ voltage | 20 | | | $\text{k}\Omega$ |
| Transmitter | | | | | | |
| $Z_{TX-DIFF-DC}$ | DC Differential Tx Impedance | Impedance of Tx during active signaling, $V_{ID,diff} = 1\text{Vpp}$ | | 100 | | Ω |
| $V_{TX-DC-CM}$ | Tx DC common mode Voltage | | | 1.0 | | V |
| $I_{TX-SHORT}$ | Tx Short Circuit Current | Total current the Tx can supply when shorted to GND | | 70 | | mA |

6.5 High Speed Electrical Characteristics

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|--|--|-----|-----|-----|------|
| Receiver | | | | | | |
| RL _{RX-DIFF} | Input differential return loss | 50 MHz to 1.25 GHz | | -22 | | dB |
| | | 1.25 GHz to 2.5 GHz | | -22 | | dB |
| | | 2.5 GHz to 4.0 GHz | | -20 | | dB |
| | | 4.0 GHz to 8.0 GHz | | -13 | | dB |
| | | 8.0 GHz to 16 GHz | | -9 | | dB |
| RL _{RX-CM} | Input common-mode return loss | 50 MHz to 2.5 GHz | | -20 | | dB |
| | | 2.5 GHz to 8.0 GHz | | -14 | | dB |
| | | 8.0 GHz to 16 GHz | | -9 | | dB |
| XT _{RX} | Receive-side pair-to-pair isolation | Minimum over 10 MHz to 16 GHz range | | -45 | | dB |
| Transmitter | | | | | | |
| V _{TX-AC-CM-PP} | Tx AC Peak-to-Peak Common Mode Voltage | Measured with lowest EQ, GAIN = L4; PRBS-7, 32 Gbps, over at least 10 ⁶ bits using a bandpass-Pass Filter from 30 KHz - 500 MHz | | | 50 | mVpp |
| V _{TX-RCV-DETECT} | Amount of Voltage change allowed during Receiver Detection | Measured while Tx is sensing whether a low-impedance Receiver is present. No load is connected to the driver output | 0 | | 600 | mV |
| RL _{TX-DIFF} | Output differential return loss | 50 MHz to 1.25 GHz | | -22 | | dB |
| | | 1.25 GHz to 2.5 GHz | | -22 | | dB |
| | | 2.5 GHz to 4.0 GHz | | -21 | | dB |
| | | 4.0 GHz to 8.0 GHz | | -15 | | dB |
| | | 8.0 GHz to 16 GHz | | -10 | | dB |
| RL _{TX-CM} | Output Common-mode return loss | 50 MHz to 2.5 GHz | | -16 | | dB |
| | | 2.5 GHz to 8.0 GHz | | -12 | | dB |
| | | 8.0 GHz to 16 GHz | | -10 | | dB |
| XT _{TX} | Transmit-side pair-to-pair isolation; Port A or Port B | Minimum over 10 MHz to 16 GHz range | | -50 | | dB |
| Device Datapath | | | | | | |
| T _{PLHD/PHLD} | Input-to-output latency (propagation delay) through a data channel | For either Low-to-High or High-to-Low transition. | | 90 | 130 | ps |
| L _{TX-SKEW} | Lane-to-Lane Output Skew | Between any two lanes within a single transmitter. | | | 20 | ps |
| T _{RJ-DATA} | Additive Random Jitter with data | Jitter through redriver minus the calibration trace. 32 Gbps PRBS15. 800 mVpp-diff input swing. | | 55 | | fs |
| T _{RJ-INTRINSIC} | Intrinsic additive Random Jitter with clock | Jitter through redriver minus the calibration trace. 32 GHz CK. 800 mVpp-diff input swing. | | 35 | | fs |
| JITTER _{TOTAL-DATA} | Additive Total Jitter with data | Jitter through redriver minus the calibration trace. 32 Gbps PRBS15. 800 mVpp-diff input swing. | | 1.0 | | ps |
| JITTER _{TOTAL-INTRINSIC} | Intrinsic additive Total Jitter with clock | Jitter through redriver minus the calibration trace. 16 GHz CK. 800 mVpp-diff input swing. | | 0.1 | | ps |

6.5 High Speed Electrical Characteristics (continued)

over operating free-air temperature and voltage range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----|------|-----|------|
| FLAT-GAIN | Broadband DC and AC flat gain - input to output, measured at DC | Minimum EQ, GAIN1/0=L0 | | -5.6 | | dB |
| | | Minimum EQ, GAIN1/0=L1 | | -3.8 | | dB |
| | | Minimum EQ, GAIN1/0=L2 | | -1.2 | | dB |
| | | Minimum EQ, GAIN1/0=L3 | | 2.6 | | dB |
| | | Minimum EQ, GAIN1/0=L4 (Float) | | 0.6 | | dB |
| EQ-MAX _{16G} | EQ boost at max setting (EQ INDEX = 19) | AC gain at 16 GHz relative to gain at 100 MHz. | | 24.0 | | dB |
| LINEARITY-DC | Output DC Linearity. | at 0dB Flat Gain | | 1700 | | mVpp |
| LINEARITY-AC | Output AC Linearity at 32 Gbps | at 0dB Flat Gain | | 930 | | mVpp |

6.6 SMBUS/I2C Timing Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|---|--|-----|-----|-----|------|
| Secondary Mode | | | | | | |
| t _{SP} | Pulse width of spikes which must be suppressed by the input filter | | | | 50 | ns |
| t _{HD-STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated | | 0.6 | | | μs |
| t _{LOW} | LOW period of the SCL clock | | 1.3 | | | μs |
| T _{HIGH} | HIGH period of the SCL clock | | 0.6 | | | μs |
| t _{SU-STA} | Set-up time for a repeated START condition | | 0.6 | | | μs |
| t _{HD-DAT} | Data hold time | | 0 | | | μs |
| T _{SU-DAT} | Data setup time | | 0.1 | | | μs |
| t _r | Rise time of both SDA and SCL signals | Pull-up resistor = 4.7 kΩ, C _b = 10pF | | 120 | | ns |
| t _f | Fall time of both SDA and SCL signals | Pull-up resistor = 4.7 kΩ, C _b = 10pF | | 2 | | ns |
| t _{SU-STO} | Set-up time for STOP condition | | 0.6 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | | 1.3 | | | μs |
| t _{VD-DAT} | Data valid time | | | | 0.9 | μs |
| t _{VD-ACK} | Data valid acknowledge time | | | | 0.9 | μs |
| C _b | capacitive load for each bus line | | | | 400 | pF |

6.7 Typical Characteristics

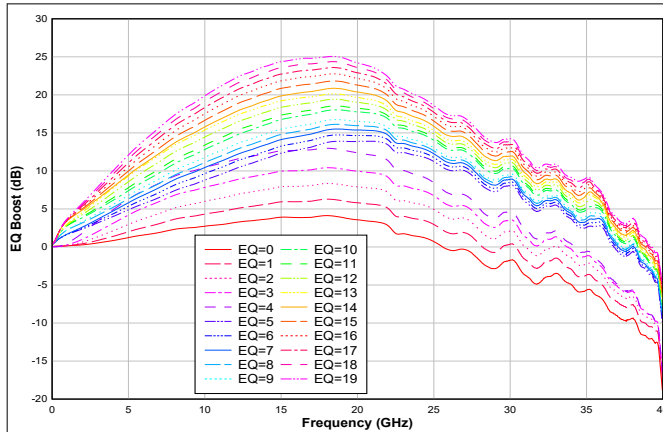


图 6-1. Typical EQ Boost vs Frequency

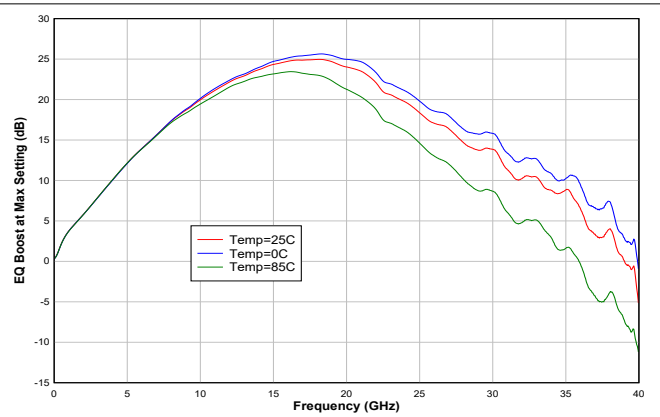


图 6-2. Typical EQ Boost at Max Setting vs Frequency at Different Temperature with EQ=19

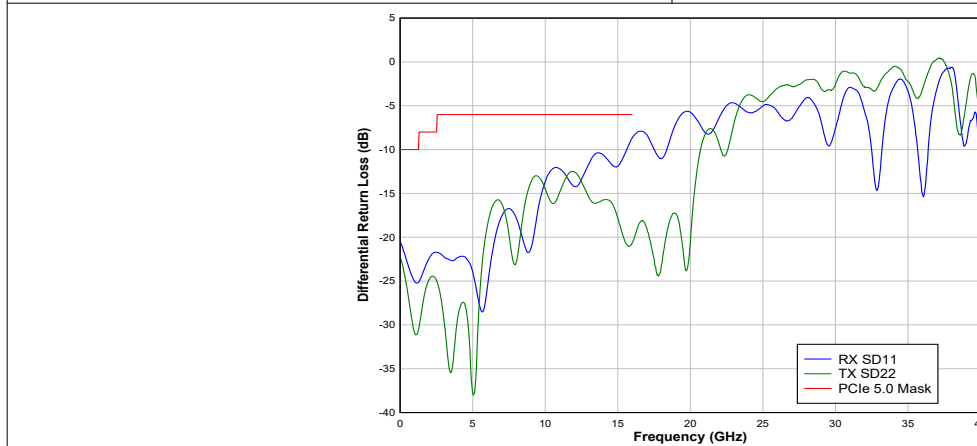


图 6-3. Typical Differential Return Loss

6.8 Typical Jitter Characteristics

图 6-4, 图 6-5, and 图 6-6 illustrate eye diagrams at source, through calibration traces, and through SN75LVPE5412 respectively.

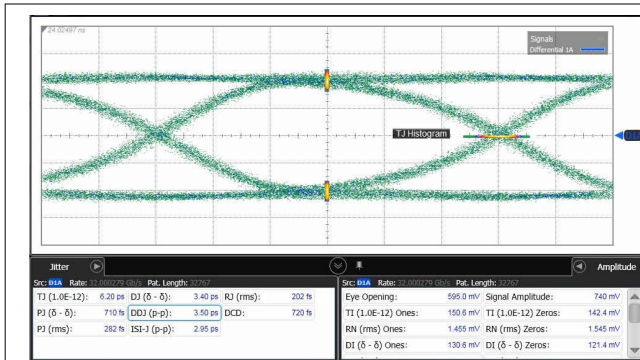


图 6-4. 32 Gbps 800 mV PRBS15 Source (1 dB Loss)

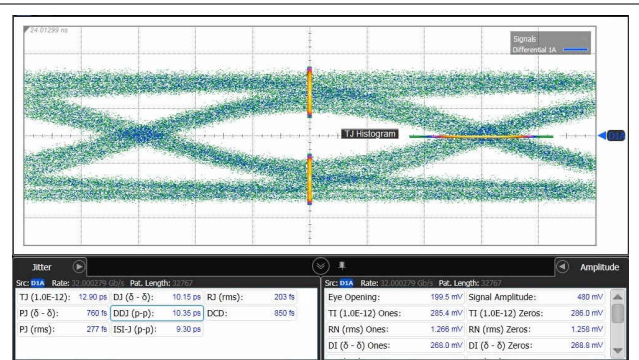


图 6-5. Through Calibration Trace (6.5 dB Loss)



图 6-6. Through SN75LVPE5412 (6.5 dB loss and DUT EQ=0)

7 Detailed Description

7.1 Overview

The SN75LVPE5412 is a four channel linear redriver with integrated demultiplexer (demux). The low-power high-performance linear repeater or redriver is designed to support PCIe 1.0, 2.0, 3.0, 4.0, and 5.0. The device is a protocol agnostic linear redriver that can operate for other AC-coupled interface up to 32 Gbps.

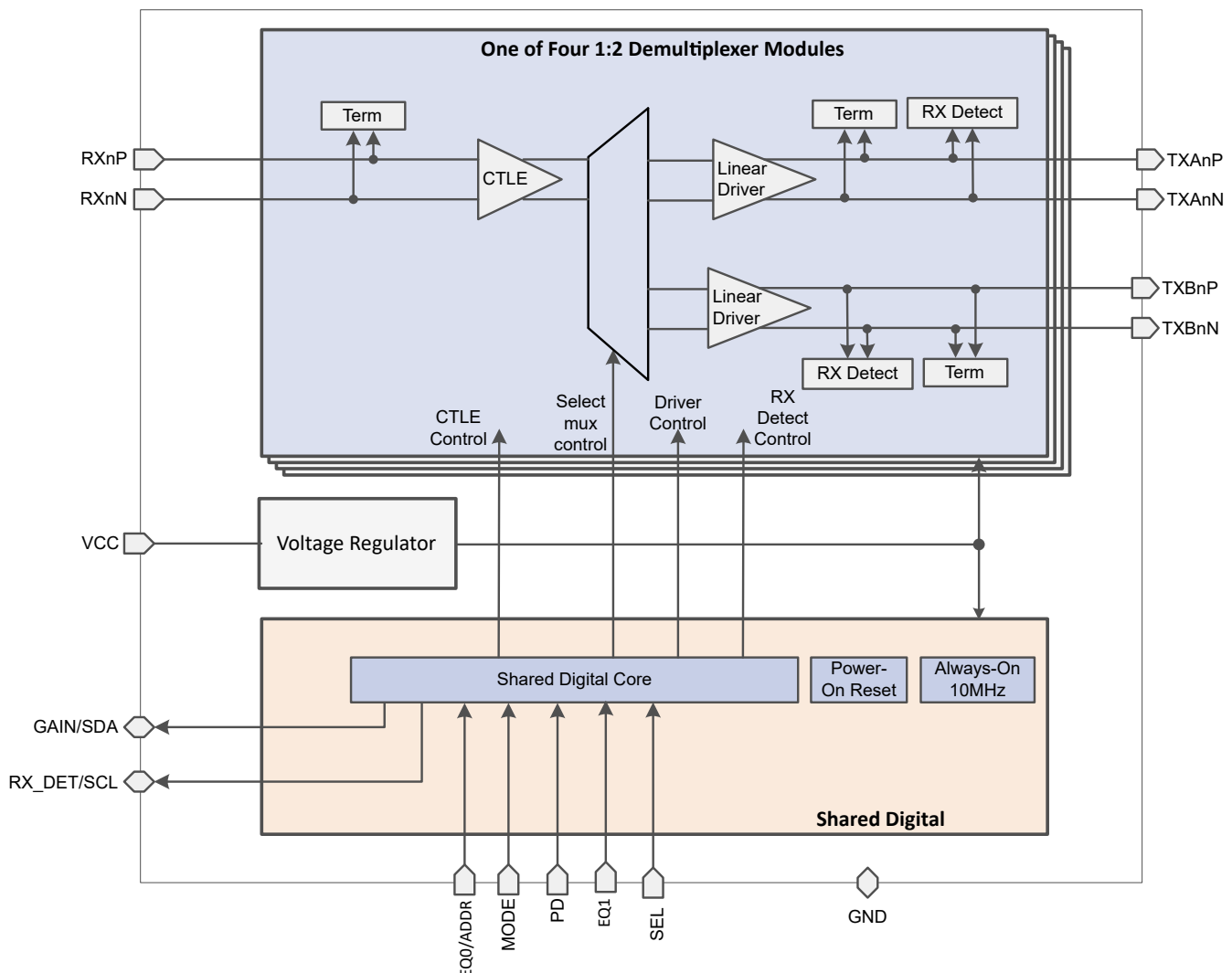
The signal channels of the SN75LVPE5412 operate independently from one another. Each channel includes a continuous-time linear equalizer (CTLE) and a linear output driver, which together compensate for a lossy transmission channel between the source transmitter and the final receiver. The linearity of the data path is specifically designed to preserve any transmit equalization while keeping PCIe receiver's (either from Root Complex or Endpoint) equalization effective.

The SN75LVPE5412 can be configured in two different ways:

Pin Mode - device control configuration is done solely by strap pins. Pin mode is expected to be good enough for many system implementation needs.

SMBus/I²C Secondary Mode - provides most flexibility. Requires an external SMBus/I²C primary device to configure SN75LVPE5412 though writing to its secondary address.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Five-Level Control Inputs

The SN75LVPE5412 has five 5-level inputs pins (EQ1, EQ0, GAIN, MODE, and RX_DET) that are used to control the configuration of the device. These 5-level inputs use a resistor divider to help set the 5 valid levels and provide a wider range of control settings. External resistors must be of 10% tolerance or better. The EQ0, EQ1, GAIN, and RX_DET pins are sampled at power-up only. The MODE pin can be exercised at device power up or in normal operation mode.

表 7-1. 5-Level Control Pin Settings

| LEVEL | SETTING |
|-------|----------------|
| L0 | 1 kΩ to GND |
| L1 | 8.25 kΩ to GND |
| L2 | 24.9 kΩ to GND |
| L3 | 75 kΩ to GND |
| L4 | F (Float) |

7.3.2 Linear Equalization

The SN75LVPE5412 receivers feature a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of a passive channel. The receivers implement two stage linear equalizer for wide range of equalization capability. The equalizer stages also provide flexibility to make subtle modifications of mid-frequency boost for best EQ gain profile match with wide range of channel media characteristics. The EQ profile control feature is only available in SMBus/I²C Mode. In Pin Mode the settings are optimized for FR4 traces.

表 7-2 shows available equalization boost through EQ control pins or SMBus/I²C registers. In Pin Control mode EQ1 and EQ0 pins set equalization boost for all channels. In I²C Mode individual channels can be independently programmed for EQ boost.

表 7-2. Equalization Control Settings

| EQ INDEX | EQUALIZATION SETTING | | | | | | TYPICAL EQ BOOST (dB) | |
|----------|----------------------|-----|-----------------------------|---------------|----------------|------------------|-----------------------|-----------|
| | Pin Mode | | SMBus/I ² C Mode | | | | At 8 GHz | At 16 GHz |
| | EQ1 | EQ0 | eq_stage1_3:0 | eq_stage2_2:0 | eq_profile_3:0 | eq_stage1_bypass | | |
| 0 | L0 | L0 | 0 | 0 | 0 | 1 | 2.0 | 4.0 |
| 1 | L0 | L1 | 1 | 0 | 0 | 1 | 4.0 | 6.0 |
| 2 | L0 | L2 | 3 | 0 | 0 | 1 | 5.0 | 8.0 |
| 3 | L0 | L3 | 7 | 0 | 0 | 1 | 7.0 | 10.0 |
| 4 | L0 | L4 | 7 | 1 | 0 | 1 | 8.0 | 12.0 |
| 5 | L1 | L0 | 0 | 0 | 1 | 0 | 7.0 | 12.0 |
| 6 | L1 | L1 | 1 | 0 | 1 | 0 | 7.5 | 13.0 |
| 7 | L1 | L2 | 2 | 0 | 1 | 0 | 8.0 | 14.0 |
| 8 | L1 | L3 | 3 | 0 | 3 | 0 | 9.0 | 15.0 |
| 9 | L1 | L4 | 4 | 0 | 3 | 0 | 10.0 | 15.5 |
| 10 | L2 | L0 | 5 | 1 | 7 | 0 | 10.5 | 16.0 |
| 11 | L2 | L1 | 6 | 1 | 7 | 0 | 11.0 | 17.0 |
| 12 | L2 | L2 | 8 | 1 | 7 | 0 | 12.0 | 17.5 |

表 7-2. Equalization Control Settings (continued)

| EQ INDEX | EQUALIZATION SETTING | | | | | | TYPICAL EQ BOOST (dB) | |
|----------|----------------------|-----|-----------------------------|---------------|----------------|------------------|-----------------------|-----------|
| | Pin Mode | | SMBus/I ² C Mode | | | | At 8 GHz | At 16 GHz |
| | EQ1 | EQ0 | eq_stage1_3:0 | eq_stage2_2:0 | eq_profile_3:0 | eq_stage1_bypass | | |
| 13 | L2 | L3 | 10 | 1 | 7 | 0 | 12.5 | 18.5 |
| 14 | L2 | L4 | 10 | 2 | 15 | 0 | 13.0 | 19.0 |
| 15 | L3 | L0 | 11 | 3 | 15 | 0 | 14.0 | 20.0 |
| 16 | L3 | L1 | 12 | 4 | 15 | 0 | 15.0 | 21.0 |
| 17 | L3 | L2 | 13 | 5 | 15 | 0 | 16.0 | 22.0 |
| 18 | L3 | L3 | 14 | 6 | 15 | 0 | 16.5 | 23.0 |
| 19 | L3 | L4 | 15 | 7 | 15 | 0 | 17.0 | 24.0 |

7.3.3 Flat Gain

The GAIN pin can be used to set the overall datapath flat gain (broadband gain including high frequency) of the SN75LVPE5412 when the device is in Pin Mode. The pin GAIN sets the Flat-Gain for all channels. In I²C Mode each channel can be independently set. 表 7-3 shows flat gain control configuration settings. The default recommendation for most systems will be GAIN = L4 (float) that provides flat gain of 0 dB.

The flat gain and equalization of the SN75LVPE5412 must be set such that the output signal swing at DC and high frequency does not exceed the DC and AC linearity ranges of the devices, respectively.

表 7-3. Flat Gain Configuration Settings

| Pin Mode GAIN | I ² C Mode flat_gain_2:0 | Flat Gain |
|------------------|--|----------------------------------|
| L0 | 0 | -5.6 dB |
| L1 | 1 | -3.8 dB |
| L2 | 3 | -1.2 dB |
| L3 | 7 | +2.6 dB |
| L4 (float) | 5 | +0.6 dB (default recommendation) |

7.3.4 Receiver Detect State Machine

The SN75LVPE5412 deploys an RX detect state machine that governs the RX detection cycle as defined in the PCI express specifications. At device power up or through manually triggered event using PD or SEL pin or writing to the relevant I²C/SMBus register, the redriver determines whether or not a valid PCI express termination is present at the far end of the link. The RX_DET pin of SN75LVPE5412 provides additional flexibility for system designers to appropriately set the device in desired mode according to 表 7-4. For the PCIe application the RX_DET pin can be left floating for default settings.

Note power up ramp or PD/SEL event triggers RX detect for all four channels. In applications where SN75LVPE5412 channels are used for multiple PCIe links, the RX detect function can be performed for individual channels through writing in appropriate I²C/SMBus registers.

表 7-4. Receiver Detect State Machine Settings

| PD | RX_DET | RX Common-mode Impedance | COMMENTS |
|----|--------|--------------------------|---|
| L | L0 | Always 50 Ω | PCI Express RX detection state machine is disabled. Recommended for non PCIe interface use case where the SN75LVPE5412 is used as buffer with equalization. |

表 7-4. Receiver Detect State Machine Settings (continued)

| PD | RX_DET | RX Common-mode Impedance | COMMENTS |
|----|------------|---|---|
| L | L1 | Pre Detect: Hi-Z Post Detect: 50 Ω . | Outputs polls until 3 consecutive valid detections |
| L | L2 | Pre Detect: Hi-Z Post Detect: 50 Ω . | Outputs polls until 2 consecutive valid detections |
| L | L3 | Pre Detect: Hi-Z Post Detect: 50 Ω . | Reserved |
| L | L4 (Float) | Pre Detect: Hi-Z Post Detect: 50 Ω . | TX polls every $\approx 150 \mu\text{s}$ until valid termination is detected. RX CM impedance held at Hi-Z until detection Reset by asserting PD high for 200 μs then low. Recommended default setting for PCIe. |
| H | X | Hi-Z | Reset Channels and set their RX impedance to Hi-Z |

7.4 Device Functional Modes

7.4.1 Active PCIe Mode

The device is in normal operation with PCIe state machine enabled by RX_DET = L4 (float). This mode is recommended for PCIe use cases. In this mode, the PD pin is driven low in a system (for example, by PCIe connector "PRSNT" signal). In this mode, the device redrives and equalizes PCIe RX or TX signals to provide better signal integrity.

7.4.2 Active Buffer Mode

The device is in normal operation with PCIe state machine disabled by RX_DET = L0. This mode is recommended for non-PCIe use cases. In this mode, the device is working as a buffer to provide linear equalization to improve signal integrity.

7.4.3 Standby Mode

The device is in standby mode invoked by PD = H. In this mode, the device is in standby mode conserving power.

7.5 Programming

7.5.1 Pin Mode

The SN75LVPE5412 can be fully configured through pin-strap pins. In this mode the device uses 2-level and 5-level pins for device control and signal integrity optimum settings.

7.5.2 SMBUS/I²C Register Control Interface

If MODE = L2 (SMBus / I²C secondary control mode), the SN75LVPE5412 is configured for best signal integrity through a standard I²C or SMBus interface that may operate up to 400 kHz. The secondary address of the SN75LVPE5412 is determined by the pin strap settings on the ADDR and MODE pins. 表 7-5 shows the eight possible secondary addresses (7-bit) for each channel banks of the device. In SMBus/I²C modes the SCL, SDA pins must be pulled up to a 3.3 V supply with a pull-up resistor. The value of the resistor depends on total bus capacitance. 4.7 kΩ is a good first approximation for a bus capacitance of 10 pF.

表 7-5. SMBUS/I²C Secondary Address Settings

| MODE | ADDR | 7-bit Secondary Address Channels 0-1 | 7-bit Secondary Address Channels 2-3 |
|------|------|--------------------------------------|--------------------------------------|
| L1 | L0 | 0x18 | 0x19 |
| L1 | L1 | 0x1A | 0x1B |
| L1 | L2 | 0x1C | 0x1D |
| L1 | L3 | 0x1E | 0x1F |
| X | L4 | Reserved | Reserved |
| L2 | L0 | 0x20 | 0x21 |
| L2 | L1 | 0x22 | 0x23 |

表 7-5. SMBUS/I2C Secondary Address Settings (continued)

| MODE | ADDR | 7-bit Secondary Address Channels 0-1 | 7-bit Secondary Address Channels 2-3 |
|------|------|--------------------------------------|--------------------------------------|
| L2 | L2 | 0x24 | 0x25 |
| L2 | L3 | 0x26 | 0x27 |

The SN75LVPE5412 has two types of registers:

- **Shared Registers:** These registers can be accessed at any time and are used for device-level configuration, status read back, control, or to read back the device ID information.
- **Channel Registers:** These registers are used to control and configure specific features for each individual channel. All channels have the same register set and can be configured independent of each other or configured as a group via broadcast writes to Bank 0 or Bank 1.

The SN75LVPE5412 features two banks of channels, Bank 0 (Channels 0-1) and Bank 1 (Channels 2-), each featuring a separate register set and requiring a unique SMBus secondary address.

| Channel Registers Base Address | Channel Bank 0 Access | Channel Bank 1 Access |
|--------------------------------|---|---|
| 0x00 | Channel 0 registers | Channel 2 registers |
| 0x20 | Channel 0 registers | Channel 2 registers |
| 0x40 | Channel 1 registers | Channel 3 registers |
| 0x60 | Channel 1 registers | Channel 3 registers |
| 0x80 | Broadcast write channel Bank 0 registers, read channel 0 registers | Broadcast write channel Bank 1 registers, read channel 2 registers |
| 0xE0 | Bank 0 Share registers | Bank 1 Share registers |

7.5.2.1 Shared Registers

表 7-6. General Registers (Offset = 0xE2)

| Bit | Field | Type | Reset | Description |
|-----|--------------|-------|-------|--|
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | rst_i2c_regs | RW/SC | 0x0 | Device reset control: Reset all I2C registers to default values (self-clearing). |
| 5 | rst_i2c_mas | RW/SC | 0x0 | Reset I ² C Primary (self-clearing). |
| 4-0 | RESERVED | R | 0x0 | Reserved |

表 7-7. DEVICE_ID0 Register (Offset = 0xF0)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-----------------------|
| 7-4 | RESERVED | R | 0x0 | Reserved |
| 3 | device_id0_3 | R | 0x1 | Device ID0 [3:1]: 111 |
| 2 | device_id0_2 | R | 0x1 | see MSB |
| 1 | device_id0_1 | R | 0x1 | see MSB |
| 0 | RESERVED | R | X | Reserved |

表 7-8. DEVICE_ID1 Register (Offset = 0xF1)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-----------------------------------|
| 7 | device_id[7] | R | 0x0 | Device ID 0010 1000: SN75LVPE5412 |
| 6 | device_id[6] | R | 0x0 | see MSB |
| 5 | device_id[5] | R | 0x1 | see MSB |
| 4 | device_id[4] | R | 0x0 | see MSB |
| 3 | device_id[3] | R | 0x1 | see MSB |
| 2 | device_id[2] | R | 0x0 | see MSB |

表 7-8. *DEVICE_ID1 Register (Offset = 0xF1) (continued)*

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|-------------|
| 1 | device_id[1] | R | 0x0 | see MSB |
| 0 | device_id[0] | R | 0x0 | see MSB |

7.5.2.2 Channel Registers

表 7-9. RX Detect Status Register (Channel Register Base + Offset = 0x00)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7 | RX_det_comp_p | R | 0x0 | RX Detect positive data pin status: 0: Not detected 1: Detected - the value is latched |
| 6 | RX_det_comp_n | R | 0x0 | RX Detect negative data pin status: 0: Not detected 1: Detected - the value is latched |
| 5-0 | RESERVED | R | 0x0 | Reserved |

表 7-10. EQ Gain Control Register (Channel Register Base + Offset = 0x01)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7 | eq_stage1_bypass | R/W | 0x0 | Enable EQ stage 1 bypass: 0: Bypass disabled 1: Bypass enabled |
| 6 | eq_stage1_3 | R/W | 0x0 | EQBoost stage 1 control See 表 7-2 for details |
| 5 | eq_stage1_2 | R/W | 0x0 | |
| 4 | eq_stage1_1 | R/W | 0x0 | |
| 3 | eq_stage1_0 | R/W | 0x0 | |
| 2 | eq_stage2_2 | R/W | 0x0 | EQ Boost stage 2 control See 表 7-2 for details |
| 1 | eq_stage2_1 | R/W | 0x0 | |
| 0 | eq_stage2_0 | R/W | 0x0 | |

表 7-11. EQ Gain / Flat Gain Control Register (Channel Register Base + Offset = 0x03)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7 | RESERVED | R | 0x0 | Reserved |
| 6 | eq_profile_3 | R/W | 0x0 | EQ mid-frequency boost profile See 表 7-2 for details |
| 5 | eq_profile_2 | R/W | 0x0 | |
| 4 | eq_profile_1 | R/W | 0x0 | |
| 3 | eq_profile_0 | R/W | 0x0 | |
| 2 | flat_gain_2 | R/W | 0x1 | Flat gain select: See 表 7-3 for details |
| 1 | flat_gain_1 | R/W | 0x0 | |
| 0 | flat_gain_0 | R/W | 0x1 | |

表 7-12. RX Detect Control Register (Channel Register Base + Offset = 0x04)

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 7-3 | RESERVED | R | 0x0 | Reserved |
| 2 | mr_RX_det_man | R/W | 0x0 | Manual override of RX_detect_p/n decision: 0: RX detect state machine is enabled 1: RX detect state machine is overridden - always valid RX termination detected |
| 1 | en_RX_det_count | R/W | 0x0 | Enable additional RX detect polling 0: Additional RX detect polling disabled 1: Additional RX detect polling enabled |
| 0 | sel_RX_det_count | R/W | 0x0 | Select number of valid RX detect polls - gated by en_RX_det_count = 1 0: Device transmitters poll until 2 consecutive valid detections 1: Device transmitters poll until 3 consecutive valid detections |

表 7-13. PD Override Register (Channel Register Base + Offset = 0x05)

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|----------|---|
| 7 | device_en_override | R/W | 0x0 | Enable power down overrides through SMBus/I ² C 0: Manual override disabled 1: Manual override enabled |
| 6-0 | device_en | R/W | 0x111111 | Manual power down of redriver various blocks - gated by device_en_override = 1 111111: All blocks are enabled 000000: All blocks are disabled |

表 7-14. RX Detect Reset Register (Channel Register Base + Offset = 0x0A)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-3 | RESERVED | R | 0x0 | Reserved |
| 2 | mr_RX_det_rst | R/W | 0x0 | RX Detect state machine reset. Toggle the bit if RX Detect machine needs to be reset in I ² C mode 0: state machine is not reset 1: RX detect state machine is reset |
| 1-0 | RESERVED | R/W | 0x0 | Reserved |

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN75LVPE5412 is a high-speed linear repeater with integrated demux. The device extends the reach of differential channels impaired by loss from transmission media like PCBs and cables. It can be deployed in a variety of different systems. The following sections outline typical applications and their associated design considerations.

8.2 Typical Applications

The SN75LVPE5412 is a PCI Express linear redriver that can also be configured as interface agnostic redriver by disabling its RX detect feature. The device can be used in a wide range of interfaces including:

- PCI Express
- Ultra Path Interconnect (UPI)
- SATA
- SAS
- Display Port

8.2.1 PCIe x8 Lane Switching

The SN75LVPE5412 and SN75LVPE5421 can be used to switch PCIe lanes from a CPU into one of the two PCIe CEM connectors. 图 8-1 shows a simplified schematic for the following configuration:

- Two SN75LVPE5412 demultiplex eight TX channels from the CPU into one of the two PCIe slots.
- Two SN75LVPE5421 multiplex eight RX channels from one of the two PCIe slots to CPU.

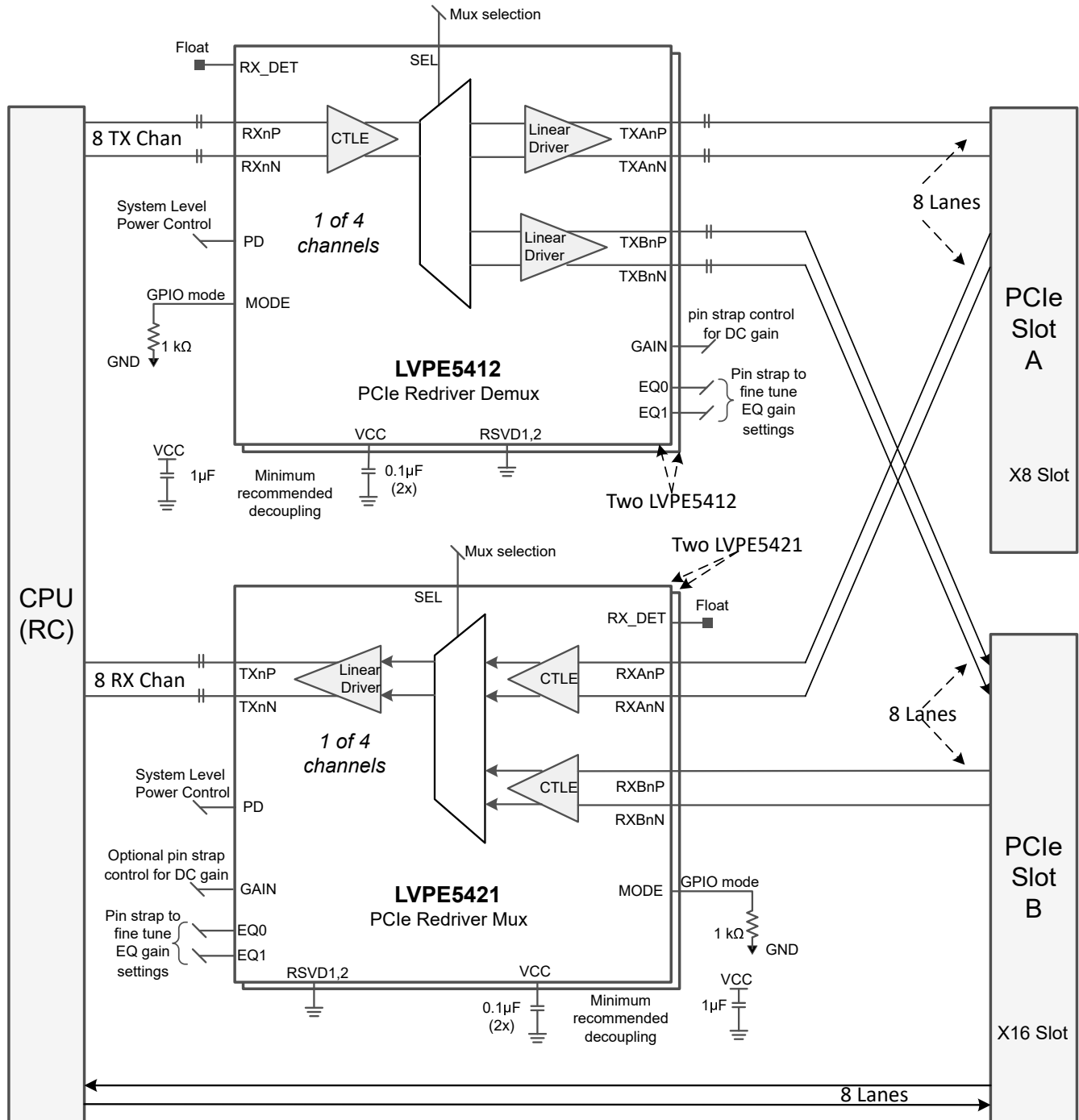


图 8-1. Simplified Schematic for PCIe Lane Switching

8.2.1.1 Design Requirements

As with any high-speed design, there are many factors which influence the overall performance. The following list indicates critical areas for consideration during design:

- Use 85 Ω impedance traces when interfacing with PCIe CEM connectors. Length matching on the P and N traces should be done on the single-ended segments of the differential pair.
- Use a uniform trace width and trace spacing for differential pairs.
- Place AC-coupling capacitors near to the receiver end of each channel segment to minimize reflections.
- For Gen 3.0, 4.0, and 5.0, AC-coupling capacitors of 220 nF are recommended, set the maximum body size to 0402, and add a cutout void on the GND plane below the landing pad of the capacitor to reduce parasitic capacitance to GND.
- Back-drill connector vias and signal vias to minimize stub length.
- Use reference plane vias to ensure a low inductance path for the return current.

8.2.1.2 Detailed Design Procedure

In PCIe Gen 3.0, 4.0, and 5.0 applications, the specification requires RX-TX link training to establish and optimize signal conditioning settings at 8.0, 16.0, and 32.0 Gbps, respectively. In link training, the RX partner requests a series of FIR - pre-shoot and de-emphasis coefficients (10 Presets) from the TX partner. The RX partner includes CTLE and DFE. The link training would pre-condition the signal, with an equalized link between the Root Complex and Endpoint.

Note: there is no link training in PCIe Gen 1.0 (2.5 Gbps) or PCIe Gen 2.0 (5.0 Gbps) applications. The SN75LVPE5412 is placed in between the TX and RX. It helps extend the PCB trace reach distance by boosting the attenuated signals with its equalization, which allows the user to recover the signal by the downstream RX more easily.

For operation in Gen 5.0, 4.0, and 3.0 links, the SN75LVPE5412 transmit outputs are designed to pass the TX Preset signaling onto the RX for the PCIe Gen 5.0, 4.0, and 3.0 link to train and optimize the equalization settings. The suggested setting for the device is GAIN = L4 (default). Adjustments to the EQ setting should be performed based on the channel loss to optimize the eye opening in the RX partner. The TX equalization presets or CTLE and DFE coefficients in the RX can also be adjusted to further improve the eye opening.

8.2.2 Protocol Agnostic Linear Redriver for High Speed Interfaces

The SN75LVPE5412 can be used as a four channel protocol agnostic linear redriver demultiplexer (demux) for data rates up to 32 Gbps. To use the device in a non-PCIe application, the RX_DET pin must be pin-strapped to GND with 1 kΩ resistor (L0).

This section illustrates how the SN75LVPE5412 can be used in DisplayPort (DP) application. The device is a linear redriver which is agnostic to DP link training. The DP link training negotiation between a display source and sink stays effective through the device. The redriver becomes part of the electrical channel along with passive traces, cables, and so forth, resulting in optimum source and sink parameters for best electrical link.

图 8-2 shows a simplified schematic for DisplayPort demultiplexing application using SN75LVPE5412. Auxiliary and Hot plug detect (HPD) are demuxed outside of the device. If system use case requires implementing DP power states, the device must be controlled by the I²C.

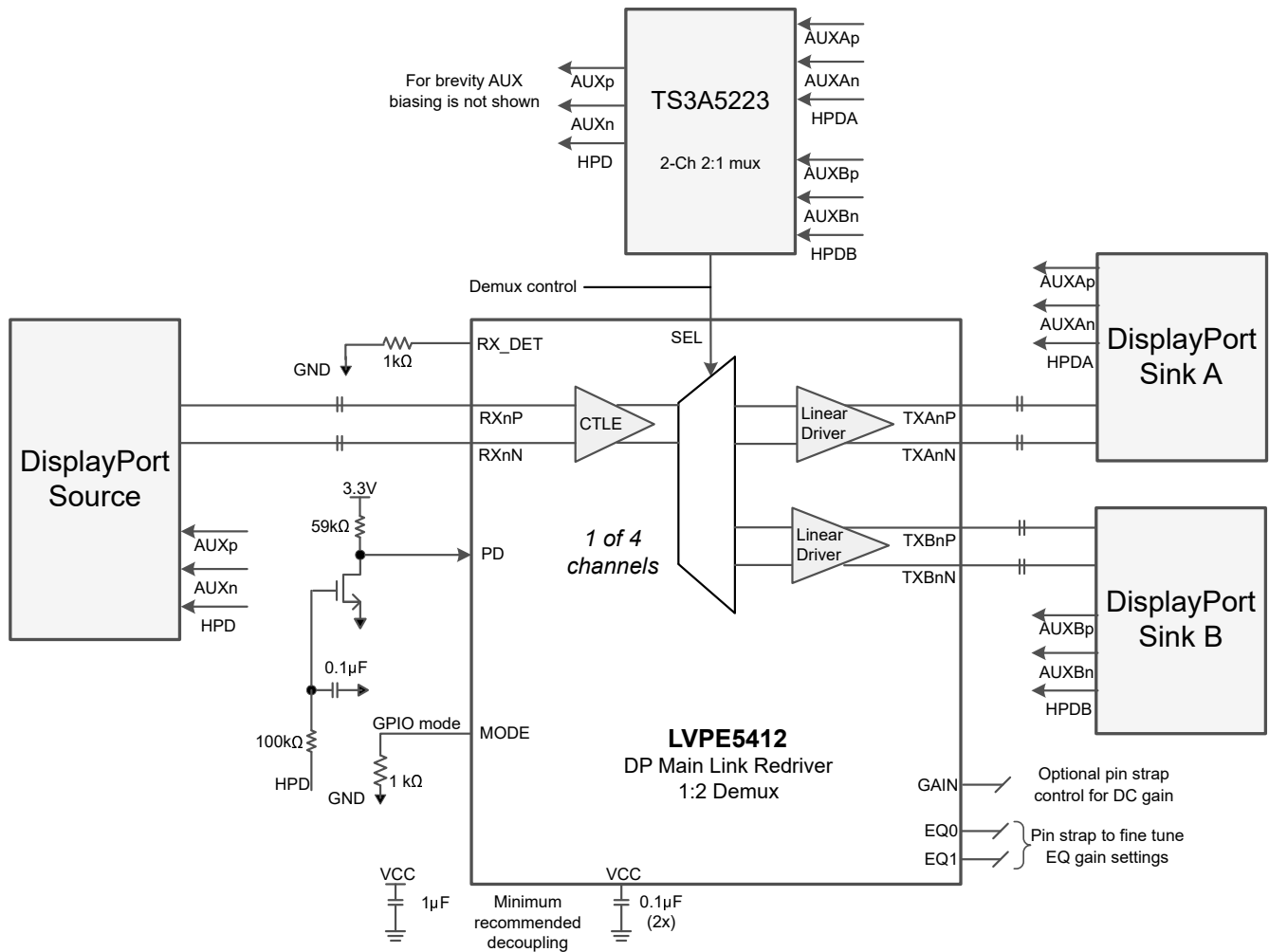


图 8-2. Simplified Schematic for DisplayPort Demultiplexer Application

The inverted DisplayPort HPD signal can be used to put the device into standby mode by using its PD pin. Note: in a DisplayPort link a sink can use HPD line to create an interrupt for its link partner source. If HPD signal is used for power management an RC filter must be installed to filter out HPD interrupt signals.

The SN75LVPE5412 can similarly be used for other AC-coupled high speed interfaces. Care must be taken to understand the specifications of the interface to ensure feasibility.

9 Power Supply Recommendations

Follow these general guidelines when designing the power supply:

1. The power supply should be designed to provide the operating conditions outlined in the recommended operating conditions section in terms of DC voltage, AC noise, and start-up ramp time.
2. The SN75LVPE5412 does not require any special power supply filtering, such as ferrite beads, provided that the recommended operating conditions are met. Only standard supply decoupling is required. Typical supply decoupling consists of a 0.1 μF capacitor per VCC pin, one 1.0 μF bulk capacitor per device, and one 10 μF bulk capacitor per power bus that delivers power to one or more devices. The local decoupling (0.1 μF) capacitors must be connected as close to the VCC pins as possible and with minimal path to the device ground pad.

10 Layout

10.1 Layout Guidelines

The following guidelines should be followed when designing the layout:

1. Decoupling capacitors should be placed as close to the VCC pins as possible. Placing the decoupling capacitors directly underneath the device is recommended if the board design permits.
2. High-speed differential signals TXnP/TXnN and RXnP/RXnN should be tightly coupled, skew matched, and impedance controlled.
3. Vias should be avoided when possible on the high-speed differential signals. When vias must be used, take care to minimize the via stub, either by transitioning through most or all layers or by back drilling.
4. GND relief can be used (but is not required) beneath the high-speed differential signal pads to improve signal integrity by counteracting the pad capacitance.
5. GND vias should be placed directly beneath the device connecting the GND plane attached to the device to the GND planes on other layers. This has the added benefit of improving thermal conductivity from the device to the board.

10.2 Layout Example

图 10-1 shows SN75LVPE5412 layout example.

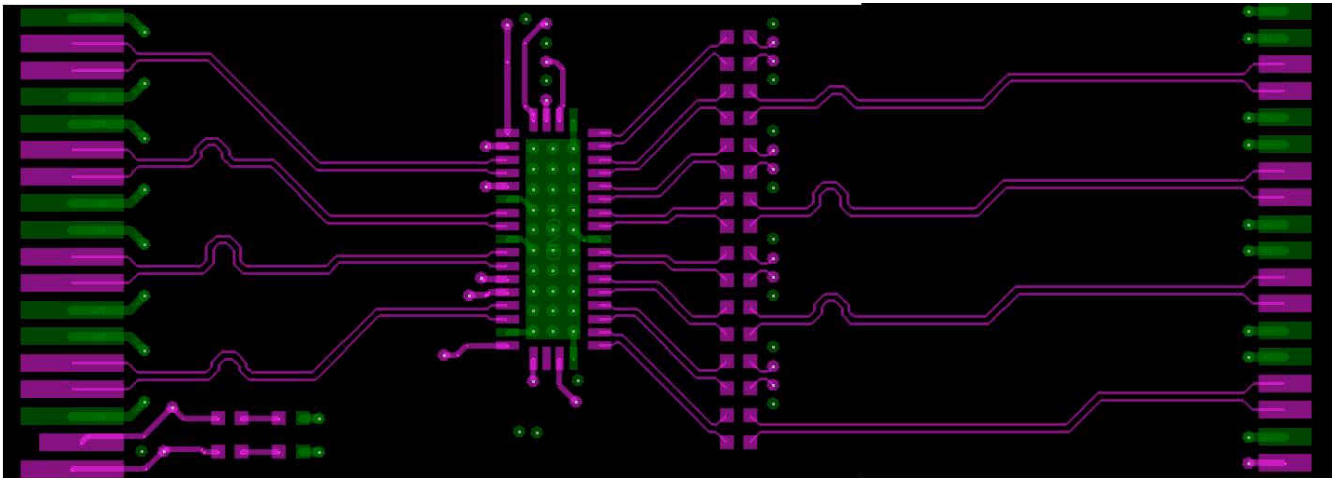


图 10-1. SN75LVPE5412 Layout Example

图 10-2 shows a layout illustration where two SN75LVPE5412 and two SN75LVPE5421 are used to switch 8 lanes between the two PCIe slots.

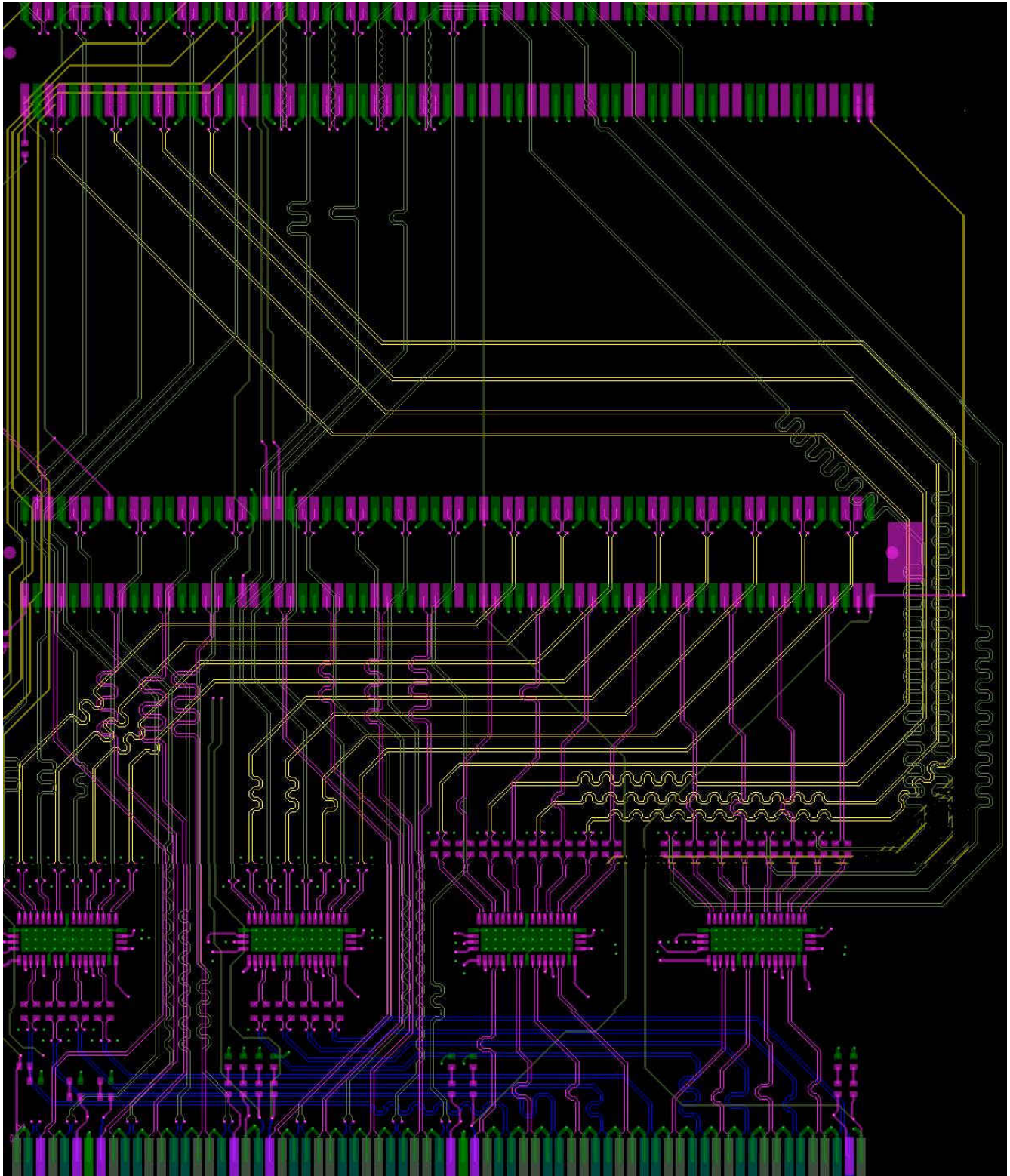


图 10-2. Layout Example for PCIe Lane Muxing Application

11 Device and Documentation Support

11.1 接收文档更新通知

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75LVPE5412RUAR | ACTIVE | WQFN | RUA | 42 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 85 | 5PR412 | Samples |
| SN75LVPE5412RUAT | ACTIVE | WQFN | RUA | 42 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 85 | 5PR412 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

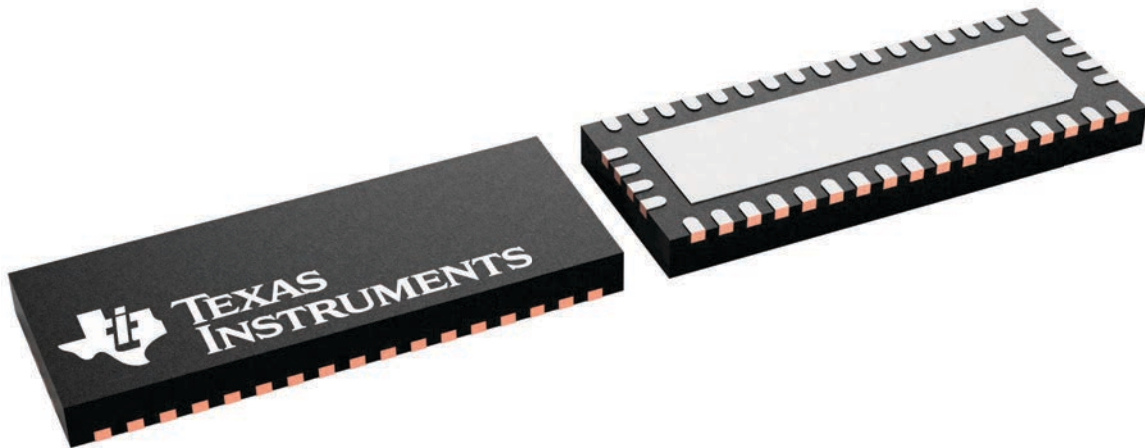
RUA 42

WQFN - 0.8 mm max height

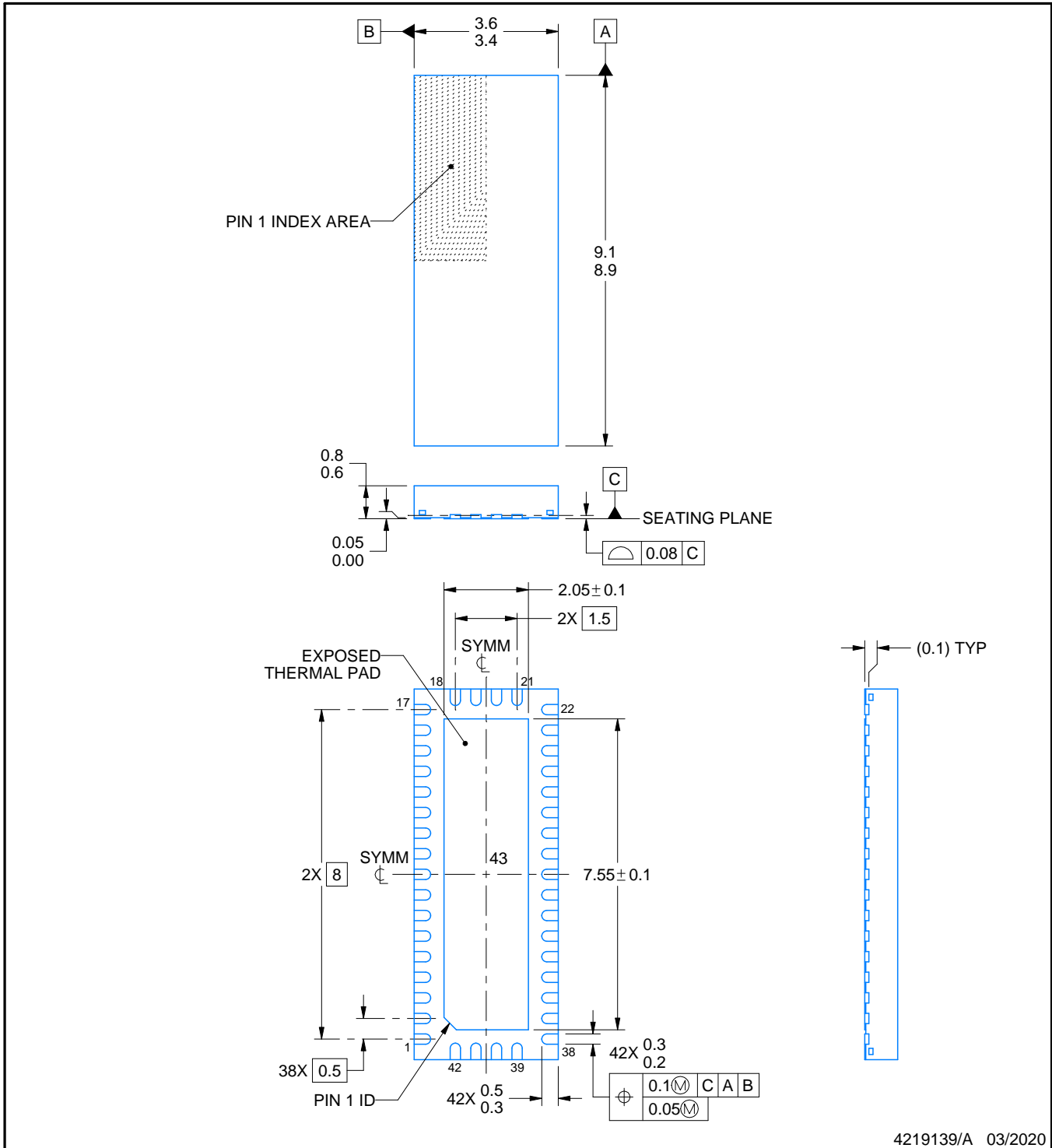
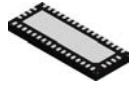
9 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4226504/A



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NOTES:

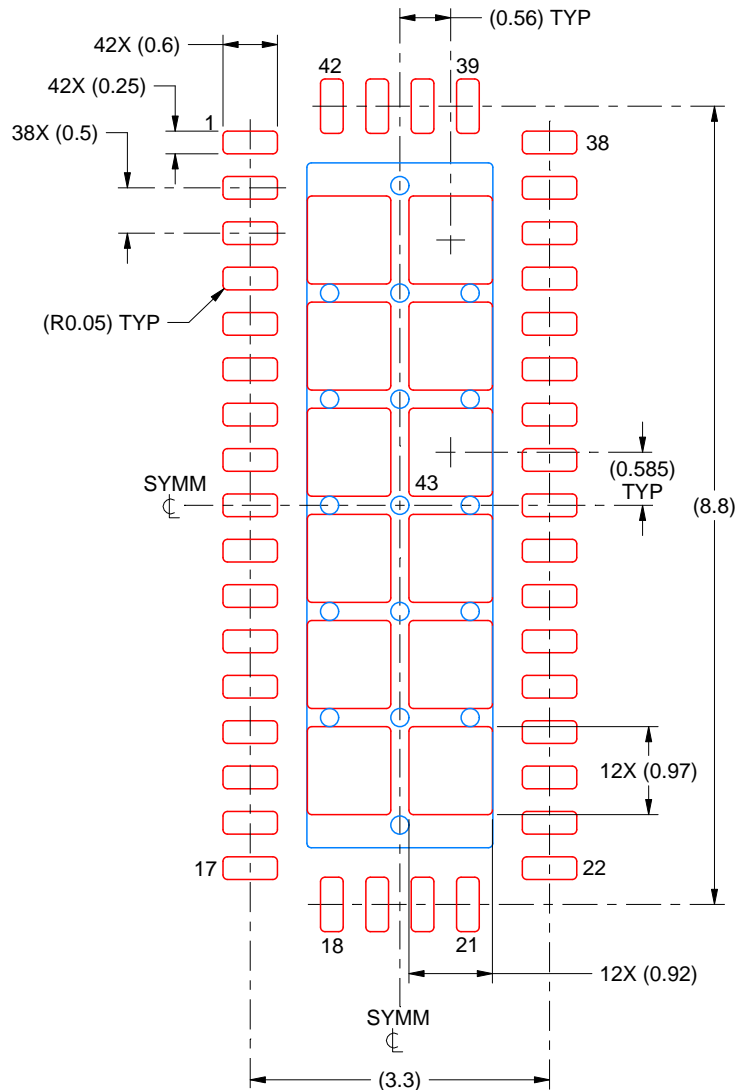
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RUA0042A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 12X

EXPOSED PAD 43
69% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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