TEXAS INSTRUMENTS
TIOS102, TIOS1023, TIOS1025
ZHCSMU4 – FEBRUARY 2022

具有集成浪涌保护功能的小封装 TIOS102 和 TIOS102x 数字传感器输出驱动器

1 特性

- 宽电源运行
  - 5V 至 36V 电源电压（TIOS102，TIOS1023）
  - 7V 至 36V 电源电压 (TIOS1025)
- PNP、NPN 或推挽可配置输出
- 提供功能安全
  - 有助于进行功能安全系统设计的文档
- 与 TIOS101(x) 引脚兼容，并提升了性能
  - 在 200mA 条件下，残余电压低，为 0.5V（典型值）
  - 有效驱动器电流限制功能
  - 改善了封装的热性能
  - 更低的驱动器压摆率，可减少过冲（最大 750ns）
- 集成保护特性，使系统更加稳健
  - 可配置驱动器过流限值（50mA 至 350mA）
  - VCC、OUT 和 GND 上高达 65V 的有效反极性保护特性
  - 过流、过热和 UVLO 的故障指示灯
- VCC 和 OUT 上集成 EMC 保护功能
  - ±8 kV IEC 61000-4-2 ESD 接触放电
  - ±4kV IEC 61000-4-4 电气快速瞬变
  - ±1.2kV/500Ω IEC 61000-4-5 浪涌
- 较大电感负载的快速退磁能力
- 较大容性负载驱动能力
- < 2.2mA 静态电源电流
- 集成式 LDO 选项可支持高达 20mA 的电流
  - TIOS1023：3.3V LDO
  - TIOS1025：5V LDO
- 扩展环境温度：-40°C 至 125°C
- 小型封装选项
  - 3mm x 3mm 10 引脚 VSON 封装（与 TIOS101 引脚兼容）
  - 1.7mm x 2.45mm WCSP 选项（预发布）

2 应用

- 接近开关
- 电容式和电感式传感器
- 传动器
- 数字输出

3 说明

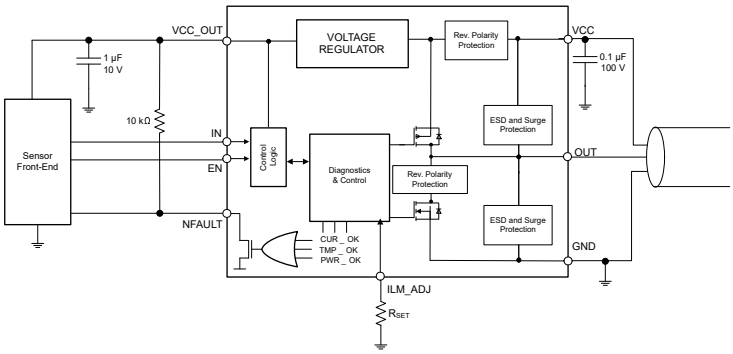
TIOS102(x) 器件可配置为高侧、低侧或推挽驱动器。这些器件能够承受高达 1.2kV (500Ω) 的 IEC 61000-4-5 浪涌，并集成反向极性保护功能。

只需通过一个引脚可编程接口便可轻松连接到电路。可使用外部电阻器配置输出电流限值。提供了故障报告和内部保护功能，可应对欠压、过流和过热条件。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TIOS102	VSON (10)	3.00mm x 3.00mm
TIOS1023		
TIOS1025		
TIOS102	DSBGA (12) (2)	1.7 mm x 2.45 mm
TIOS1023		

(1) 如需了解所有可订购器件，请参阅数据表末尾的可订购产品附录。
(2) 产品预发布



典型应用图

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

1 特性 1
2 应用 1
3 说明 1
4 Revision History 2
5 Pin Configuration and Functions 3
6 Specifications 5
6.1 Absolute Maximum Ratings 5
6.2 ESD Ratings 5
6.3 ESD Ratings - IEC Specifications 5
6.4 Recommended Operating Conditions 5
6.5 Thermal Information 6
6.6 Electrical Characteristics 6
6.7 Switching Characteristics 8
6.8 Typical Characteristics 9
7 Parameter Measurement Information 10
8 Detailed Description 11
8.1 Overview 11
8.2 Functional Block Diagrams 11
8.3 Feature Description 12
8.4 Device Functional Modes 17
9 Application Information Disclaimer 19
9.1 Application Information 19
9.2 Typical Application 19
10 Power Supply Recommendations 20
11 Layout 21
11.1 Layout Guidelines 21
11.2 Layout Example 21
12 Device and Documentation Support 22
12.1 接收文档更新通知 22
12.2 支持资源 22
12.3 Trademarks 22
12.4 静电放电警告 22
12.5 术语表 22
13 Mechanical, Packaging, and Orderable Information 22
13.1 Tape and Reel Information 23
13.2 Mechanical Data 25

4 Revision History

DATE	REVISION	NOTES
February 2022	*	Initial release.

5 Pin Configuration and Functions

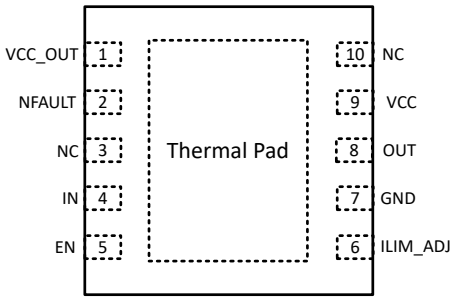


图 5-1. TIOS1023, TIOS1025
DRC, 10-Pin VSON
(Top View)

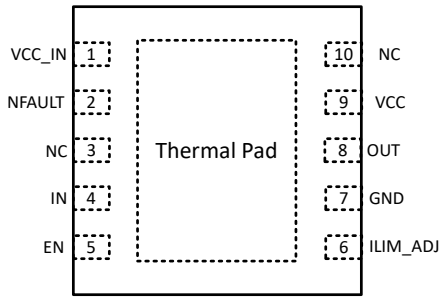


图 5-2. TIOS102
DRC, 10-Pin VSON
(Top View)

表 5-1. Pin Functions (VSON Package)

PIN NO	PIN NAME		Type	DESCRIPTION
	TIOS102	TIOS1023, TIOS1025		
1	VCC_IN	VCC_OUT	P	3.3-V or 5-V linear regulator output; external 3.3-V or 5-V logic supply input for option without LDO.
2	NFAULT	NFAULT	O	Fault indicator output signal to the microcontroller. Connect this pin via pull-up resistor to VCC_IN (TIOS102) or VCC_OUT (TIOS1023, TIOS1025)
3	NC	NC	-	Do not connect to GND. Leave floating
4	IN	IN	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
5	EN	EN	I	Driver enable input signal from the local controller. Logic low sets the OUT output at Hi-Z. Weak internal pull-down.
6	ILIM_ADJ	ILIM_ADJ	I	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and GND.
7	GND	GND	GND	Device ground connection
8	OUT	OUT	O	Driver output
9	VCC	VCC	P	Supply voltage (24 V nominal)
10	NC	NC	-	Do not connect to GND. Leave floating
	Thermal Pad	Thermal Pad	—	Connect to GND plane for optimal thermal and electrical performance

ADVANCE INFORMATION

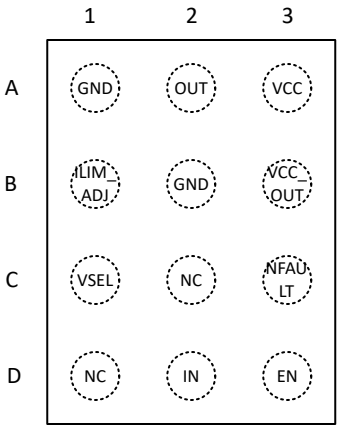


图 5-3. TIOS1023
YAH, 12-Pin DSBGA
(Top View)

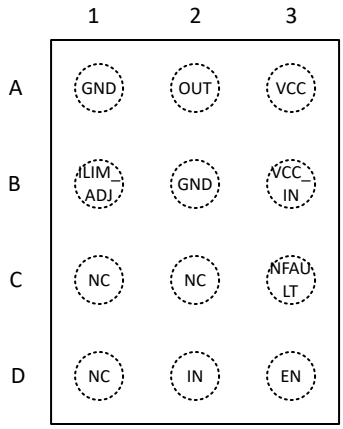


图 5-4. TIOS102
YAH, 12-Pin DSBGA
(Top View)

表 5-2. Pin Functions (DSBGA)

PIN NO	PIN NAME		Type	DESCRIPTION
	TIOS102	TIOS1023L		
B3	VCC_IN	VCC_OUT	P	3.3-V or 5-V linear regulator output; external 3.3-V or 5-V logic supply input for option without LDO.
C3	NFAULT	NFAULT	O	Fault indicator output signal to the microcontroller. Connect this pin via pull-up resistor to VCC_IN (TIOS102) or VCC_OUT (TIOS1023, TIOS1025)
D2	TX	TX	I	Transmit data input from the local controller. No effect if EN is low. Logic high sets low-side switch. Logic low sets high-side switch. Weak internal pull-up.
D3	EN	EN	I	Driver enable input signal from the local controller. Logic low sets the OUT output at Hi-Z. Weak internal pull-down.
B1	ILIM_ADJ	ILIM_ADJ	I	Input for current limit adjustment. Connect resistor R_{SET} between ILIM_ADJ and GND.
A1, B2	GND	GND	GND	Device ground connection
A2	OUT	OUT	O	Switch output
A3	VCC	VCC	P	Supply voltage (24 V nominal)
D1, C2	NC	NC	-	Leave floating. Do not connect.
C1	NC	VSEL	I	TIOS102: Leave floating. Do not connect TIOS1023L: VSEL: Connect to GND for 5V LDO output. Please leave this pin floating for 3.3V LDO output

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	Steady state voltage for VCC and OUT	–65	65	V
	Transient pulse width < 100 µs for VCC and OUT	–70	70	V
Voltage difference	$\lvert V_{(VCC)} - V_{(OUT)} \rvert$		65	V
Logic supply voltage (TIOS102)	VCC_IN	–0.3	6	V
Input logic voltage	IN, EN, VSEL	–0.3	min(VCC_IN +0.3, 6)	V
Output current	WAKE, NFAULT	–5	5	mA
Storage temperature, T_{stg}		-55	170	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute maximum ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime. All voltages are with reference to the GND pin, unless otherwise specified.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
$V_{(ESD)}$	Electrostatic discharge	Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	All pins	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Minimum 100-nF capacitor is required between VCC and GND. Minimum 1-µF capacitor is required between VCC_IN/OUT and GND.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 ESD (Contact Discharge), VCC, OUT and GND (1) (2)	±8,000	V
	Electrostatic discharge	IEC 61000-4-5, 1.2 µs/50 µs Surge with 500 Ω in series, VCC, OUT and GND (1)	±1,200	
	Electrostatic discharge	IEC 61000-4-4 EFT (Fast transient or burst), VCC, OUT and GND (1)	±4,000	

(1) Minimum 100-nF capacitor is required between VCC and GND. Minimum 1-µF capacitor is required between VCC_IN/VCC_OUT and GND.
(2) Passing level is ±4500 V if the device is powered and EN=IN=HIGH.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VCC)}$	Supply voltage	TIOS1023, TIOS102	5	24	36	V
		TIOS1025	7	24	36	V
$V_{(VCC\_IN)}$	Logic level input voltage (TIOS102 only)	3.3 V configuration	3	3.3	3.6	V
		5 V configuration	4.5	5	5.5	V
R_{SET}	External resistor for CQ current limit		0		110	kΩ
$1/t_{BIT}$	Data rate (Communication mode)				250	kbps
$I_{(VCC\_OUT)}$	LDO output current (TIOS1023, TIOS1025 only)				20	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Junction temperature				150	°C

ADVANCE INFORMATION

6.5 Thermal Information

THERMAL METRIC (1)		TIOS102, TIOS1023, TIOS1025	TIOS102, TIOS1023	UNIT
		DRC (10 Pins)	YAH (12 Pins)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.9	79.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.9	0.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.9	19.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	17.8	19.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typical values are at V_{VCC} = 24 V, V_{VCC_IN} = 3.3 V, V_{VCC_OUT} = 3.3 V and T_A = 25 ℃ unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES (VCC)							
$I_{(VCC)}$	Quiescent supply current	EN = LOW, no load			1.5	2.2	mA
		EN = HIGH, no load			2.2	2.95	mA
LOGIC-LEVEL INPUTS (EN, IN, VSEL)							
V_{IL}	Input logic low voltage					0.8	V
V_{IH}	Input logic high voltage			2			V
R_{PD}	Pull-down (EN) resistance				100		kΩ
R_{PU}	Pull-up (IN) resistance				200		kΩ
R_{PU}	Pull-up (VSEL) resistance				1000		kΩ
CONTROL OUTPUTS (NFAULT)							
V_{OL}	Output logic low voltage	I_O = 4 mA				0.5	V
I_{OZ}	Output high impedance leakage	Output in Hi-Z, V_O = 0 V or VCC_IN/OUT		–1		1	µA
DRIVER OUTPUT (OUT)							
$R_{DS(ON)}$	High-side driver on-resistance				2.5	4.5	Ω
$V_{DS(ON)}$	High-side driver residual voltage	I = 200 mA			0.5	0.9	V
		I = 100 mA			0.25	0.5	V
$R_{DS(ON)}$	Low-side driver on-resistance				2.5	4.5	Ω
$V_{DS(ON)}$	Low-side driver residual voltage	I = 200 mA			0.5	0.9	V
		I = 100 mA			0.25	0.5	V
I_P	OUT pull-up/down current	EN = LOW, IN = LOW, pull-down current	$0 \leqslant V_{(OUT)} \leqslant (V_{(VCC)} - 0.1)$ V	40	50	80	µA
I_P	OUT pull-up/down current	EN = LOW, IN = HIGH, pull-up current		40	50	80	µA
$I_{O(LIM)}$	Driver output current limit	R_{SET} = 10 kΩ; V(OUT) = ($V_{(VCC)}$-3) V or 3 V		300	350	400	mA
		R_{SET} = 110 kΩ; V(OUT) = ($V_{(VCC)}$-3) V or 3 V		35	50	70	mA
		R_{SET} = 0 to 5 kΩ; (2) V(OUT) = ($V_{(VCC)}$-3) V or 3 V $T_J < T_{(SDN)}$ or t < 200 µs		500			mA
		(Fast-detect mode) R_{SET} = OPEN(1) V(OUT) = ($V_{(VCC)}$-3) V or 3 V		260	330	400	mA

ADVANCE INFORMATION

6.6 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typical values are at V_{VCC} = 24 V, V_{VCC_IN} = 3.3 V, V_{VCC_OUT} = 3.3 V and T_A = 25 ℃ unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PROTECTION CIRCUITS							
$V_{(UVLO)}$	VCC under voltage lockout	VCC falling; NFAULT = Hi-Z	TIOS102, TIOS1023	4.2			V
$V_{(UVLO)}$	VCC under voltage lockout	VCC rising; NFAULT = Hi-Z				4.75	V
$V_{(UVLO)}$	VCC under voltage lockout	VCC falling; NFAULT = Hi-Z	TIOS1025	6	6.3		V
		VCC rising; NFAULT = Hi-Z			6.5	6.8	V
$V_{(UVLO,HYS)}$	VCC under voltage lockout hysteresis	Rising to falling threshold	Rising to falling threshold	200			mV
$V_{(UVLO\_IN)}$	VCC_IN under voltage lockout (No LDO option)	VCC_IN falling; NFAULT = Hi-Z			2.4		V
		VCC_IN rising; NFAULT = LOW			2.5		V
$V_{(UVLO\_IN,HYS)}$	VCC_IN under voltage hysteresis (No LDO option)	Rising to falling threshold			100		mV
$T_{(WRN)}$	Thermal warning	Die temperature T_J		125			°C
$T_{(SDN)}$	Thermal shutdown			150	160		°C
$T_{(HYS)}$	Thermal hysteresis for shutdown				14		°C
I_{REV}	Leakage current in reverse polarity	EN=LOW, TX=x; $V_{(OUT)} < V_{(GND)}$ or $V_{(OUT)} > V_{(VCC)}$, up to |36 V|				50	µA
		EN=LOW, TX=x; $V_{(OUT)} < V_{(GND)}$ or $V_{(OUT)} > V_{(VCC)}$, up to |55 V|				110	µA
		EN = HIGH, TX = LOW; $V_{(OUT\ to\ VCC)}$ = 3 V				550	µA
		EN = HIGH, TX = HIGH; $V_{(OUT\ to\ GND)}$ = -3 V				10	µA
LINEAR REGULATOR (LDO)							
$V_{(VCC\_OUT)}$	Voltage regulator output	TIOS1025		4.75	5	5.25	V
		TIOS1023		3.13	3.3	3.46	V
$V_{(DROP)}$	Voltage regulator drop-out voltage ($V_{(VCC)}$ – $V_{(VCC\_OUT)}$)	I_{CC} = 20 mA load current	TIOS1025			1.9	V
			TIOS1023			2.3	V
REG	Line regulation ($dV_{(VCC\_OUT)}$/ dV(VCC))	$I_{(VCC\_OUT)}$ = 1 mA				1.7	mV/V
L_{REG}	Load regulation ($dV_{(VCC\_OUT)}$/ $V_{(VCC\_OUT)}$)	$V_{(VCC)}$ = 24 V, $I_{(VCC\_OUT)}$ = 100 µA to 20 mA				1%	
PSSR	Power Supply Rejection Ratio	100 kHz, $I_{(VCC\_OUT)}$ = 20 mA			40		dB

(1) Current fault indication will be active. Current fault auto recovery will be de-activated.
(2) If operating continuously with this current limit, ensure that the current through the device does not cause the T_J to be greater than $T_{(SDN)}$ for a given ambient temperature and thermal property of the system. For pulse durations t < 200 µs, the device can source or sink current of at least 500 mA across the recommended operating conditions.

ADVANCE INFORMATION

6.7 Switching Characteristics

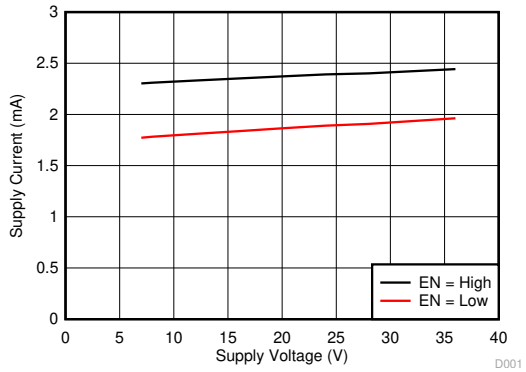
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER						
t_{PLH}, t_{PHL}	Driver propagation delay	See 图 7-3 R_L = 2 kΩ C_L = 5 nF $R_{(SET)}$ = 10 kΩ		600	1200	ns
$t_{P(skew)}$	Driver propagation delay skew. | t_{PLH} - t_{PHL} |			100		ns
t_{PZH}, t_{PZL}	Driver enable delay				4	µs
t_{PHZ}, t_{PLZ}	Driver disable delay				4	µs
t_r, t_f	Driver output rise, fall time		200		700	ns
$\|t_r - t_f\|$	Difference in rise and fall time				50	ns
t_{SC}	Current fault blanking time		175	200		µs
t_{pSC}	Current fault indication delay				280	µs
t_{SCEN}	Current fault driver re-enable wait time			15		ms
$t_{(UVLO)}$	OUT re-enable delay after UVLO (1)	$V_{(UVLO)}$ rising threshold crossing time to CQ enable time	10	30	50	ms

(1) CQ output remains Hi-Z for this time

ADVANCE INFORMATION

6.8 Typical Characteristics



No load IN = OPEN T_A = 25°C

图 6-1. Supply Current vs Supply Voltage

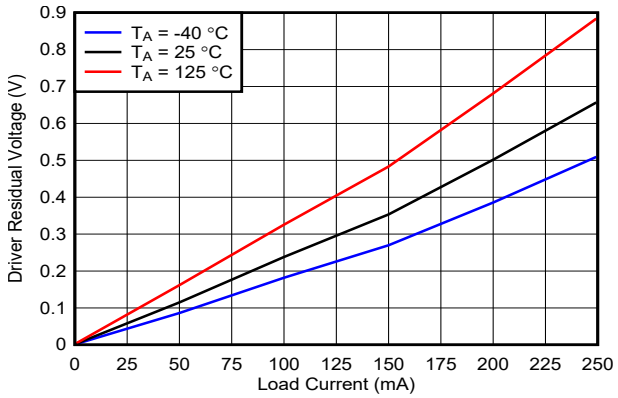


图 6-2. Residual Voltage vs Load Current: High Side

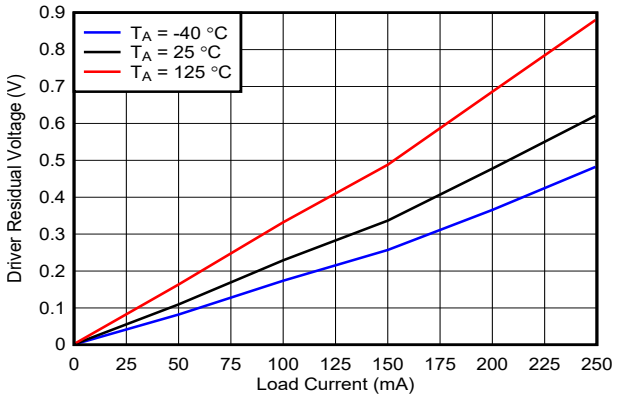


图 6-3. Residual Voltage vs Load Current: Low Side

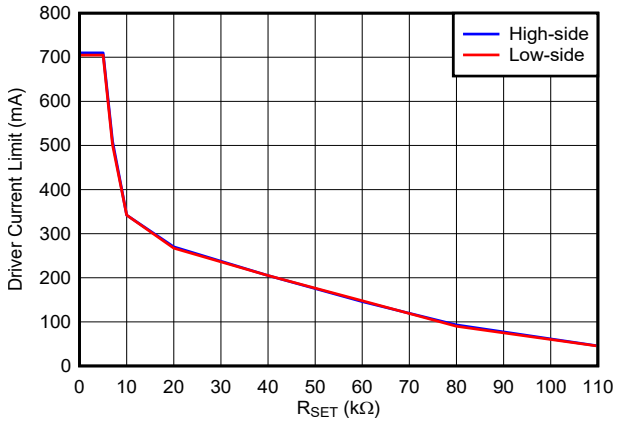
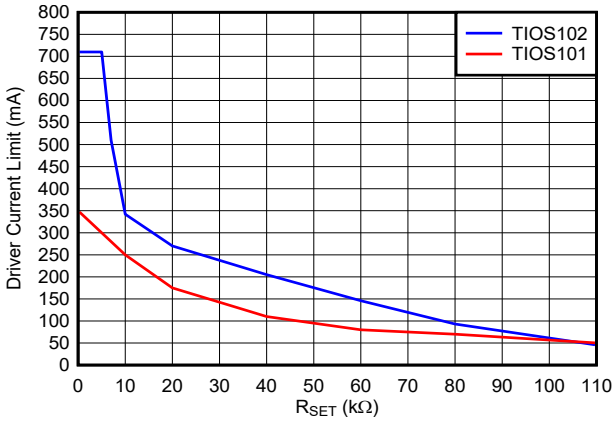


图 6-4. Current Limit vs R_{SET}



T_A = 25°C

图 6-5. Current Limit vs R_{SET} : TIOS102(x) vs TIOS101(x)

ADVANCE INFORMATION

7 Parameter Measurement Information

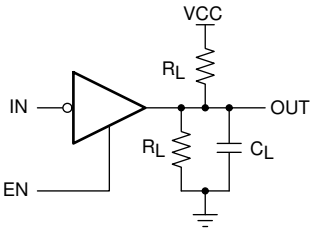


图 7-1. Test Circuit for Driver Switching

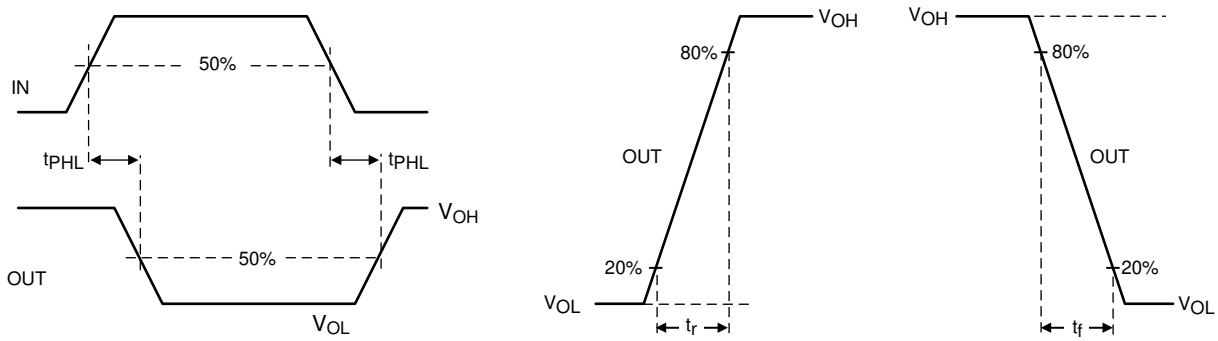


图 7-2. Waveforms for Driver Output Switching Measurements

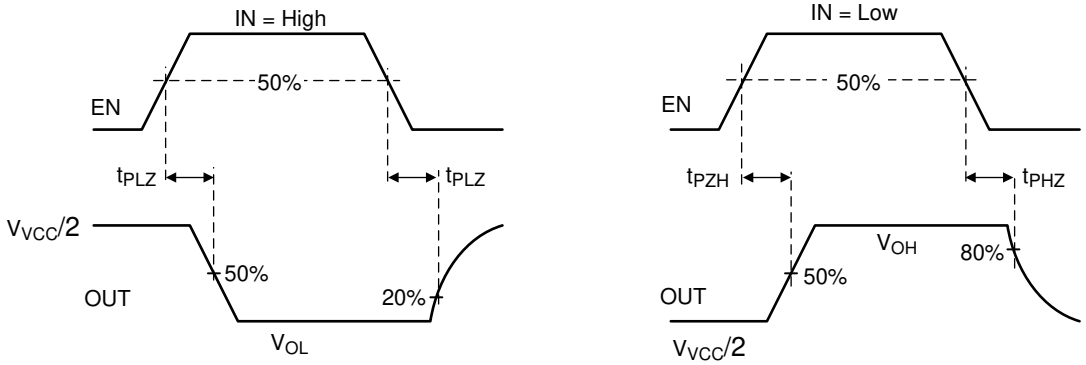


图 7-3. Waveforms for Driver Enable or Disable Time Measurements

8 Detailed Description

8.1 Overview

图 8-1 shows that the device driver output (OUT) can be used in a push-pull, high-side, or low-side configuration using the enable (EN) and transmit data (IN) input pins. OUT can drive resistive, large capacitive or large inductive loads.

TIOS102 and TIOS102x devices have integrated IEC 61000-4-4/5 EFT and surge protection. In addition, tolerance to ±65-V transients enables flexibility to choose from a wider range of TVS diodes if an application requires higher levels of protection. These integrated robustness features will simplify the system-level design by reducing the external protection circuitry.

These devices implement protection features for over-current, over-voltage and over-temperature conditions. The devices also provide a current-limit setting of the driver output current using an external resistor.

The TIOS102x devices derive the low voltage supply from the typical 24 V industrial supply via an internal linear regulator to provide power to the local controller and sensor circuitry.

8.2 Functional Block Diagrams

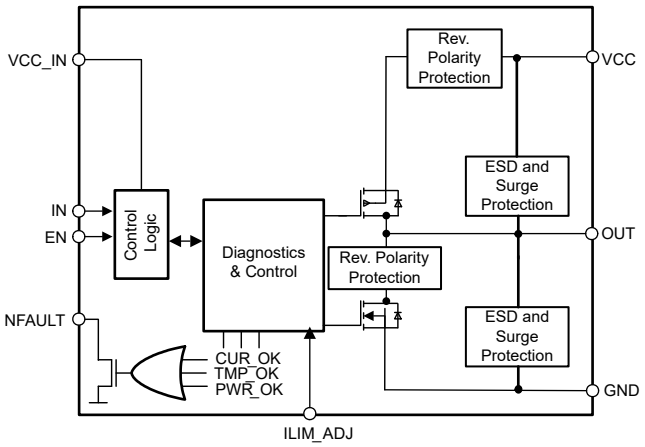


图 8-1. Block Diagram, TIOS102

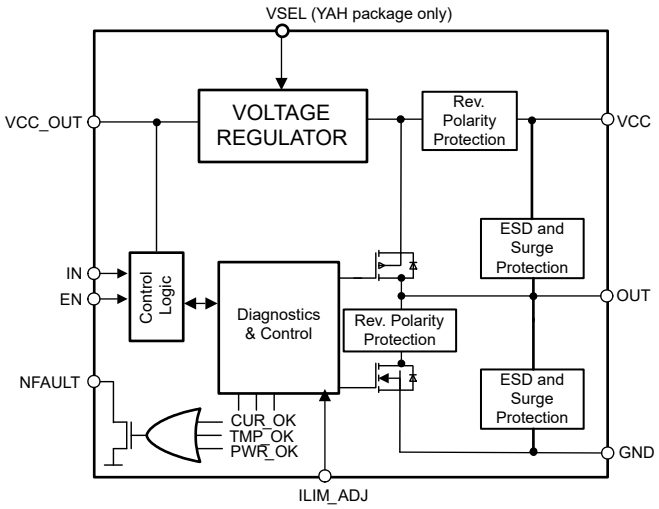


图 8-2. Block Diagram, TIOS102x

ADVANCE INFORMATION

ADVANCE INFORMATION

8.3 Feature Description

8.3.1 Current Limit Configuration

The output current can be configured with an external resistor on ILIM_ADJ pin. The highest current limit setting with an external resistor of 10 kΩ guarantees a minimum of 300 mA over the operating temperature and voltage range.

Output disable due to current fault and current fault auto recovery features can be disabled by floating ILIM_ADJ pin. However, the current fault indication is still active in this configuration. This feature is useful when driving large capacitances.

When ILIM_ADJ pin is shorted to ground, the TIOS102(x) is configured to source or sink minimum of 500mA. In this mode, current fault indication is disabled. Output Disable and Auto Recovery feature is also disabled in this mode. The driver will be disabled if the power dissipation in the device causes the junction temperature to reach $T_{(SDN)}$.

表 8-1. Current Limitation

ILIM_ADJ Pin Condition	OUT Current Limit (Min.)	NFAULT Indication During Fault	Output Disable and Auto Recovery
R_{SET} resistor to GND (R_{SET}: 10 kΩ to 110 kΩ)	Variable (35 mA to 300 mA)	Yes	Yes
Connected to GND (R_{SET} 0 to 5 kΩ)	500 mA	No	No
OPEN	260 mA	Yes	No

8.3.2 Current Fault Detection, Indication and Auto Recovery

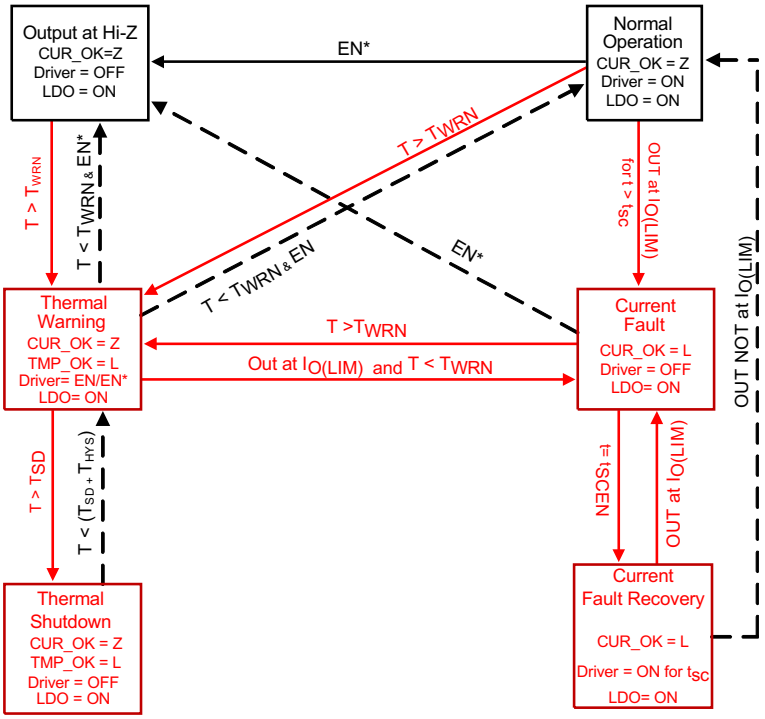
If the output current at OUT exceeds the internally set current limit $I_{O(LIM)}$ for a duration longer than t_{SC}, the NFAULT pin is driven logic low to indicate a fault condition. The output is turned off, but the LDO continues to function. The output periodically retries to check if the output is still in the over current condition. In this mode, the output is switched on for t_{SC} in t_{SCEN} intervals. Current fault auto recovery mode can be disabled by setting ILIM_ADJ = OPEN or GND. See 表 8-3. Toggling EN will clear NFAULT.

8.3.3 Thermal Warning, Thermal Shutdown

If the die temperature exceeds $T_{(WRN)}$, the NFAULT flag is held low indicating a potential over temperature problem. When the T_J exceeds $T_{(SDN)}$, The output is disabled but the LDO remains operational. As soon as the temperature drops below the temperature threshold (and after $T_{(HYS)}$), the internal circuit re-enables the driver, subject to the state of the EN and IN pins.

8.3.4 Fault Reporting (NFAULT)

NFAULT is driven low if either a current fault condition is detected, die temperature has exceeded $T_{(WRN)}$ or supply has dropped below the UVLO threshold. NFAULT returns to high-impedance as soon as all three fault conditions clear.



NFAULT = [CUR_OK && PWR_OK && TMP_OK]

图 8-3. Device State Diagram

ADVANCE INFORMATION

8.3.5 Device Function Tables

表 8-2. Driver Function

EN	IN	OUT	COMMENT
L / Open	X	Hi-Z	Device is in ready-to-receive state
H	L	H	OUT is sourcing current (high-side drive)
H	H / Open	L	OUT is sinking current (low-side drive)

表 8-3. Current Limit Indicator Function ($t > t_{SC}$)

EN	IN	OUT CURRENT	NFAULT	COMMENT
H	H / Open	$\lvert I_{(OUT)} \rvert > I_{O(LIM)}$	L	OUT current exceeds the set limit for over t_{SC}
		$\lvert I_{(OUT)} \rvert < I_{O(LIM)}$	Z	Normal operation
H	L	$\lvert I_{(OUT)} \rvert > I_{O(LIM)}$	L	OUT current exceeds the set limit for over t_{SC}
		$\lvert I_{(OUT)} \rvert < I_{O(LIM)}$	Z	Normal operation
L / Open	X	X	Z	Driver is disabled, current limit indicator is inactive

8.3.6 The Integrated Voltage Regulator (LDO)

The TIOS1023 and TIOS1025 each have an integrated linear voltage regulator (LDO) which can supply power to external components. The voltage regulator is specified for VCC voltages in the range of 7 V to 36 V (TIOS1025) or in the range of 5 V to 36 V (TIOS102, TIOS1023) with respect to GND. The LDO is capable of delivering up to 20 mA. The LDO output is current limited to 35-mA to limit the inrush current onto VCC_OUT decoupling capacitors during initial power up.

In the DSBGA (YAH) package, TIOS1023 offers pin-configurable LDO output via VSEL pin. When VSEL is connected to GND, VCC_OUT is configured to provide a 5-V output. When VSEL is left floating, VCC_OUT provides a 3.3-V output.

表 8-4. LDO Output Configuration via VSEL pin (YAH Package)

VSEL pin connection	VCC_OUT
GND	5 V
Floating	3.3 V

The LDO is designed to be stable with standard ceramic capacitors with values of 1 μF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 1 Ω. With tolerance and dc bias effects, the minimum capacitance to ensure stability is 1 μF.

ADVANCE INFORMATION

8.3.7 Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the VCC, OUT and GND pins. The maximum voltage between any of the pins may not exceed 65 V DC at any time.

图 8-4 and 图 8-5 shows all the possible connection combinations.

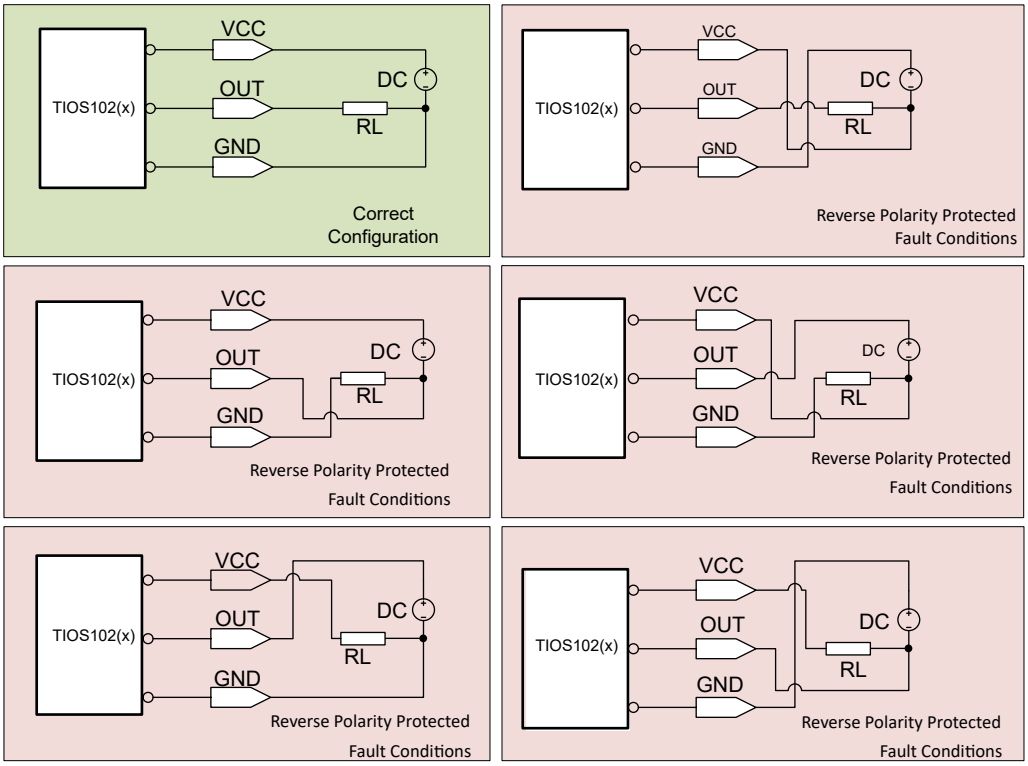


图 8-4. High-Side Driver Configuration

ADVANCE INFORMATION

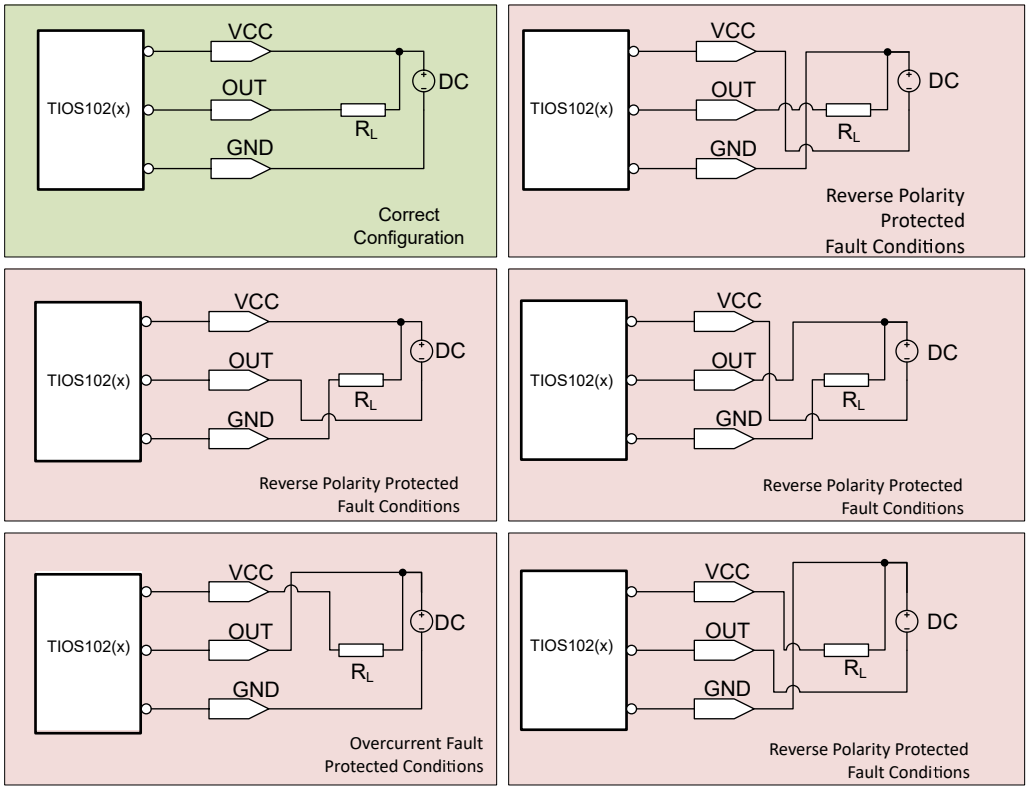
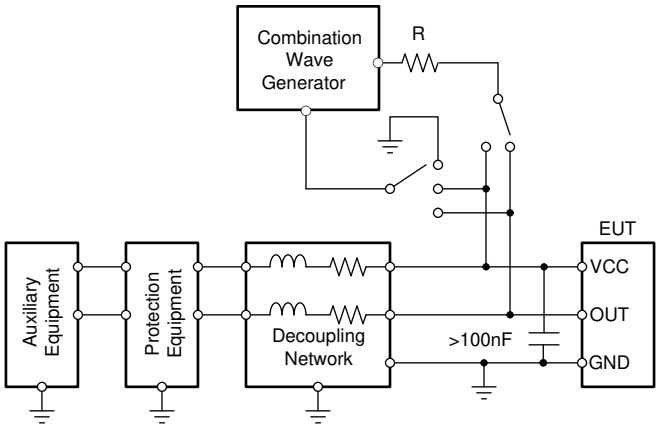


图 8-5. Low-Side Driver Configuration

8.3.8 Integrated Surge Protection and Transient Waveform Tolerance

The VCC and OUT pins of the device are capable of withstanding up to 1.2 kV of 1.2/50 – 8/20 μs IEC 61000-4-5 surge with a source impedance of 500 Ω. The surge testing should be performed with a minimum 100 nF supply decoupling capacitor between VCC and GND, and 1 μF between VCC_IN/OUT and GND.

External TVS diodes may be required for higher transient protection levels. The system designer should ensure that the maximum clamping voltage of the external diodes should be < 65 V at the desired current level. The device is capable of withstanding up to ±65-V transient pulses < 100 μs.



1.2/50 - 80/20 μs CWG
R = 500 Ω

图 8-6. Surge Test Setup

8.3.9 Power Up Sequence

VCC_IN and VCC domains can be powered up in any sequence. In the event of VCC is powered and VCC_IN is not, the OUT pin remains in high impedance.

8.3.10 Undervoltage Lock-Out (UVLO)

The device enters UVLO if the VCC voltage falls below $V_{(UVLO)}$. (For the device without the integrated LDO, the device monitors VCC_IN in addition to VCC. UVLO happens if either supply falls below the threshold.)

As soon as the supply falls below $V_{(UVLO)}$, NFAULT is pulled low, the LDO is turned off and the OUT output is disabled (Hi-Z). Receiver performance is not specified in this mode.

When the supply rises above $V_{(UVLO)}$, NFAULT returns to Hi-Z (given no other fault conditions present) and the LDO will be enabled immediately. The OUT output will be turned on after $T_{(UVLO)}$ delay.

8.4 Device Functional Modes

These devices can operate in three different modes.

8.4.1 NPN Configuration (N-Switch Mode)

Set IN pin high (or open) and use EN pin as control for realizing the function of an N-switch (low-side configuration) on OUT.

8.4.2 PNP Configuration (P-Switch Mode)

Set IN pin low and use EN pin as control for realizing the function of a P-switch (high-side configuration) on OUT.

8.4.3 Push-Pull Mode

Set EN pin high and toggle IN as control for realizing the function of a push-pull output on OUT. 表 8-5, 表 8-6, and 表 8-7 summarize the pin configurations to accomplish the functional modes.

ADVANCE INFORMATION

表 8-5. NPN Mode

EN	IN	OUT
L / Open	H / Open	Hi-Z
H	H / Open	N-Switch

表 8-6. PNP Mode

EN	IN	OUT
L / Open	L	Hi-Z
H	L	P-Switch

表 8-7. Push-Pull Mode

EN	IN	OUT
L / Open	X	Hi-Z
H	H / Open	N-Switch
H	L	P-Switch

9 Application Information Disclaimer

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

TIOS102 and TIOS102x are robust 24-V digital drivers for industrial sensors.

9.2 Typical Application

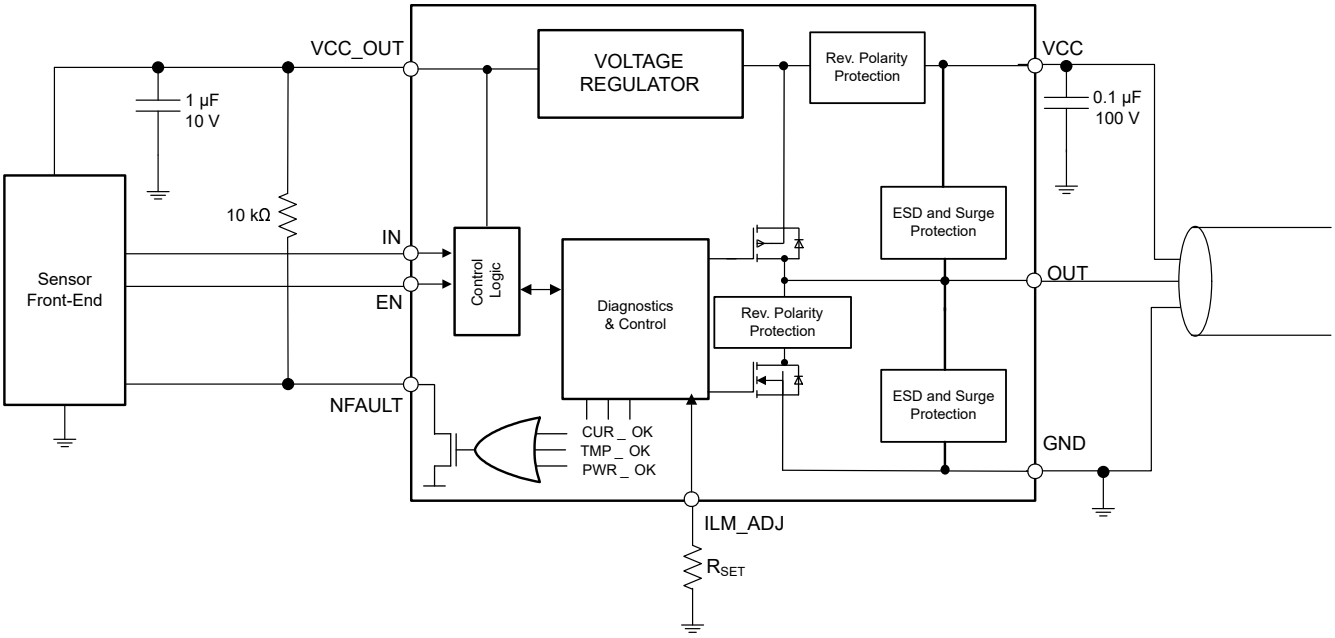


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

表 9-1 shows recommended components for a typical system design.

表 9-1. Design Parameters

PARAMETERS	Design Requirement	TIOS102(x) Specification
Input voltage range (VCC)	24 V, 30 V (max)	7 V to 36 V (TIOS1025)
Output current (OUT)	200 mA	Choose 250 mA limit with R_{SET} = 27 kΩ
Output voltage (VCC_OUT), Pick TIOS1025	5 V	Choose TIOS1025; VCC_OUT = 5 V
Maximum LDO output current ($I_{VCC(OUT)}$)	5 mA	I_{VCC_OUT}: Up to 20 mA
Pull-up resistors for NFAULT	10 kΩ	10 kΩ
VCC decoupling capacitor	0.1 µF / 100 V	0.1 µF / 100 V
LDO output capacitor	1 µF / 10 V	1 µF / 10 V
Maximum Ambient Temperature, T_A	105°C	TIOS102(x) can support up to T_A of 125 °C if $T_J < T_{(SDN)}$

ADVANCE INFORMATION

9.2.2 Detailed Design Procedure

9.2.2.1 Maximum Junction Temperature Check

For a 200 mA current limit:

- Choose driver output current limit, $I_{O(LIM)}$ = 250 mA (allowing for current limit tolerance); R_{SET} = 27 kΩ
- The maximum voltage drop across the high-side switch at 250 mA current is $V_{DS(ON)}$ = 1.1 V.

This causes a power consumption of:

$$PD_{OP} = V_{DS(ON)} \times I_{O(LIM)} = 1.1\,V \times 250\,mA = 275\,mW \quad (1)$$

For a 5 mA LDO current output,

$$PD_{LDO} = \left(V_{L+} - V_{VCC_{OUT}}\right) \times I_{VCC\_OUT} = (30 - 5)V \times 5\,mA = 125\,mW \quad (2)$$

Total power dissipation,

$$PD = PD_{LDO} + PD_{OP} = 275\,mW + 125\,mW = 400\,mW \quad (3)$$

Multiply this value with the Junction-to-ambient thermal resistance of θ_{JA} = 45.9 °C/W (taken from the *Thermal Information* table) to receive the difference between junction temperature, T_J, and ambient temperature, T_A:

$$\Delta T = T_J - T_A = PD \times \theta_{JA} = 400\,mW \times 45.9\,^{\circ}C/W = 18.36\,^{\circ}C \quad (4)$$

Add this value to the maximum ambient temperature of T_A = 105°C to receive the final junction temperature:

$$T_J = T_A + \Delta T = T_A + PD \times \theta_{JA} = 105\,^{\circ}C + 400\,mW \times 45.9\,^{\circ}C/W = 105\,^{\circ}C + 18.36\,^{\circ}C = 123.36\,^{\circ}C \quad (5)$$

As long as T_J is below the recommended maximum value of 150°C, no thermal shutdown will occur. However, the junction temperature is closer to T_{WRN} and thermal warning may be generated if the junction temperature rises above T_{WRN}.

Note that the modeling of the complete system may be necessary to predict junction temperature in smaller PCBs and/or enclosures without air flow.

10 Power Supply Recommendations

The TIOS102 and TIOS102x are designed to operate from a 24-V nominal supply at VCC, which can vary by +12 V and -17 V from the nominal value to remain within the device's recommended supply voltage range of 7 V to 36 V. This supply should be buffered with at least a 100-nF/100-V capacitor.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

- Use of a 4-layer board is recommended for good heat conduction. Use layer 1 (top layer) for control signals, layer 2 as GND, layer 3 for the 24-V supply plane (VCC), and layer 4 for the regulated output supply (VCC_IN/OUT).
- Connect the thermal pad to GND with maximum amount of thermal vias for best thermal performance.
- Use entire planes for VCC, VCC_IN/OUT and GND to assure minimum inductance.
- The VCC terminal must be decoupled to ground with a low-ESR ceramic decoupling capacitor with a minimum value of 100 nF. The capacitor must have a voltage rating of 50 V minimum (100 V depending on max sensor supply fault rating) and an X5R or X7R dielectric.
- • The optimum placement of the capacitor is closest to the VCC and GND terminals to reduce supply drops during large supply current loads. See 图 11-1 for a PCB layout example.
- Connect all open-drain control outputs via 10 kΩ pull-up resistors to the VCC_IN/OUT plane to provide a defined voltage potential to the system controller inputs when the outputs are high-impedance.
- Connect the R_{SET} resistor between ILIM_ADJ and GND.
- Decouple the regulated output voltage at VCC_IN/OUT to ground with a low-ESR, 1 µF, ceramic decoupling capacitor. The capacitor should have a voltage rating of 10 V minimum and an X5R or X7R dielectric.

11.2 Layout Example

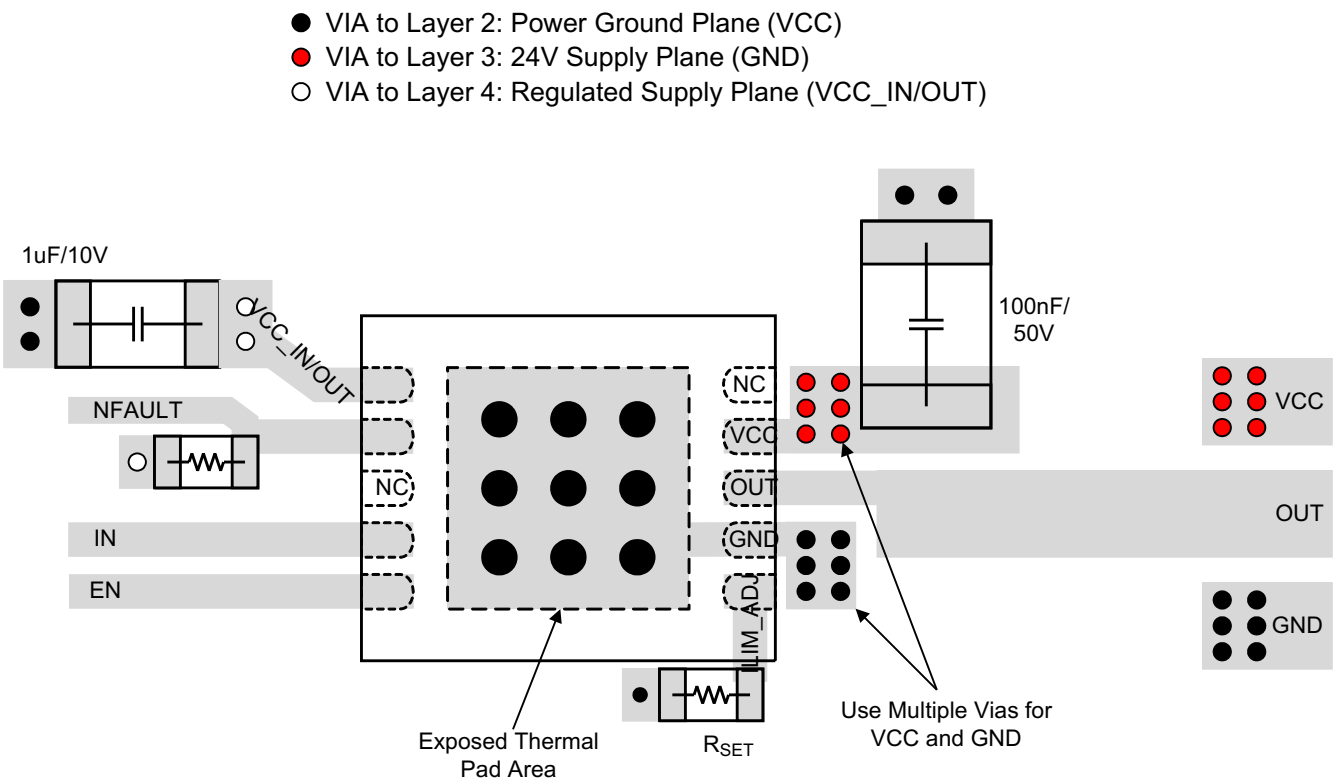


图 11-1. Layout Example

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

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所有商标均为其各自所有者的财产。

12.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

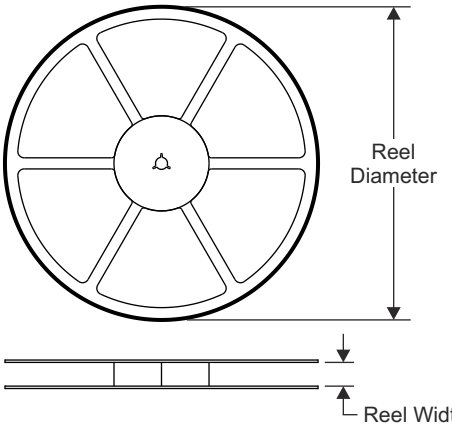
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

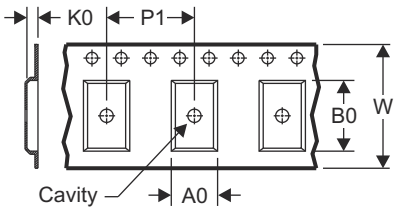
ADVANCE INFORMATION

13.1 Tape and Reel Information

REEL DIMENSIONS

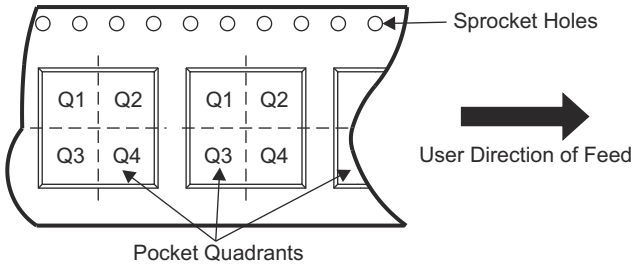


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

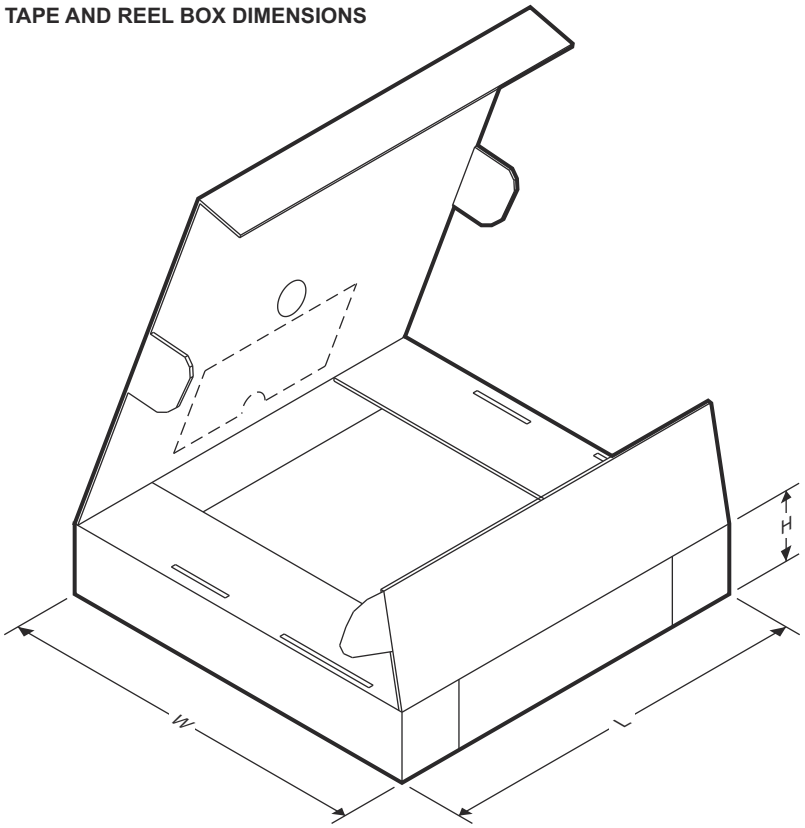


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTIOS102DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PTIOS102YAHR	DSBGA	YAH	12	1500	330.0	12.4	1.88	2.76	0.55	4.0	12.0	Q1
PTIOS1023DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
PTIOS1023LYAHR	DSBGA	YAH	12	1500	330.0	12.4	1.88	2.76	0.55	4.0	12.0	Q1
PTIOS1025DRCR	VSON	DRC	10	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTIOS102DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
PTIOS102YAHR	DSBGA	YAH	12				
PTIOS1023DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
PTIOS1023LYAHR	DSBGA	YAH	12				
PTIOS1025DRCR	VSON	DRC	10	3000	367.0	367.0	35.0

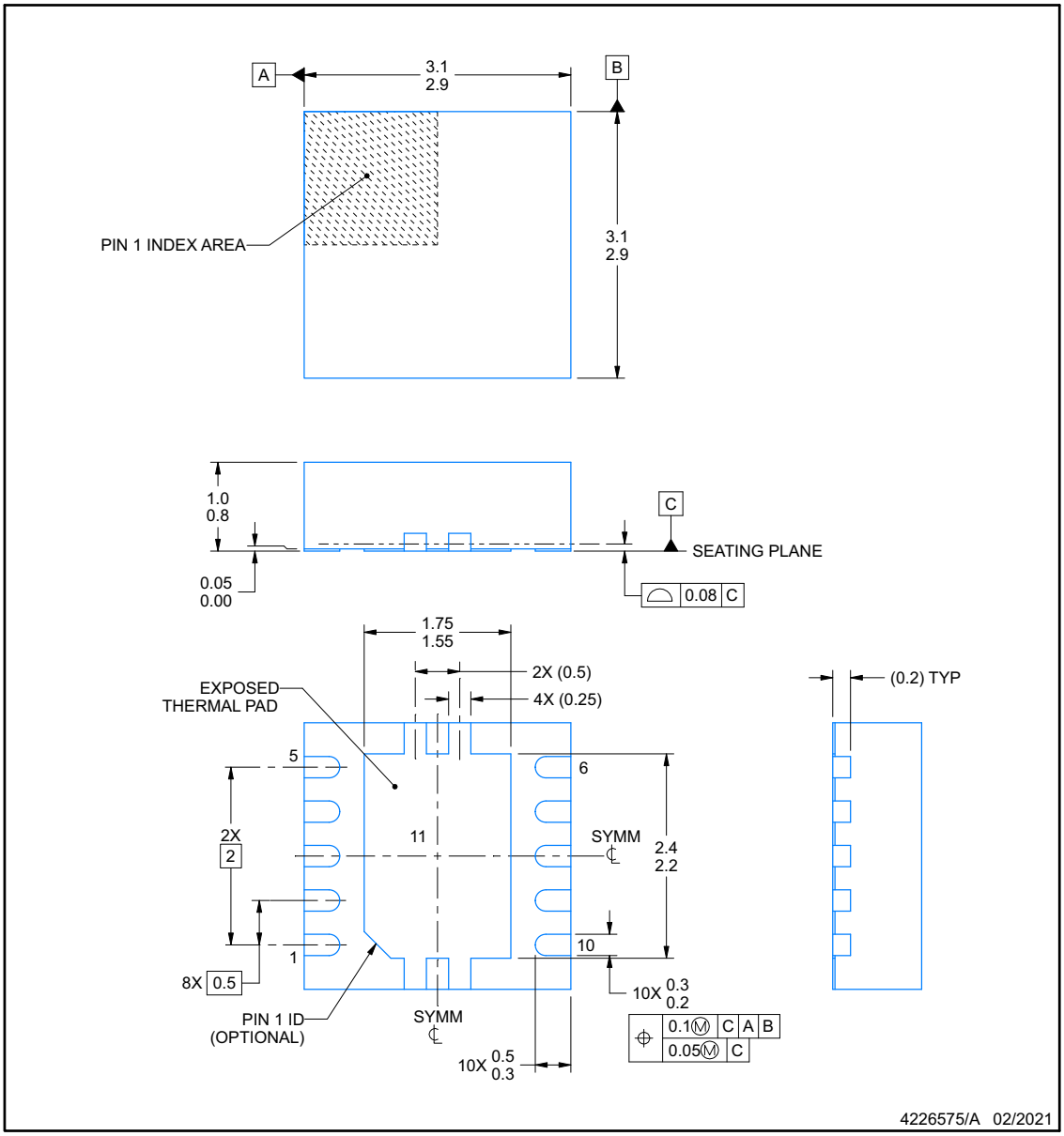
13.2 Mechanical Data

DRC0010V

PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

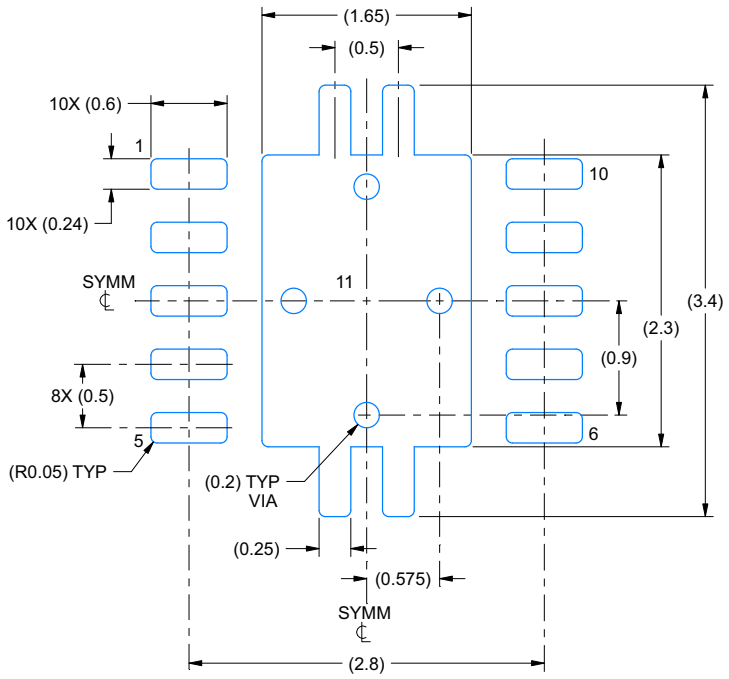
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

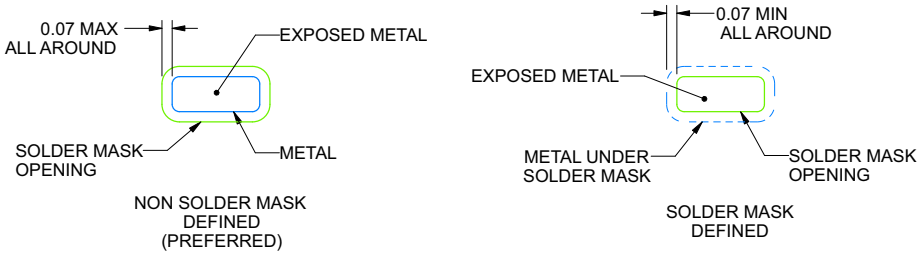
DRC0010V

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4226575/A 02/2021

NOTES: (continued)

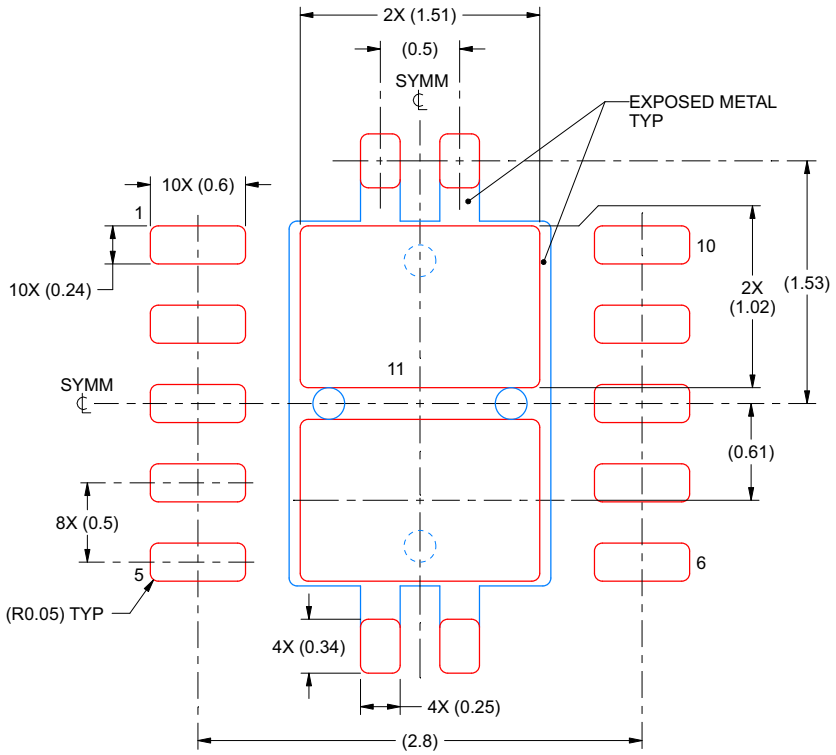
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010V

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

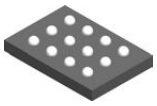
4226575/A 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

ADVANCE INFORMATION

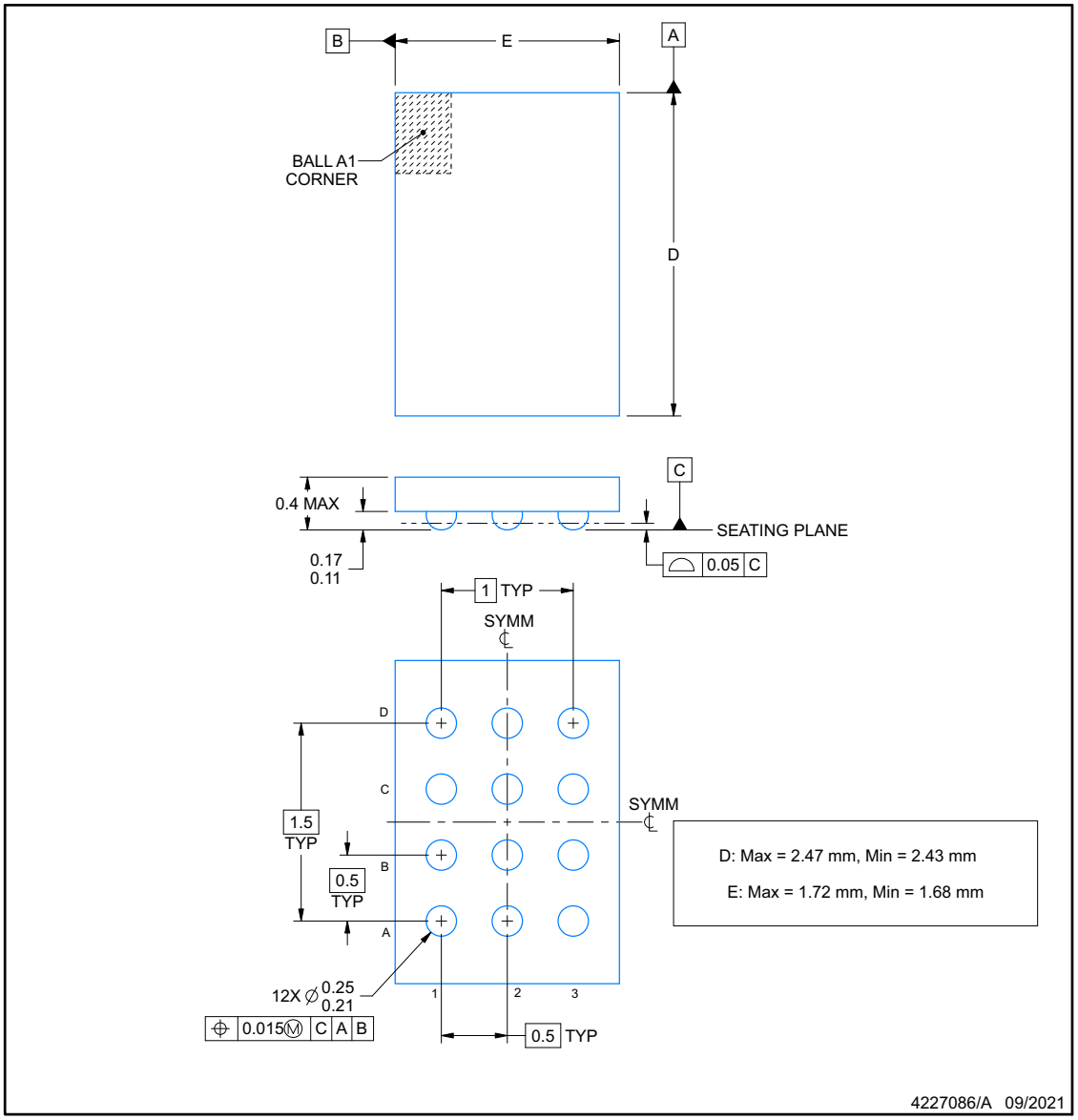


PACKAGE OUTLINE

YAH0012-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

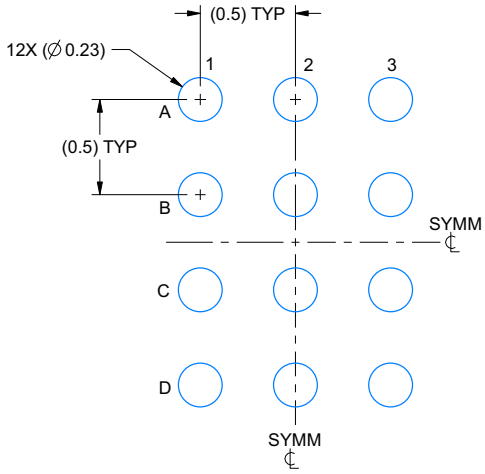
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

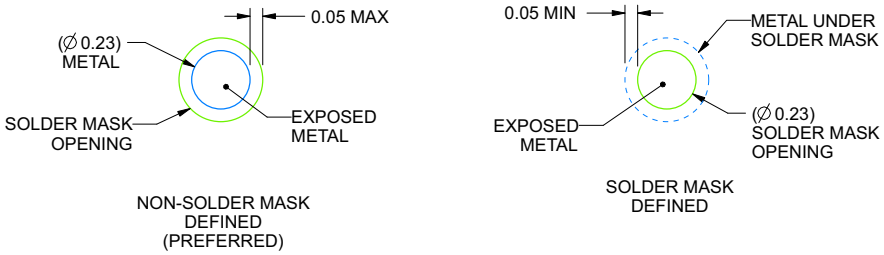
YAH0012-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS
NOT TO SCALE

4227086/A 09/2021

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

ADVANCE INFORMATION

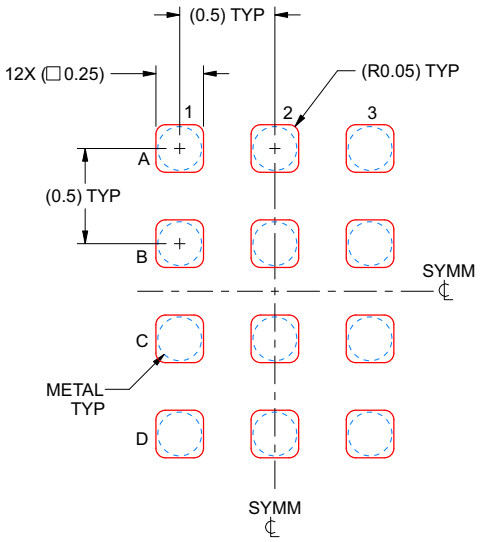
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

YAH0012-C01

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 30X

4227086/A 09/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTIOS1023DRCR	ACTIVE	VSON	DRC	10	5000	TBD	Call TI	Call TI	-40 to 125		Samples
PTIOS1025DRCR	ACTIVE	VSON	DRC	10	5000	TBD	Call TI	Call TI	-40 to 125		Samples
PTIOS102DRCR	ACTIVE	VSON	DRC	10	5000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

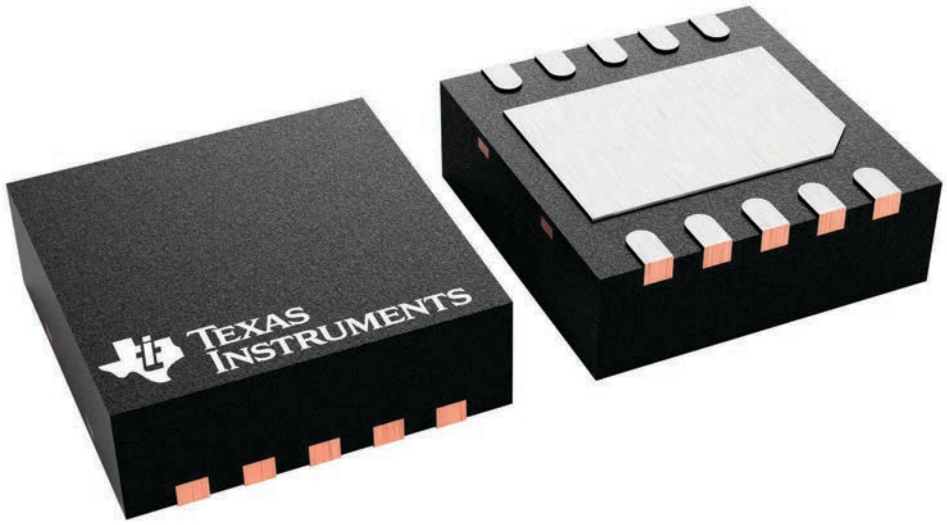
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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