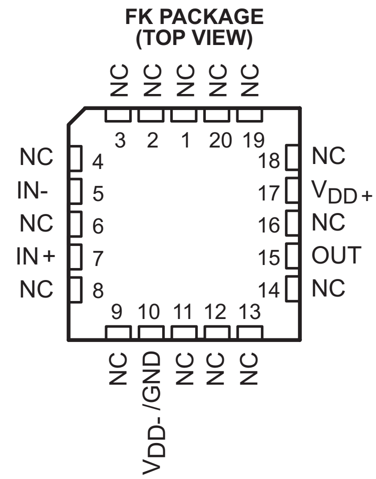
ClassV、先进 LinCMOS™ 工艺、低噪声精密运算放大器

查询样品: **TLC2201-SP**

特性

- 符合 **QML-V** 标准要求的 **SMD5962-9088203V2A**
- 低输入失调电压： **400μV** （最大值）
- 在整个温度范围内提供了出色的失调电压稳定性：**0.05μV/**℃ （典型值）
- 轨至轨输出摆幅
- 低输入偏置电流： 在 **T_A = 25**℃ 时的典型值为 **1pA**
- 共模输入电压范围包括负电源轨
- 技术规格针对单电源及分离电源操作全面拟订



NC - No internal connection

说明

TLC2201 是一款精密、低噪声运算放大器，运用了 TI 先进的 LinCMOS™ 制造工艺。 该器件将极低噪声 JFET 放大器的噪声性能与以往仅双极型放大器可提供的直流 (dc) 精度完美地组合在了一起。 Advanced LinCMOS™工艺采用硅栅技术来获得远远超过采用金属栅技术所能获得的随温度和时间变化的输入失调电压稳定性。 此外，这项工艺技术还可实现达到或超过顶栅 JFET 和昂贵的介质隔离器件所提供的输入阻抗位准 (impedance level)。

由于兼具卓越的直流和噪声性能以及一个包括负电源轨的共模输入范围，因而使得这些器件非常适合于单电源或分离电源配置中的高阻抗、低电平信号调节应用。

器件输入和输出专为承受－100mA 的浪涌电流而设计，而不会发生持续闭锁的现象。 此外，依据 MIL-PRF-38535、Method 3015.2 所进行的测试还证实：该器件的内部 ESD 保护电路可防止在高达 2000V 的电压条件下出现功能故障；不过，在使用这些器件时应谨慎从事，因为遭受 ESD 有可能导致参数性能的下降。

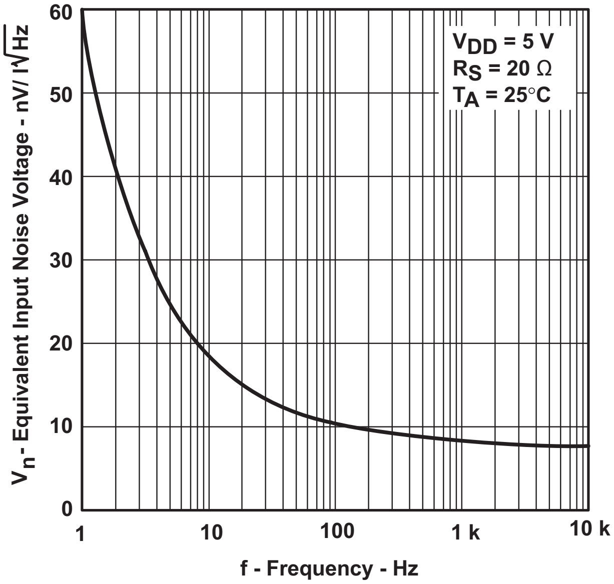
TLC2201 针对完整军用温度范围内 （－40℃ 至 125℃ ）的运作进行了特性分析。

English Data Sheet: SLOS710

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

TYPICAL EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

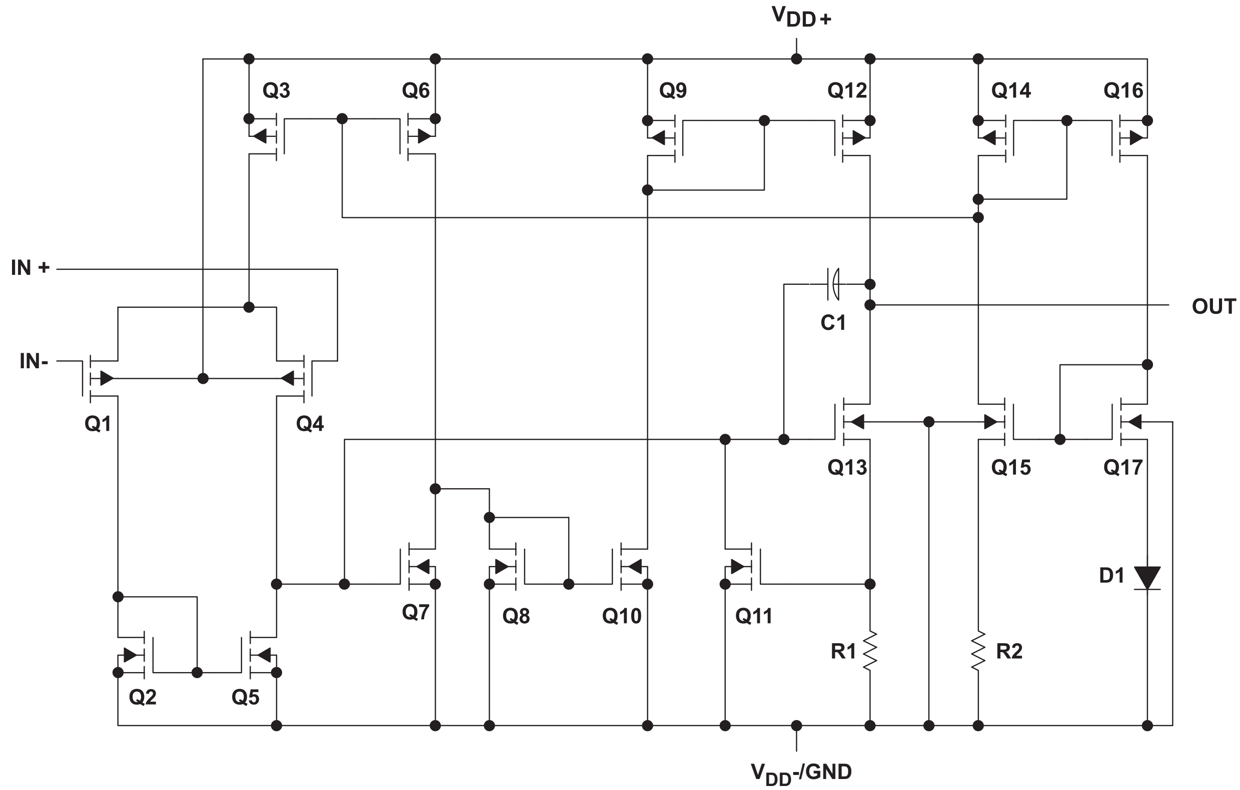


ORDERING INFORMATION(1)

TEMPERATURE	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C T_{case}	20-pin FK	5962-9088203V2A	5962-9088203V2A TLC2201AMFKBQMLV

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

EQUIVALENT SCHEMATIC



ACTUAL DEVICE COMPONENT COUNT	
COMPONENT	**TLC2201**
Transistors	17
Resistors	2
Diodes	1
Capacitors	1

ABSOLUTE MAXIMUM RATINGS[(1)]

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
V_{DD}	Supply voltage[(2)], V_{DD-} to V_{DD+}	-8 to 8	V
V_{ID}	Differential input voltage[(3)]	±16	V
V_I	Input voltage (any input)	±8	V
I_I	Input current (each input)	±5	mA
I_O	Output current (each output)	±50	mA
	Duration of short-circuit current at (or below) 25°C[(4)]	Unlimited	
	Continuous total power dissipation	See Dissipation Ratings Table	
T_C	Operating case temperature	–55 to 125	°C
T_{stg}	Storage temperature	–65 to 150	°C
	Case temperature for 60 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential voltages are with respect to the midpoint between $_{VDD+}$ and V_{DD-}.
(3) Differential voltages are at IN+ with respect to IN−.
(4) The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating in not exceeded.

THERMAL RESISTANCE FOR FK PACKAGE[(1)(2)]

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 test method 1012			16	°C/W

(1) Maximum power dissipation is a function of T_J (max), θ_{JC} and T_C. The maximum allowable power dissipation at any allowable case temperature is PD = (T_J (max) - T_C)/θ_{JC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
(2) The package thermal impedance is calculated in accordance with MIL-STD-883.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
$V_{DD\pm}$	Supply voltage	±2.3	±8	V
V_{IC}	Common-mode input voltage	V_{DD-}	V_{DD+}-2.3	V
T_C	Operating case temperature	–55	125	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200	µV
			Full range			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		µV/°C
	Input offset voltage long-term drift (2)		25°C		0.001		µV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	0 to 2.7			V
V_{OH}	Maximum high-level output voltage	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OL}	Maximum low-level output voltage	I_O = 0	25°C		0	50	mV
			Full range			50	
A_{VD}	Large-signal differential voltage amplification	V_O = 1 V to 4 V, R_L = 500 kΩ	25°C	150	315		V/mV
			Full range	75			
		V_O = 1 V to 4 V, R_L = 10 kΩ	25°C	25	55		
			Full range	10			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	90	110		dB
			Full range	85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = 4.6 V to 16 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		1.1	1.5	mA
			Full range			1.5	
SR	Slew rate at unity gain	V_O = 0.5 V to 2.5 V, R_L = 10 kΩ, C_L = 100 pF	25°C	1.8	2.5		V/µs
			Full range	1.1			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{n(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		µV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, RL = 10 kΩ, CL = 100 pF	25°C		1.8		MHz
φ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		45°		

(1) Full range is −55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observable through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{DD} = ±5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A (1)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{IC} = 0, R_S = 50 Ω	25°C		80	200	μV
			Full range			400	
α_{VIO}	Temperature coefficient of input offset voltage		Full range		0.5		μV/°C
	Input offset voltage long-term drift (2)		25°C		0.001		μV/mo
I_{IO}	Input offset current		25°C		0.5		pA
			Full range			500	
I_{IB}	Input bias current		25°C		1		pA
			Full range			500	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω	Full range	-5 to 2.7			V
V_{OM+}	Maximum positive peak output voltage swing	R_L = 10 kΩ	25°C	4.7	4.8		V
			Full range	4.7			
V_{OM-}	Maximum negative peak output voltage swing		25°C	-4.7	-4.9		V
			Full range	-4.7			
A_{VD}	Large-signal differential voltage amplification	V_O = ±4 V, R_L = 500 kΩ	25°C	400	560		V/mV
			Full range	200			
		V_O = ±4 V, R_L = 10 kΩ	25°C	90	100		
			Full range	45			
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR}min, V_O = 0, R_S = 50 Ω	25°C	90	115		dB
			Full range	85			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	V_{DD} = ±2.3 V to ±8 V	25°C	90	110		dB
			Full range	85			
I_{DD}	Supply current	V_O = 0 V, No load	25°C		1.1	1.5	mA
			Full range			1.5	
SR	Slew rate at unity gain	V_O = ±2.3 V, R_L = 10 kΩ, C_L = 100 pF	25°C	2	2.7		V/μs
			Full range	1.3			
V_n	Equivalent input noise voltage	f = 10 Hz	25°C		18		nV/√Hz
		f = 1 kHz	25°C		8		
$V_{n(pp)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 to 1 Hz	25°C		0.5		μV
		f = 0.1 to 10 Hz	25°C		0.7		
I_n	Equivalent input noise current		25°C		0.6		fA/√Hz
	Gain-bandwidth product	f = 10 kHz, RL = 10 kΩ, CL = 100 pF	25°C		1.9		MHz
φ_m	Phase margin at unity gain	R_L = 10 kΩ, C_L = 100 pF	25°C		48°		

(1) Full range is −55°C to 125°C.
(2) Typical values are based on the input offset voltage shift observable through 168 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

PARAMETER MEASUREMENT INFORMATION

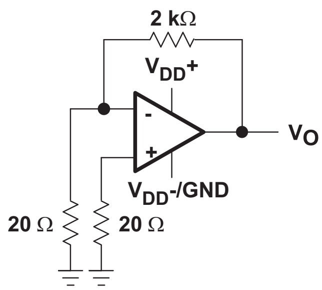
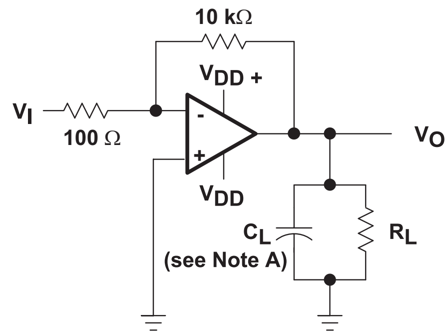
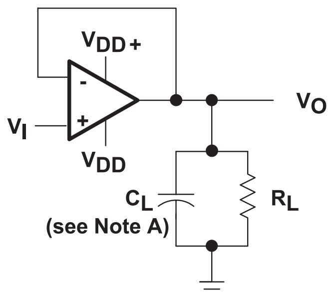


Figure 1. Noise-Voltage Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 2. Phase-Margin Test Circuit



NOTE A: C_L includes fixture capacitance.

Figure 3. Slew-Rate Test Circuit

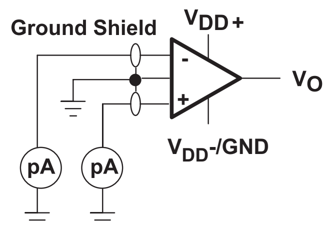


Figure 4. Input-Bias and Offset-Current Test Circuit

TYPICAL VALUES

Typical values presented in this data sheet represent the median (50% point) of device parametric performance.

INPUT BIAS AND OFFSET CURRENT

At the picoamp bias current level of the TLC2201 accurate measurement of the bias current becomes difficult. Not only does this measurement require a picoammeter, but test socket leakages can easily exceed the actual device bias currents. To measure these small currents, Texas Instruments uses a two-step process. The socket leakage is measured using picoammeters with bias voltages applied but with no device in the socket. The device is then inserted in the socket, and a second test measuring both the socket leakage and the device input bias current is performed. The two measurements are then subtracted algebraically to determine the bias current of the device.

NOISE

Texas Instruments offers automated production noise testing to meet individual application requirements. Noise voltage at f = 10 Hz and f = 1 kHz is sample tested on every TLC2201. For other noise requirements, please contact the factory.

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	Figure 5
I_{IB}	Input bias current	vs Common-mode input voltage	Figure 6
		vs Free-air temperature	Figure 7
V_{OM}	Maximum peak output voltage	vs Output curre	Figure 8
		vs Free-air temperature	Figure 9
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	Figure 10
V_{OH}	High-level output voltage	vs Frequency	Figure 11
		vs High-level output current	Figure 12
		vs Free-air temperature	Figure 13
V_{OL}	Low-level output voltage	vs Low-level output current	Figure 14
		vs Free-air temperature	Figure 15
A_{VD}	Large-signal differential voltage amplification	vs Frequency	Figure 16
		vs Free-air temperature	Figure 17
I_{OS}	Short-circuit output current	vs Supply voltage	Figure 18
		vs Free-air temperature	Figure 19
CMRR	Common-mode rejection ratio	vs Frequency	Figure 20
I_{DD}	Supply current	vs Supply voltage	Figure 21
		vs Free-air temperature	Figure 22
	Pulse response	Small signal	Figure 23
			Figure 24
		Large signal	Figure 25
			Figure 26
SR	Slew rate	vs Supply voltage	Figure 27
		vs Free-air temperature	Figure 28
	Noise voltage (referred to input)	0.1 Hz to 1 Hz	Figure 29
		0.1 Hz to 10 Hz	Figure 30
	Gain-bandwidth product	vs Supply voltage	Figure 31
		vs Free-air temperature	Figure 32
φ_m	Phase margin	vs Supply voltage	Figure 33
		vs Free-air temperature	Figure 34
	Phase shift	vs Frequency	Figure 16

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE DISTRIBUTION

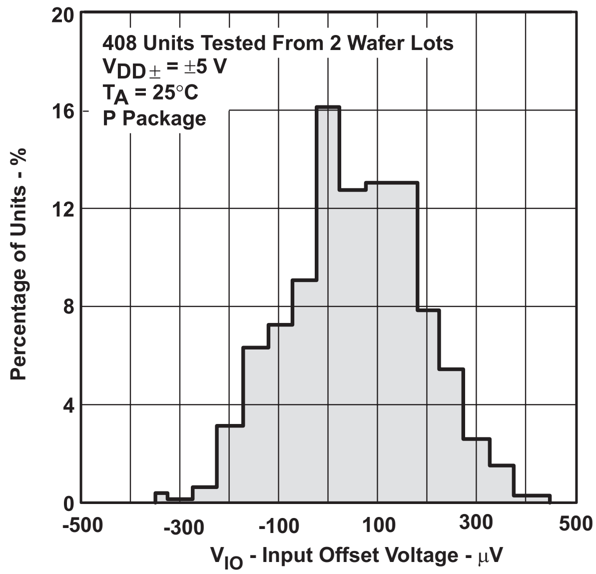


Figure 5.

INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

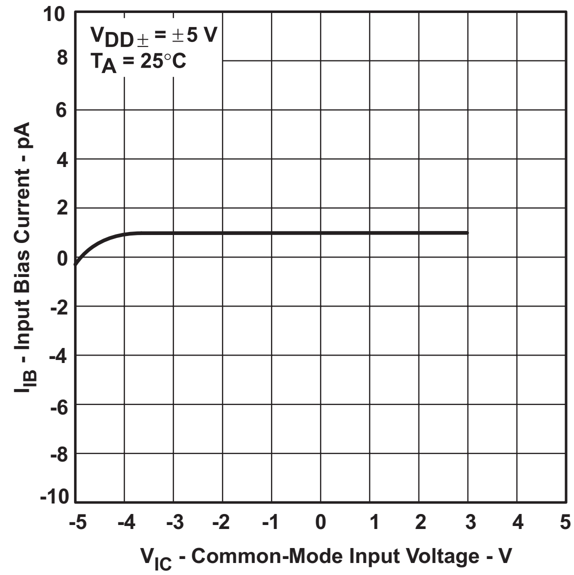


Figure 6.

INPUT BIAS CURRENT[(1)] vs FREE-AIR TEMPERATURE

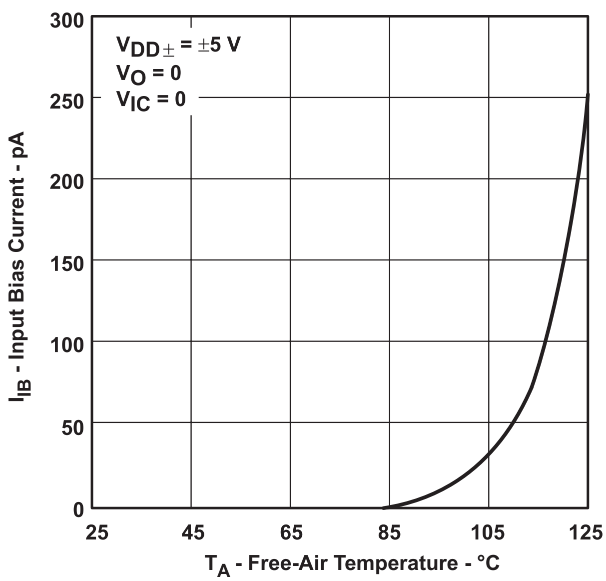


Figure 7.

MAXIMUM PEAK OUTPUT VOLTAGE vs OUTPUT CURRENT

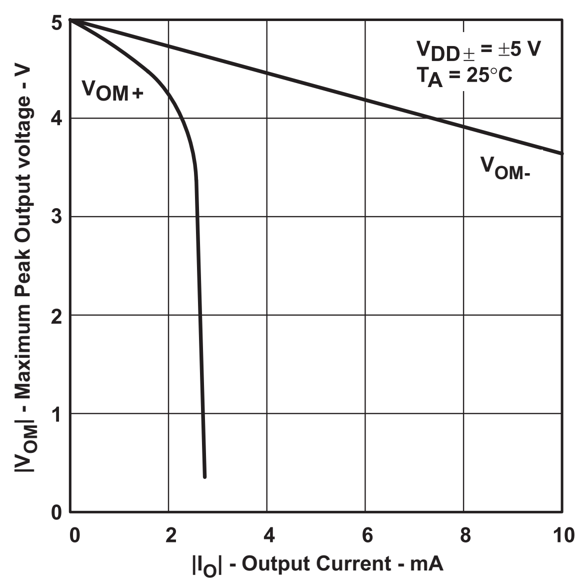


Figure 8.

(1) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (continued)

MAXIMUM PEAK OUTPUT VOLTAGE[(2)] vs FREE-AIR TEMPERATURE

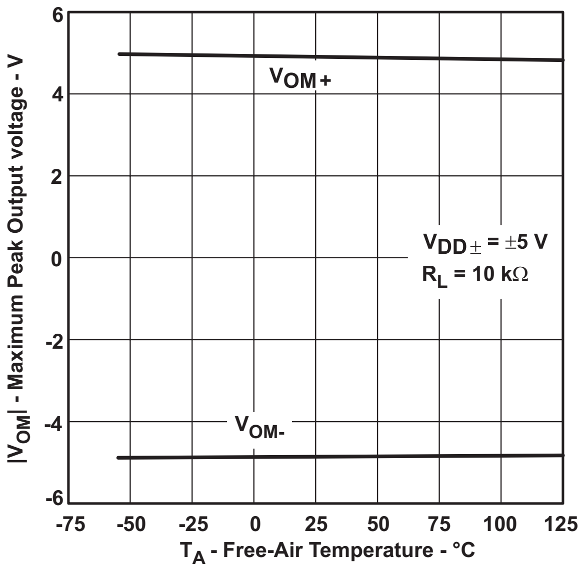


Figure 9.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

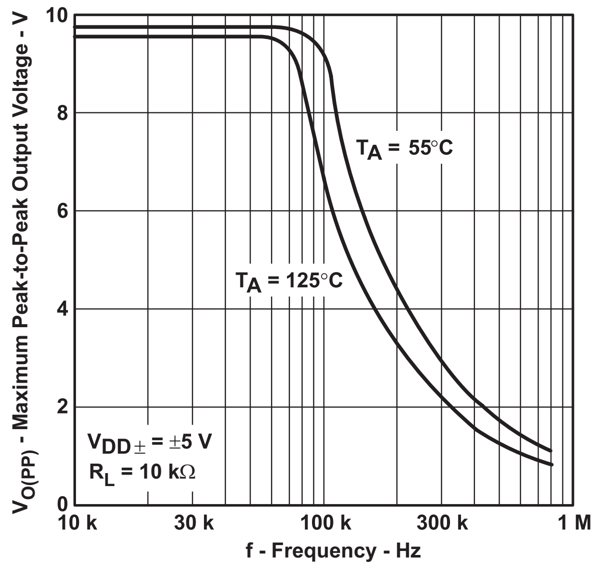


Figure 10.

HIGH-LEVEL OUTPUT VOLTAGE vs FREQUENCY

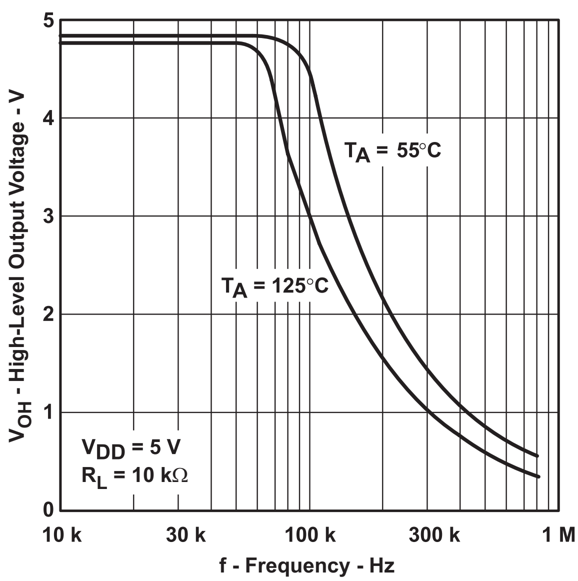


Figure 11.

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

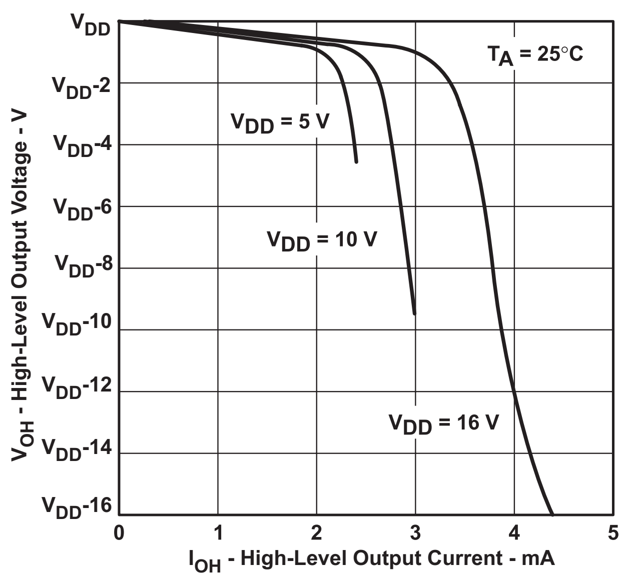


Figure 12.

(2) Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS (continued)

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

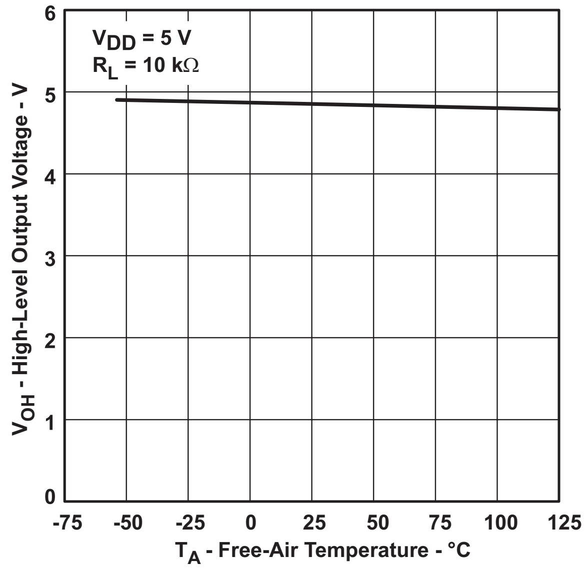


Figure 13.

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

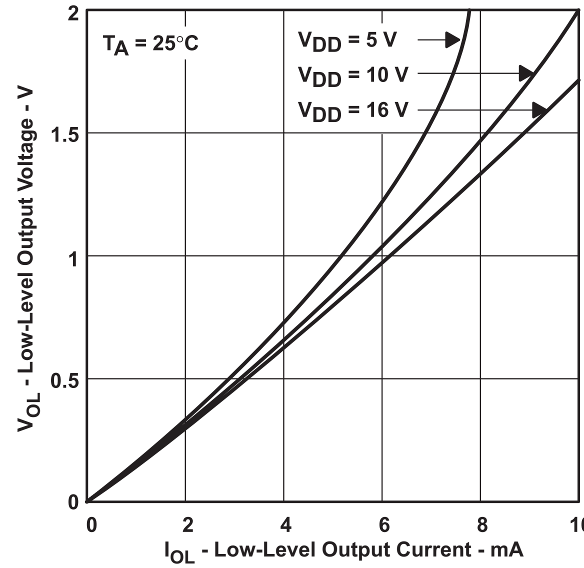


Figure 14.

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

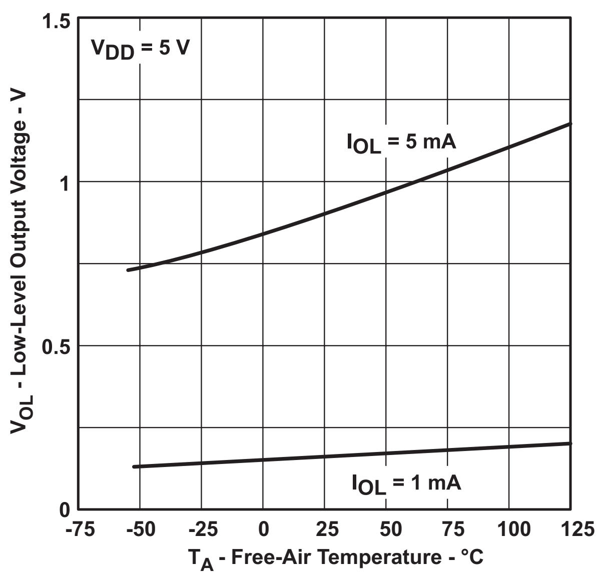


Figure 15.

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

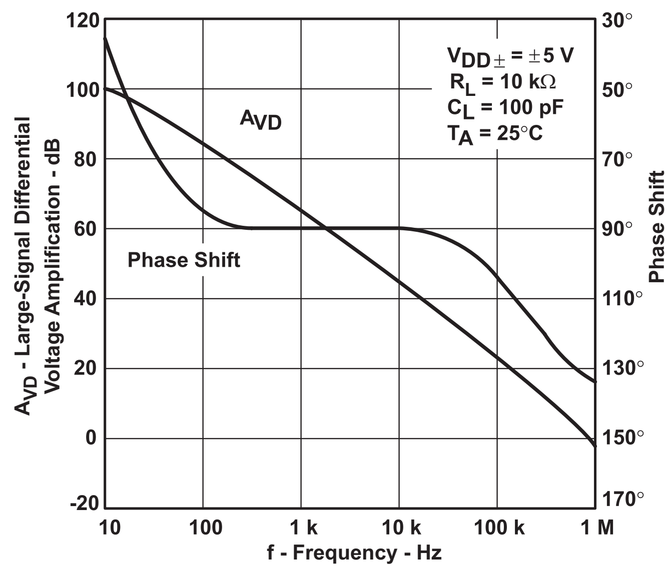


Figure 16.

TYPICAL CHARACTERISTICS (continued)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

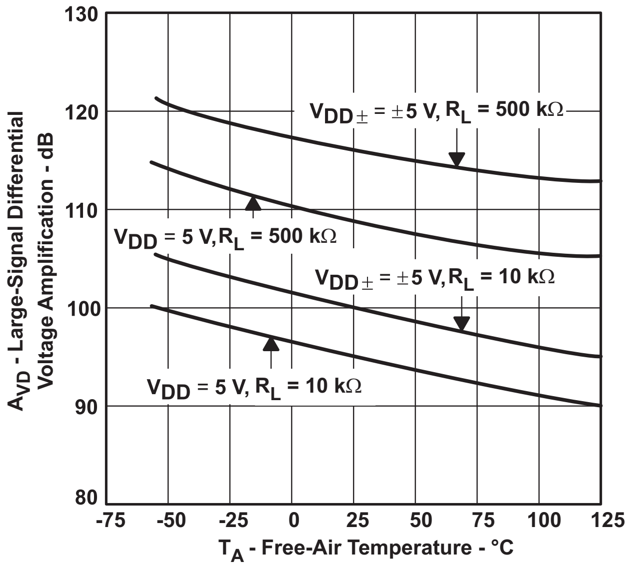


Figure 17.

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

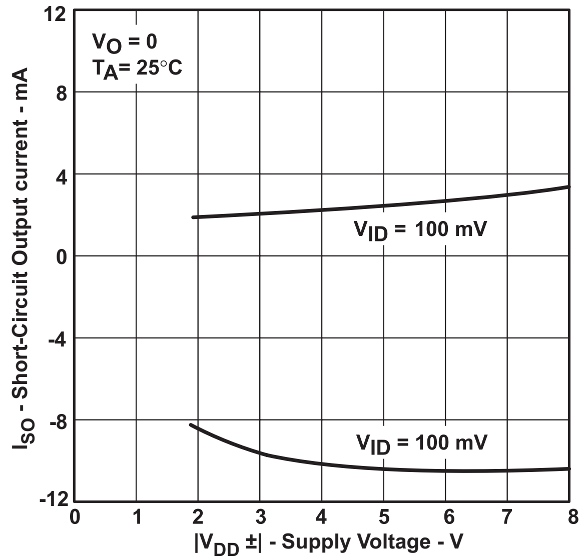


Figure 18.

SHORT-CIRCUIT OUTPUT CURRENT
vs
FREE-AIR TEMPERATURE

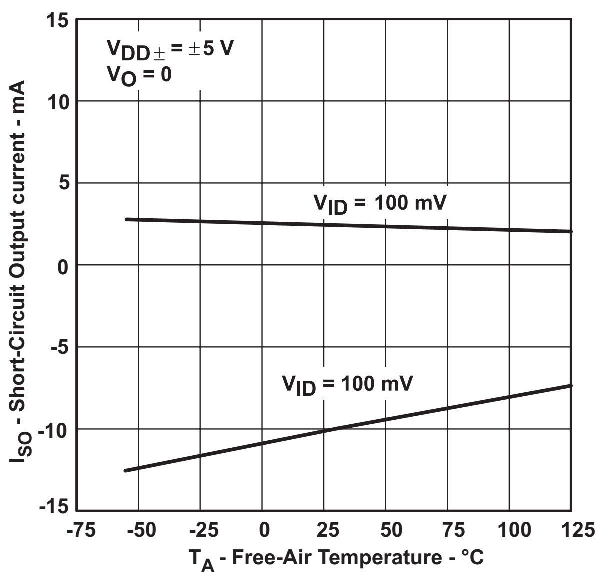


Figure 19.

COMMON-MODE REJECTION RATIO
vs
FREQUENCY

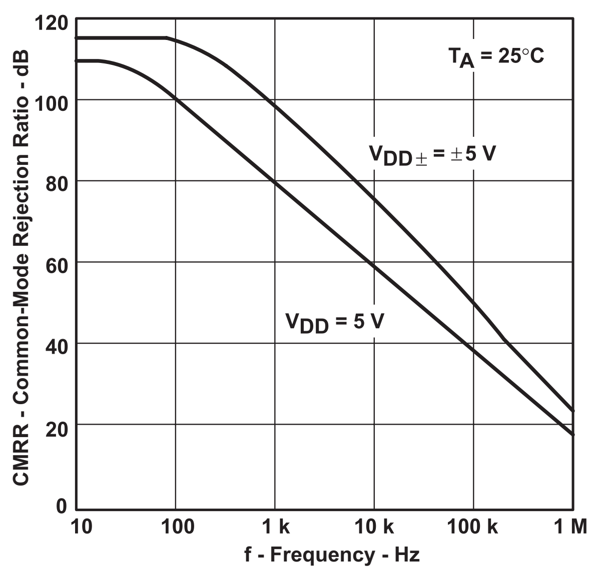


Figure 20.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

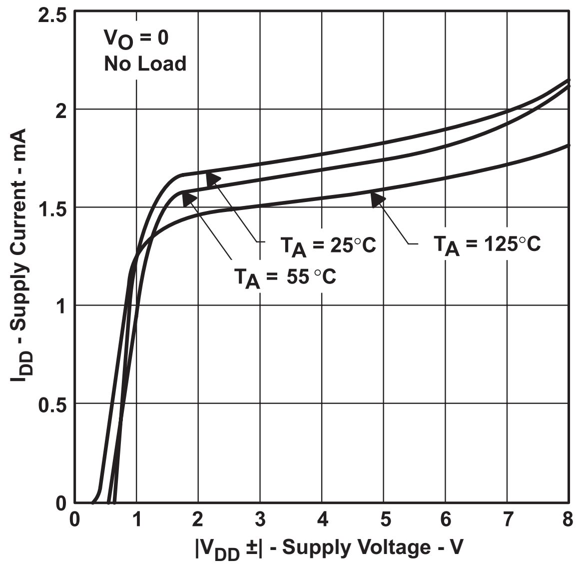


Figure 21.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

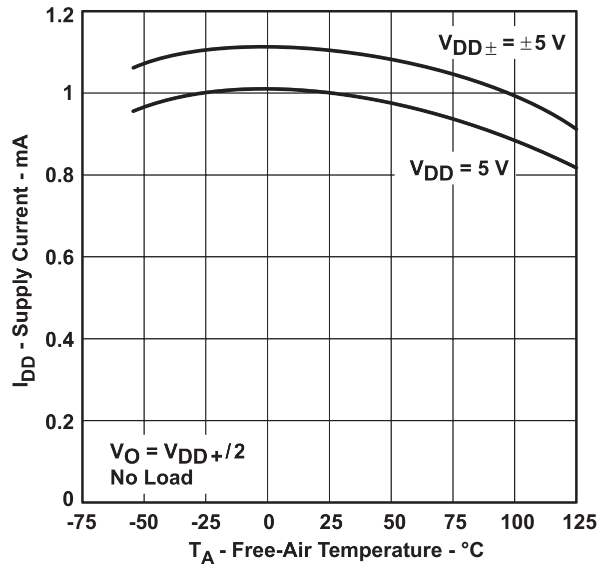


Figure 22.

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

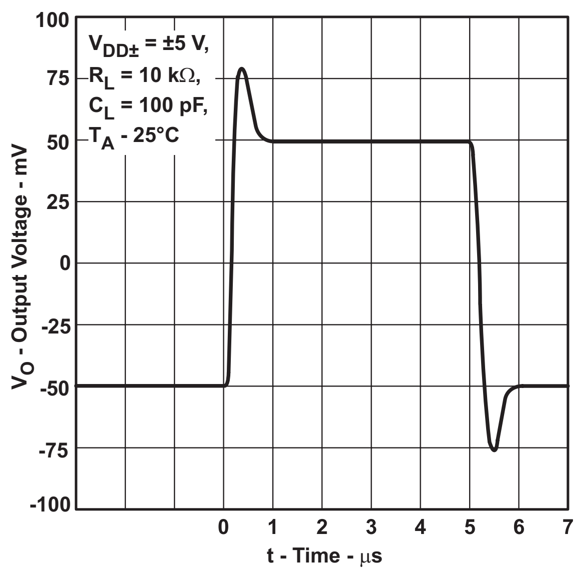


Figure 23.

VOLTAGE-FOLLOWER
SMALL-SIGNAL
PULSE RESPONSE

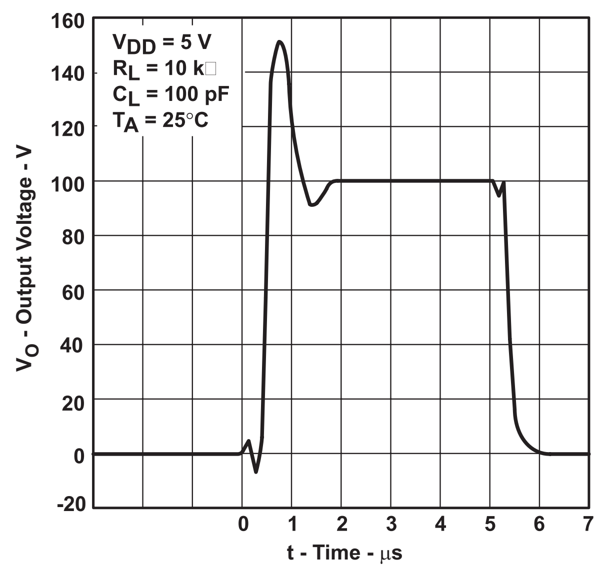


Figure 24.

TYPICAL CHARACTERISTICS (continued)

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

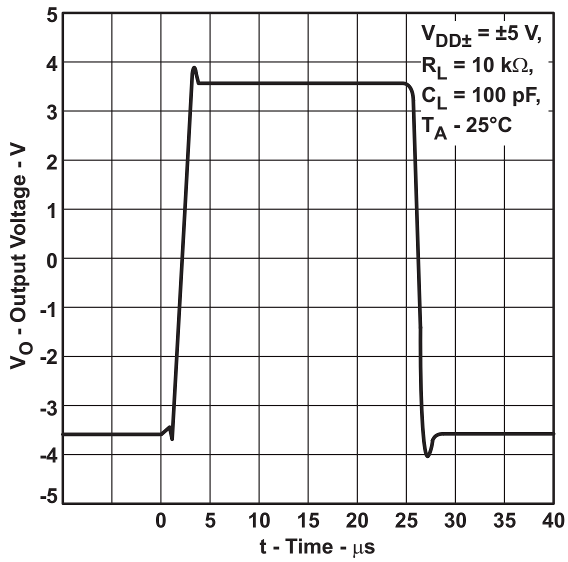


Figure 25.

VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE

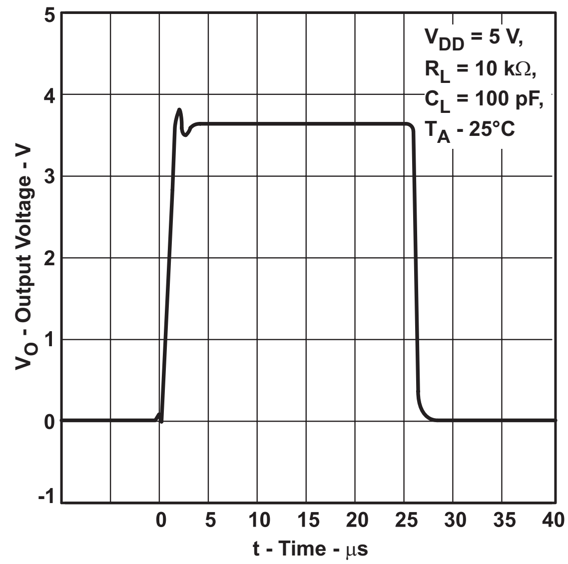


Figure 26.

SLEW RATE vs SUPPLY VOLTAGE

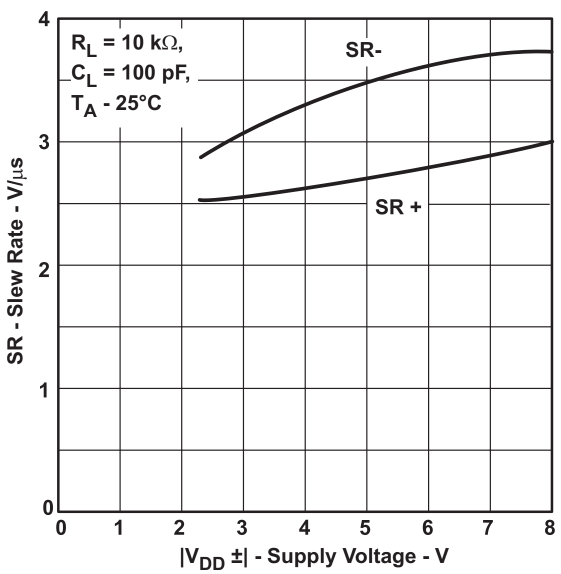


Figure 27.

SLEW RATE vs FREE-AIR TEMPERATURE

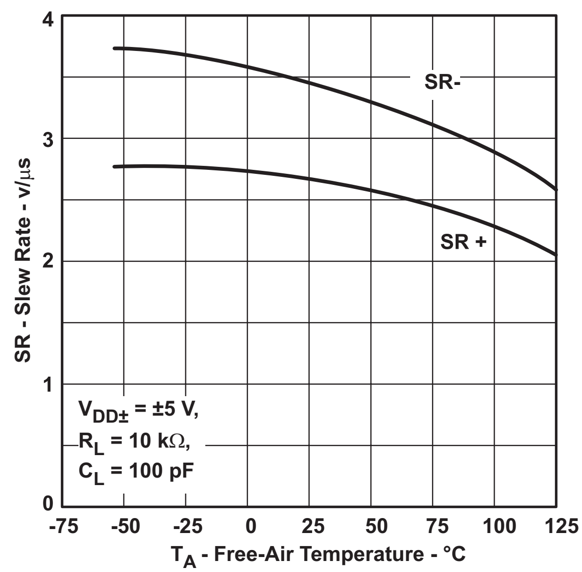


Figure 28.

TYPICAL CHARACTERISTICS (continued)

NOISE VOLTAGE (REFERRED TO INPUT) OVER A 10-SECOND INTERVAL

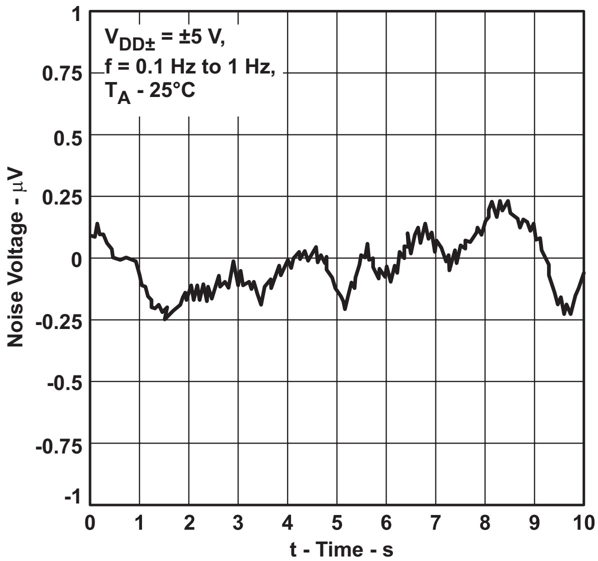


Figure 29.

NOISE VOLTAGE (REFERRED TO INPUT) OVER A 10-SECOND INTERVAL

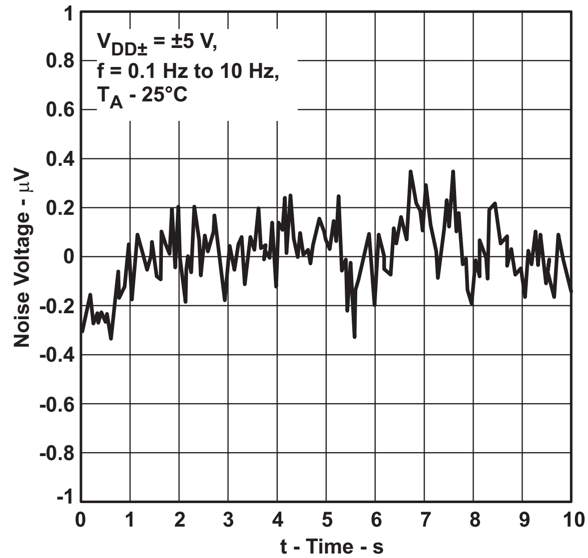


Figure 30.

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

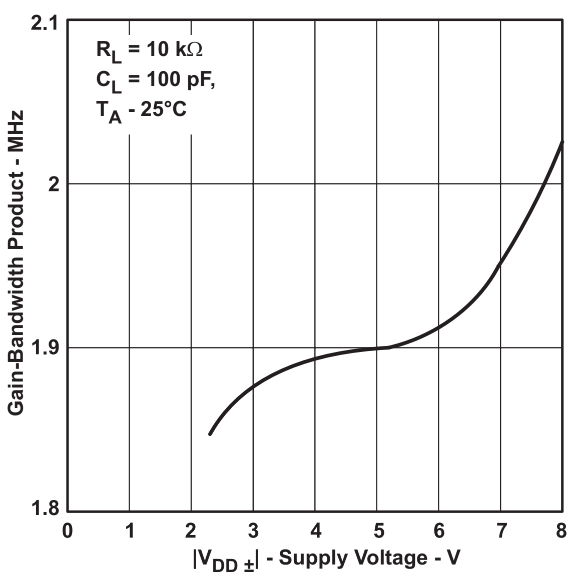


Figure 31.

GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE

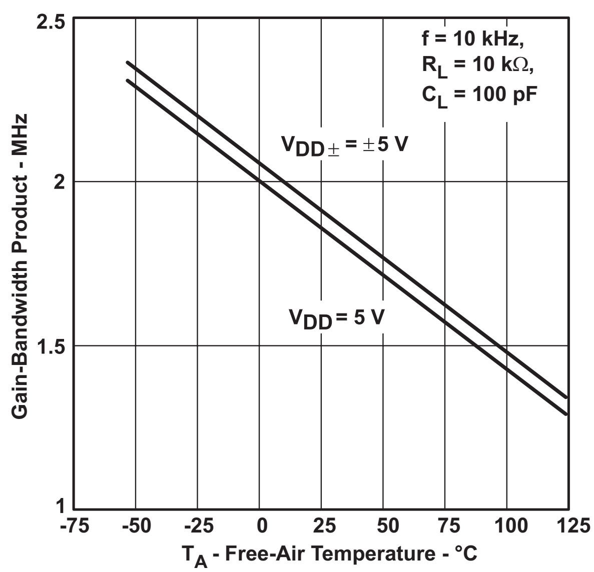


Figure 32.

TYPICAL CHARACTERISTICS (continued)

PHASE MARGIN vs SUPPLY VOLTAGE

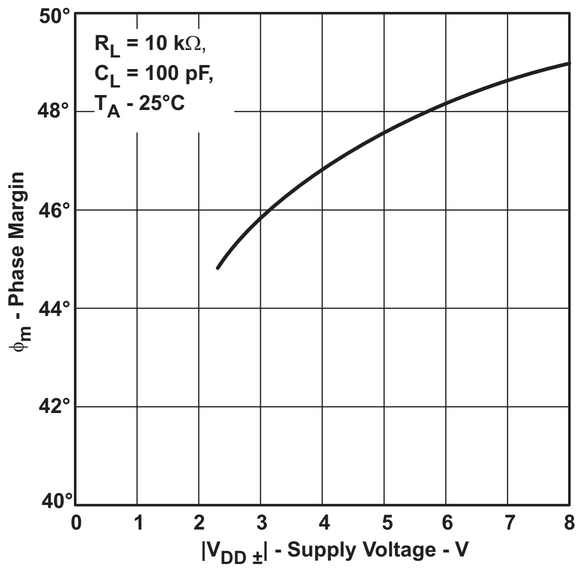


Figure 33.

PHASE MARGIN vs FREE-AIR TEMPERATURE

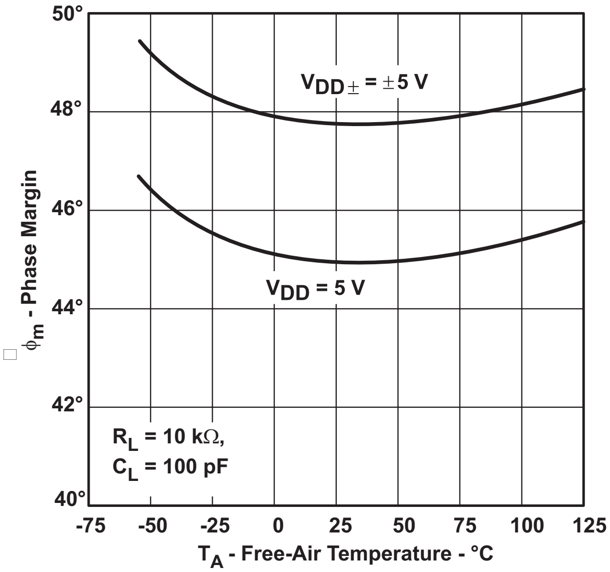


Figure 34.

APPLICATION INFORMATION

LATCH-UP AVOIDANCE

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLC2201 inputs and outputs are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques reducing the chance of latch-up should be used whenever possible. Internal protection diodes should not be forward biased in normal operation. Applied input and output voltages should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

ELECTROSTATIC DISCHARGE PROTECTION

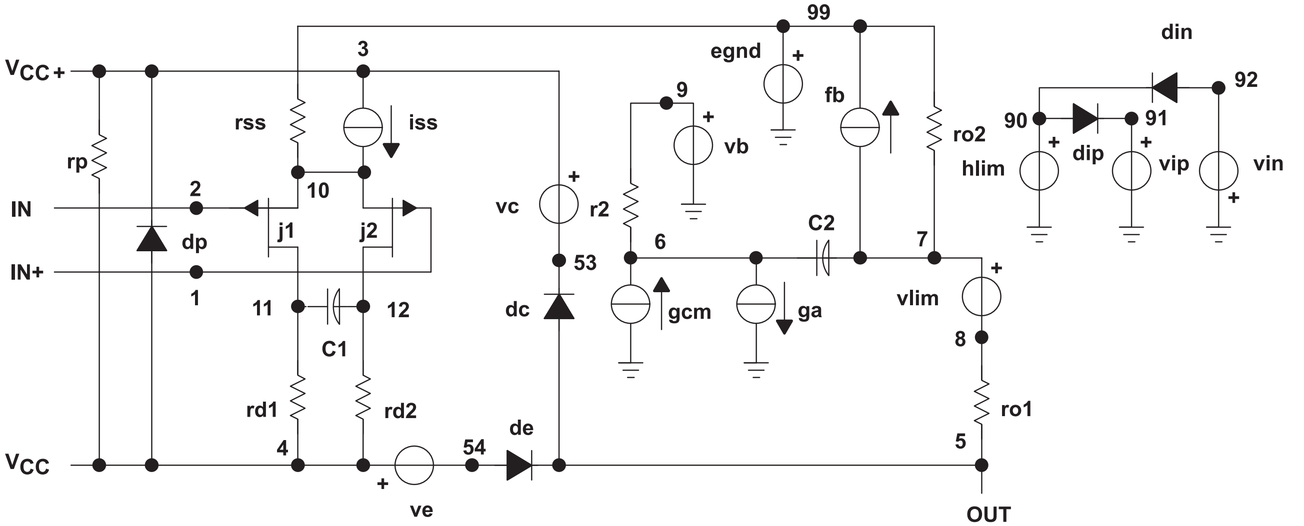
These devices use internal ESD-protection circuits that prevent functional failures at voltages at or below 2000 V. Care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

MACROMODEL INFORMATION

Macromodel information provided was derived using Microsim Parts™, the model generation software used with Microsim PSpice™. The Boyle macromodel[3] and subcircuit in Figure 35 were generated using the TLC2201 typical electrical and operating characteristics at 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

(3) G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Integrated Circuit Operational Amplifiers”, IEEE Journal of Solid-State Circuits, SC-9, 353 (1974).




```
.subckt TLC220x  1 2 3 4 5
*
   c1      11   12  8.51E12
   c2      6     7    50.00E12
   cpsr  85   86  79.6E9
   dcm+  81   82  dx
   dcm  83   81  dx
   dc     5     53  dx
   de     54    5    dx
   dlp    90   91  dx
   dln    92   90  dx
   dp     4     3    dx
   ecmr  84   99  (2,99) 1
   egnd  99   0    poly(2) (3,0) (4,0) 0 .5 .5
   epsr  85   0    poly(1) (3,4) 200E6 20E6
   ense  89   2    poly(1) (88,0) 100E6 1
   fb     7     99  poly(6) vb vc ve vlp vln
+   vpsr 0 +       895.9E3 90E3 90E3 90E3 90E3 895E3
   ga     6     0     11 12 314.2E6
   gcm   0     6     10 99 1.295E9
   gpsr  85   86  (85,86) 100E6
   grd1  60   11  (60,11) 3.141E4
   grd2  60   12  (60,12) 3.141E4
   hlim  90   0    vlim 1k
   hcmr  80   1    poly(2) vcm+ vcm 0 1E2 1E2
   irp    3     4    965E6
   iss    3     10   dc 135.0E6
   iio    2     0     .5E12
   i1      88   0     1E21
   j1      11   89   10 jx
   j2      12   80   10 jx
   r2      6     9     100.0E3
   rcm    84   81   1k
   rn1    88   0     1500
   ro1    8     5     188
   ro2    7     99   187
   rss    10   99   1.481E6
   vad    60   4     .3v
   vcm+  82   99   2.2
   vcm   83   99   4.5
   vb      9     0     dc 0
   vc      3     53   dc .9
   ve      54   4     dc .8
   vlim   7     8     dc 0
   vlp    91   0     dc 2.8
   vln    0     92   dc 2.8
   vpsr   0     86   dc 0
.model  dx   d(is=800.0E18)
.model  jx  pjf(is=500.0E15 beta=1.462E3
+ vto=.155 kf=1E17)
.endsx
```

Figure 35. Boyle Macromodel and Subcircuit

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安全	http://www.ti.com.cn/security
电话	http://www.ti.com.cn/telecom
视频与成像	http://www.ti.com.cn/video
无线	http://www.ti.com.cn/wireless

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9088203V2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9088203V2A TLC2201 AMFKBQMLV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLC2201-SP :

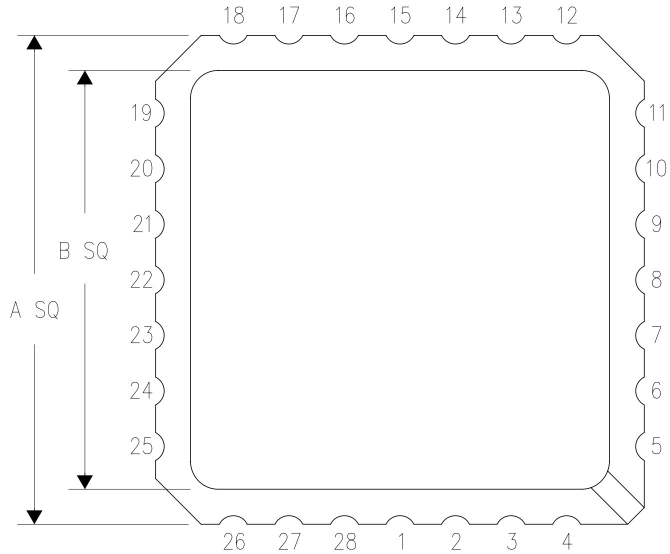
- Catalog : TLC2201
- Military : TLC2201M

NOTE: Qualified Version Definitions:

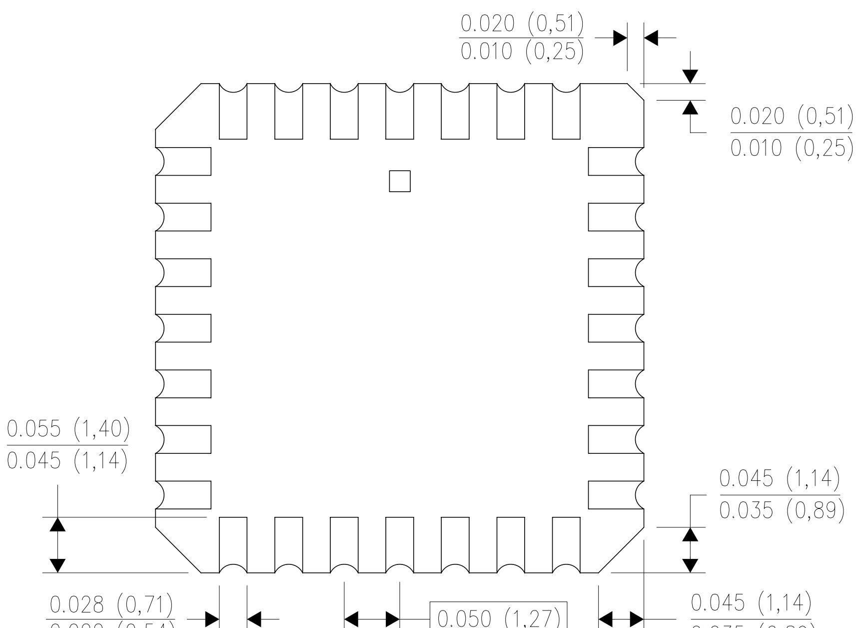
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

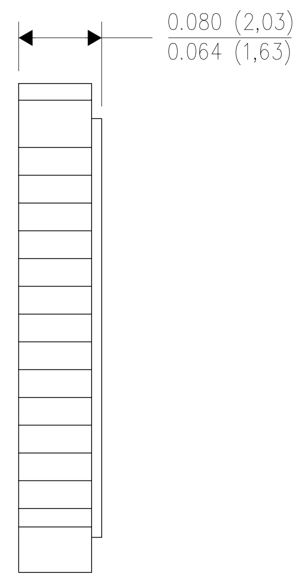
FK (S-CQCC-N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)





4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS-004