

TLV761 16V、1A、固定输出线性稳压器

1 特性

- 引脚与业界通用的 **LM1117** 和 **x1117** 器件兼容
 - 更低的 I_Q : 60 μ A
 - 折返电流限制
 - 高精度: 2% (最大值)
 - 与陶瓷电容和其他电容一起工作时可保持稳定
 - 高 PSRR: 1MHz 时为 46dB
- V_{IN} : 2.5V 至 16V
 - V_{IN} 绝对最大值: 18V
- V_{OUT} : 0.8V 至 13V (固定)
 - 采用业界通用电压 (例如 3.3V、5.0V、12V)
- 最低保证限流: 1.1A
- 温度范围: -40°C 至 +125°C
- 热关断保护
- 封装: SOT-223

2 应用

- 电器
- 家庭影院和娱乐系统
- 电机驱动器
- HVAC 和楼宇安全系统
- 智能仪表
- 电机驱动控制板

3 说明

TLV761 是一款线性稳压器，它通过减小接地电流来降低待机功耗，同时提高浪涌性能，从而改进了传统 x1117 稳压器 (TLV1117 或 LM1117) 的功能。

TLV761 与固定输出电压的 SOT-223 稳压器引脚对引脚兼容。

TLV761 输入电压范围为 2.5V 至 16V，提供的输出电压范围为 1.2V 至 13V，可支持各种应用。此外，TLV761 还具有内部软启动功能，可减少启动期间的浪涌电流，这有助于通过最小化输入电容来节省设计空间和成本。TLV761 具有折返电流限制，可在高负载电流故障或短路事件期间限制器件的功率耗散。

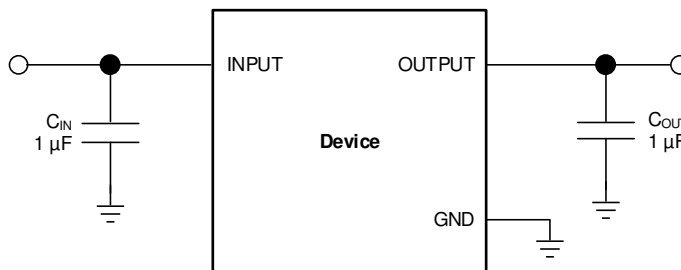
TLV761 采用 SOT-223 封装。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TLV761	SOT-223 (4)	6.50mm x 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路



目录

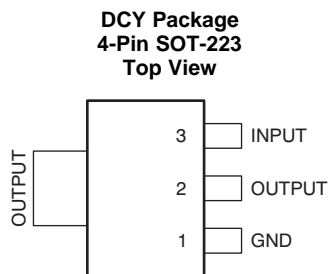
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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2020 年 2 月	*	初始发行版。

5 Pin Configuration and Functions



Pin Functions

NO.	NAME	I/O	DESCRIPTION
1	GND	—	Ground pin
2, Tab	OUTPUT	O	Regulated output voltage pin
3	INPUT	I	Input pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	V_{IN}	-0.3	18	V
	V_{OUT}	-0.3	$V_{IN} + 0.3$	V
Current	I_{OUT}	Internally limited		A
Temperature	Operating junction temperature (T_J)	-55	150	°C
	Storage temperature (T_{stg})	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2.5		16	V
V_{OUT}	Output voltage	1.2		13	V
I_{OUT}	Output current	0		1	A
C_{OUT}	Recommended output capacitance range	1	2.2	220	µF
C_{OUT} ESR	Output capacitor ESR	2		500	mΩ
C_{IN}	Recommended input capacitance		1		µF
T_J	Junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV761	UNIT
		DCY (SOT-223)	
		4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

at operating temperature range ($T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$), $V_{IN} = V_{OUT(NOM)} + 1.5\text{ V}$ or 2.5 V , whichever is greater, $I_{OUT} = 10\text{ mA}$, $C_{IN} = 1\text{ }\mu\text{F}$, $C_{OUT} = 1\text{ }\mu\text{F}$ (unless otherwise noted); all typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Nominal output accuracy	$T_J = 25^{\circ}\text{C}$	-1		1	%
	DC output accuracy	$V_{IN} \geq 3.0\text{ V}$, $1\text{ mA} \leq I_{OUT} \leq 1\text{ A}$ $2.5\text{ V} \leq V_{IN} \leq 3.0\text{ V}$, $1\text{ mA} \leq I_{OUT} \leq 800\text{ mA}$	-2		2	
$\Delta V_{OUT(\Delta V_{IN})}$	Line regulation	$V_{OUT(NOM)} + 1.5\text{ V} \leq V_{IN} \leq 16\text{ V}$, $I_{OUT} = 10\text{ mA}$.			0.02	%/V
$\Delta V_{OUT(\Delta I_{OUT})}$	Load regulation	$1\text{ mA} \leq I_{OUT} \leq 1\text{ A}$, $V_{IN} \geq 3.0\text{ V}$		0.1	0.5	%/A
		$1\text{ mA} \leq I_{OUT} \leq 800\text{ mA}$, $2.5\text{ V} \leq V_{IN} \leq 3.0\text{ V}$		0.1	0.5	
V_{DO}	Dropout voltage ⁽¹⁾	$V_{IN} \geq 3.0\text{ V}$, $I_{OUT} = 1\text{ A}$		1.2	1.7	V
		$2.5\text{ V} \leq V_{IN} \leq 3.0\text{ V}$, $I_{OUT} = 800\text{ mA}$		1	1.6	
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(NOM)}$, $V_{IN} \geq 3.0\text{ V}$	1.1		1.8	A
		$V_{OUT} = 0.9 \times V_{OUT(NOM)}$, $2.5\text{ V} \leq V_{IN} \leq 3.0\text{ V}$	0.81		1.6	
I_{SC}	Short-circuit current limit	$V_{OUT} = 0\text{ V}$		250		mA
I_Q	Quiescent current	$I_{OUT} = 0\text{ mA}$		60	100	μA
PSRR	Power supply rejection ratio	$V_{IN} = 3.3\text{ V}$, $V_{OUT} = 1.8\text{ V}$, $I_{OUT} = 300\text{ mA}$, $f = 120\text{ Hz}$		70		dB
V_n	Output noise voltage	BW 10 Hz to 100 kHz, $V_{IN} = 3.3\text{ V}$, $V_{OUT} = 0.8\text{ V}$, $I_{OUT} = 100\text{ mA}$		60		μV_{RMS}
UVLO	Under voltage lockout	V_{IN} rising		2.2	2.4	V
		Hysteresis falling		130		mV
		V_{IN} falling	1.9			V
$I_{Pulldown}$	Pulldown current	$V_{IN} = V_{OUT} = 1.9\text{ V}$		1.2		mA
T_{SD}	Thermal shutdown temperature	Shutdown temperature increasing		180		°C
		Reset temperature falling		160		°C

(1) V_{DO} is measured with $V_{IN} = 95\% \times V_{OUT(nom)}$. V_{DO} is not measured for fixed output devices when $V_{OUT} < 2.5\text{ V}$.

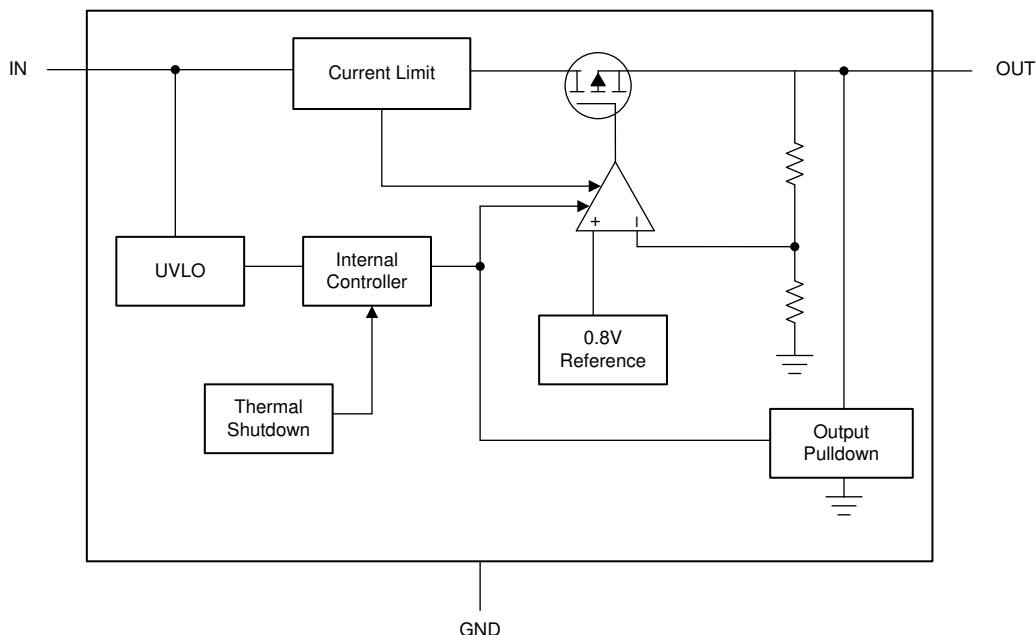
7 Detailed Description

7.1 Overview

The TLV761 is a low quiescent current, high PSRR linear regulator capable of handling up to 1 A of load current. Unlike typical high current linear regulators, the TLV761 consumes significantly less quiescent current. This device is ideal for high current applications such as appliances where there are increasingly stringent requirements for standby and active power consumption.

This device features integrated foldback current limit, thermal shutdown, internal output pulldown, and undervoltage lockout (UVLO). This device delivers excellent line and load transient performance. The TLV761 is low noise and exhibits very good PSRR. The operating ambient temperature range of the device is -40°C to $+125^{\circ}\text{C}$.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. Use [Equation 1](#) to calculate the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (1)$$

Feature Description (continued)

7.3.2 Foldback Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a hybrid brickwall-foldback scheme. The current limit transitions from a brickwall scheme to a foldback scheme at the foldback voltage ($V_{FOLDBACK}$). In a high-load current fault with the output voltage above $V_{FOLDBACK}$, the brickwall scheme limits the output current to the current limit (I_{CL}). When the voltage drops below $V_{FOLDBACK}$, a foldback current limit activates that scales back the current as the output voltage approaches GND. When the output is shorted, the device supplies a typical current called the short-circuit current limit (I_{SC}). I_{CL} and I_{SC} are listed in the *Electrical Characteristics* table.

For this device, $V_{FOLDBACK} = 50\% \times V_{OUT(nom)}$.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brickwall current limit, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{CL}]$. When the device output is shorted and the output is below $V_{FOLDBACK}$, the pass transistor dissipates power $[(V_{IN} - V_{OUT}) \times I_{SC}]$. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the [Know Your Limits application report](#).

Figure 1 shows a diagram of the foldback current limit.

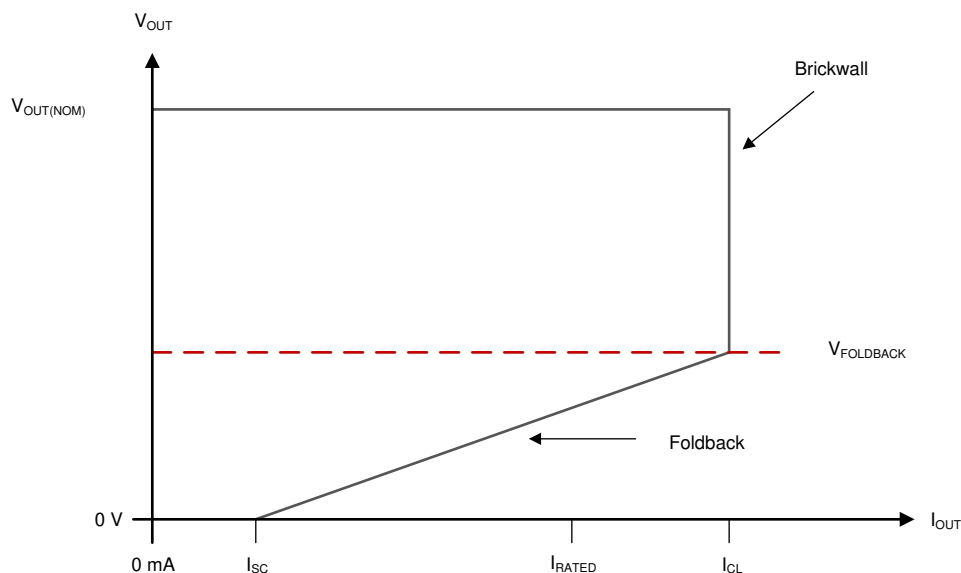


Figure 1. Foldback Current Limit

7.3.3 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.4 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

Feature Description (continued)

The thermal time-constant of the semiconductor die is fairly short, thus the device may cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during startup can be high from large $V_{IN} - V_{OUT}$ voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before startup completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

The *Device Functional Mode Comparison* table shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output-voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during startup), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. As a rule of thumb, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors recommended in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. An input capacitor is recommended if the source impedance is more than 0.5 Ω . A higher value capacitor may be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.1.3 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leq V_{IN} + 0.3$ V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

Application Information (接下页)

If reverse current flow is expected in the application, external protection is recommended to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

Figure 2 shows one approach for protecting the device.

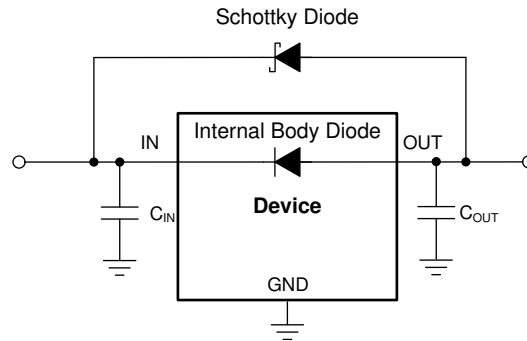


Figure 2. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.4 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. Equation 2 calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

NOTE

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to Equation 3, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (3)$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

Application Information (接下页)

8.1.5 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (Ψ_{JT}) and junction-to-board characterization parameter (Ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J). As described in , use the junction-to-top characterization parameter (Ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. As described in , use the junction-to-board characterization parameter (Ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \Psi_{JT} \times P_D$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

$$T_J = T_B + \Psi_{JB} \times P_D$$

where

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the [Semiconductor and IC Package Thermal Metrics application report](#).

8.2 Typical Application

The TLV761 is a low quiescent current linear regulator designed for high current applications. Unlike most typical high current linear regulators, the TLV761 consumes significantly less quiescent current. This device delivers excellent line and load transient performance. The device is low noise and exhibits a very good PSRR. As a result, the TLV761 is ideal for high current applications that require very sensitive power-supply rails.

This regulator offers both current limit and thermal protection. The operating ambient temperature range of the device is -40°C to $+125^{\circ}\text{C}$.

图 3 shows a typical application circuit for this device.

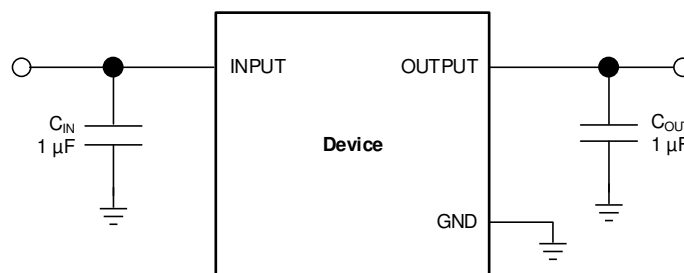


图 3. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 2 as the input parameters.

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	12 V
Output voltage	3.3 V
Output current	500 mA

8.2.2 Detailed Design Procedure

For this design example, the 3.3-V, fixed-version TLV76133 is selected and is powered by a standard 12-V input supply. The dropout voltage (V_{DO}) is kept within the TLV761 dropout voltage specification for the 3.3-V output voltage option to keep the device in regulation under all load and temperature conditions for this design. A 1.0- μ F output capacitor is recommended for excellent load transient response. The input capacitor is optional and is used to reduce the input impedance of the circuit and improve the transient response.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude.

8.3 What To Do and What Not To Do

Place input and output capacitors as close to the device as possible.

Use a ceramic output capacitor.

Do not exceed the device absolute maximum ratings.

9 Power Supply Recommendations

Connect a low output impedance power supply directly to the INPUT pin of the device. Inductive impedances between the input supply and the INPUT pin can create significant voltage excursions at the INPUT pin during startup or load transient events.

10 Layout

10.1 Layout Guidelines

Place input and output capacitors should be placed as close to the device pins as possible. To improve characteristic AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT} , with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the GND pin of the device. Higher value ESR capacitors may degrade PSRR performance.

10.2 Layout Example

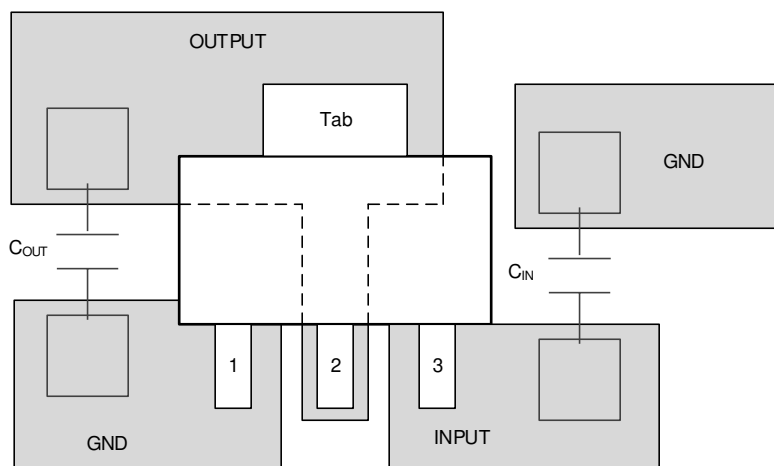


图 4. Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

表 3. 可用选项⁽¹⁾⁽²⁾

产品	V _{OUT}
TLV761xxyyyz	xx 是标称输出电压 (比如, 33 = 3.3V) yyy 为封装标识符 z 为封装数量

- (1) 要获得最新的封装和订货信息, 请参阅本文档末尾的封装选项附录, 或者访问 www.ti.com.cn 上的器件产品文件夹。
 (2) 该器件可按需提供工厂可编程的固定输出电压, 单位增量为 50mV。

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档:

- 德州仪器 (TI), 《[TLV1117 可调节和固定低压降稳压器](#)》数据表
- 德州仪器 (TI), 《[LM1117 800mA 低压降线性稳压器](#)》数据表

11.3 接收文档更新通知

要接收文档更新通知, 请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册, 即可每周接收产品信息更改摘要。有关更改的详细信息, 请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 商标

E2E is a trademark of Texas Instruments.
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11.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序, 可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更, 恕不另行通知, 且不会对此文档进行修订。如需获取此数据表的浏览器版本, 请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLV76133DCYR	ACTIVE	SOT-223	DCY	4	2500	TBD	Call TI	Call TI	-40 to 125		Samples
PTLV76118DCYR	OBSOLETE	SOT-223	DCY	4		TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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DCY (R-PDSO-G4)

PLASTIC SMALL-OUTLINE



- NOTES: A. All linear dimensions are in millimeters (inches).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion.
 D. Falls within JEDEC TO-261 Variation AA.

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