适用于功率敏感型应用的 TLV904x 1.2V 超低电压 10μA 微功耗 RRIO 放大器

1 特性

- 适用于成本优化型应用的低功耗 CMOS 放大器
- 可在电源电压低至 1.2V 的情况下运行
- 低输入偏置电流：1pA（典型值），12pA（最大值）
- 低静态电流：10μA/通道
- 在 0.1Hz 至 10Hz 范围内具有 6.5μV_{p-p} 的低集成噪声
- 轨至轨输入和输出
- 高增益带宽积：350kHz
- 热本底噪声：64nV/√Hz
- 低输入失调电压：±0.6mV
- 单位增益稳定
- 稳健驱动 100pF 的负载电容
- 内置 RFI 和 EMI 滤波输入引脚
- 宽额定温度范围：–40°C 至 125°C

2 应用

- 便携式电子产品
- 可穿戴健身和活动监测仪
- 耳麦/耳机和耳塞
- 个人电子产品
- 楼宇自动化
- 可穿戴设备（非医用）
- 运动检测器（PIR、uWave 等）
- 电子销售点 (EPOS)
- 单电源、低侧、单向电流检测电路

3 说明

低功耗 TLV904x 系列包括单通道 (TLV9041)、双通道 (TLV9042) 和四通道 (TLV9044) 超低压（1.2V 至 5.5V）运算放大器，具有轨至轨输入和输出摆幅功能。TLV904x 凭借低静态电流（10 μA，典型值）和在低至 1.2V 的电源电压下运行的能力实现功耗节省，因此成为业界为数不多的可支持 1.5V 纽扣电池应用的放大器之一。使用关断模式（TLV9041S、TLV9042S 和 TLV9044S）可以进一步节省功耗：让放大器关闭并进入典型电流消耗小于 150 nA 的待机模式。这些器件为电源和空间受限的应用（例如电池供电的物联网器件、可穿戴电子产品和低电压运行至关重要的个人电子产品）提供了具有成本效益的放大器解决方案。

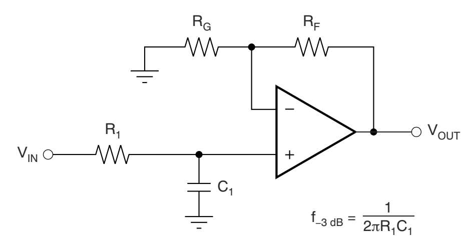
TLV904x 系列的稳健设计有助于简化电路设计。这些运算放大器集成了 RFI 和 EMI 抑制滤波器，具有单位增益稳定性，并且在输入过驱条件下不会出现相位反转。该器件还提供出色的交流性能，增益带宽为 350 kHz，高容性负载驱动为 100 pF，使设计人员能够实现更高的性能和更低的功耗。

针对所有通道型号（单通道、双通道和四通道）提供节省空间的微型封装（如 X2QFN 和 WSON）以及行业标准封装（如 SOIC、VSSOP、TSSOP 和 SOT-23 封装）。

器件信息

器件型号(1) (2)	封装	封装尺寸（标称值）
TLV9041	SOT-23 (5)	1.60mm × 2.90mm
	SC70 (5)	1.25mm × 2.00mm
	X2SON (5)	0.80mm × 0.80mm
TLV9041S	SOT-23 (6)	1.60mm × 2.90mm
TLV9042	SOIC (8)	3.91mm × 4.90mm
	SOT-23 (8)	1.60mm × 2.90mm
	WSON (8)	2.00mm × 2.00mm
	VSSOP (8)	3.00mm × 3.00mm
	TSSOP (8)	3.00mm × 4.40mm
TLV9042S	X2QFN (10)	1.50mm x 2.00mm
TLV9044	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	4.40mm × 5.00mm
	SOT-23 (14)	4.20mm × 1.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 其他单通道和双通道封装型号将于近期发布。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

单极低通滤波器

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (February 2022) to Revision G (March 2022) — **Page**

- 更新了 X2SON (5) RTM 的*器件信息* 部分 ... 1
- Updated *Device Comparison* section for TLV9041IDPWR RTM ... 3
- Added Thermal Information for TLV9041 DPW package to the *Thermal Information for Single Channel* section ... 7

Changes from Revision E (August 2021) to Revision F (February 2022) — **Page**

- Updated *Device Comparison* section for TLV9044IDYYR RTM ... 3
- Added Thermal Information for TLV9044 DYY package to the *Thermal Information for Quad Channel* section ... 7

Changes from Revision D (August 2021) to Revision E (August 2021) — **Page**

- Added Thermal Information for TLV9042 DGK package to the *Thermal Information for Dual Channel* section ... 7

5 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS												
		SC70 DCK	SOIC D	SOT-23 DBV	SOT-23 DYY	SOT-23-8 DDF	SOT-553 DRL(1)	TSSOP PW	VSSOP DGK	WQFN RTE(1)	WSON DSG	X2QFN RUC(1)	X2SON DPW	X2QFN RUG
TLV9041	1	5	—	5	—	—	5	—	—	—	—	—	5	—
TLV9041S	1	—	—	6	—	—	—	—	—	—	—	—	—	—
TLV9042	2	—	8	—	—	8	—	8	8	—	8	—	—	—
TLV9042S	2	—	—	—	—	—	—	—	—	—	—	—	—	10
TLV9044	4	—	14	—	14	—	—	14	—	16	—	14	—	—

(1) Package is preview only.

6 Pin Configuration and Functions

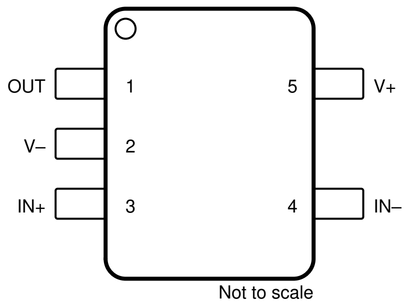


图 6-1. TLV9041 DBV Package
5-Pin SOT-23
Top View

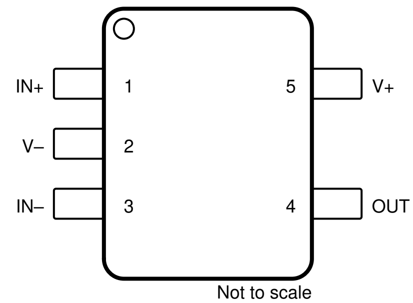


图 6-2. TLV9041U DBV Package
5-Pin SOT-23
Top View

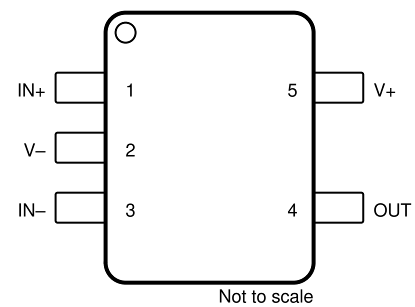


图 6-3. TLV9041 DCK Package
5-Pin SC70
Top View

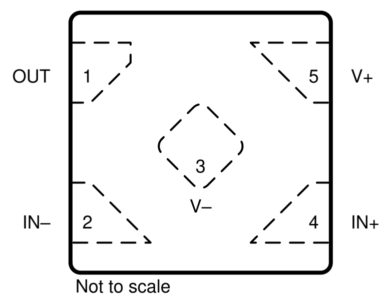


图 6-4. TLV9041 DPW Package
5-Pin X2SON
Top View

表 6-1. Pin Functions: TLV9041 and TLV9041U

PIN					I/O	DESCRIPTION
NAME	NO.					
	TLV9041			TLV9041U		
	SOT-23	SC70	X2SON	SOT-23		
IN –	4	3	2	3	I	Inverting input
IN+	3	1	4	1	I	Noninverting input
OUT	1	4	1	4	O	Output
V –	2	2	3	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	5	I	Positive (high) supply

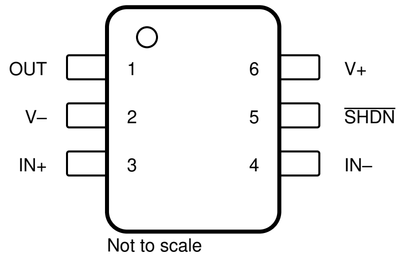


图 6-5. TLV9041S DBV Package 6-Pin SOT-23 Top View

表 6-2. Pin Functions: TLV9041S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	4	I	Inverting input
IN+	3	I	Noninverting input
OUT	1	O	Output
SHDN	5	I	Shutdown (low), enabled (high)
V–	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	6	I	Positive (high) supply

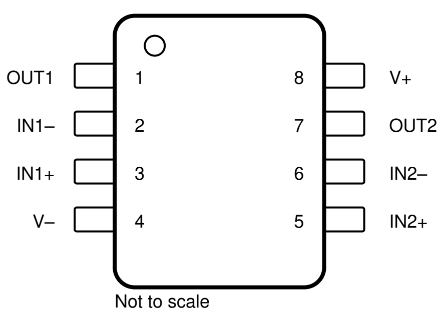
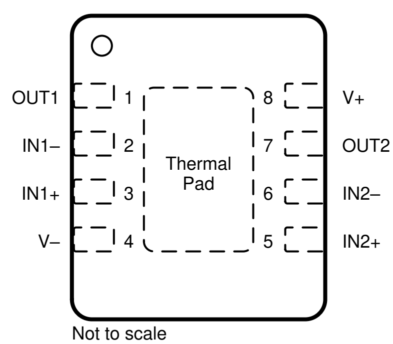


图 6-6. TLV9042 D, DDF, DGK, and PW Package 8-Pin SOIC, SOT-23 8, VSSOP, and TSSOP Top View



Connect exposed thermal pad to V–. See 节 8.3.11 for more information.

图 6-7. TLV9042 DSG Package 8-Pin WSON With Exposed Thermal Pad Top View

表 6-3. Pin Functions: TLV9042

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	I	Negative (low) supply or ground (for single-supply operation)

表 6-3. Pin Functions: TLV9042 (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
V+	8	I	Positive (high) supply

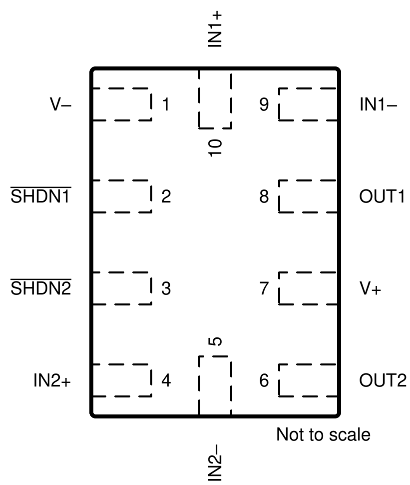


图 6-8. TLV9042S RUG Package
10-Pin X2QFN
Top View

表 6-4. Pin Functions: TLV9042S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 –	9	I	Inverting input, channel 1
IN1+	10	I	Noninverting input, channel 1
IN2 –	5	I	Inverting input, channel 2
IN2+	4	I	Noninverting input, channel 2
OUT1	8	O	Output, channel 1
OUT2	6	O	Output, channel 2
$\overline{SHDN1}$	2	I	Shutdown – low = disabled, high = enabled, channel 1
$\overline{SHDN2}$	3	I	Shutdown – low = disabled, high = enabled, channel 2
V –	1	I	Negative (low) supply or ground (for single-supply operation)
V+	7	I	Positive (high) supply

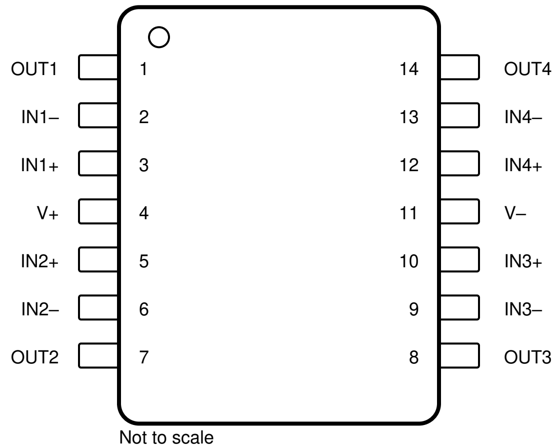


图 6-9. TLV9044 D, PW and DYY Packages 14-Pin SOIC, TSSOP and SOT-23 Top View

表 6-5. Pin Functions: TLV9044

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 –	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 –	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
IN3 –	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4 –	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
NC	—	—	No internal connection
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V –	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	I	Positive (high) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)		0	6.0	V
Signal input pins	Common-mode voltage (2)	(V–) – 0.5	(V+) + 0.5	V
	Differential voltage (2)		V_S + 0.2	V
	Current (2)	–10	10	mA
Output short-circuit (3)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	1.2	5.5	V
V_I	Input voltage range	(V–)	(V+)	V
T_A	Specified temperature	–40	125	°C

7.4 Thermal Information for Single Channel

THERMAL METRIC (1)		TLV9041, TLV9041S				UNIT
		DBV (SOT-23)		DCK (SC70)	DPW (X2SON)	
		5 PINS	6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	235.4	214.6	233.8	478.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	135.1	134.2	130.7	219.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	103.2	95.6	79.7	345.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	75.6	73.8	51.6	32.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	102.7	95.3	79.1	343.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	192.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Information for Dual Channel

THERMAL METRIC (1)		TLV9042					TLV9042S	UNIT
		D (SOIC)	DDF (SOT-23-8)	DSG (WSON)	PW (TSSOP)	DGK (VSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	148.3	203.8	99.8	203.1	196.6	196.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.8	123.9	122.2	91.9	87.5	87.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.6	121.6	66.0	133.8	118.5	117.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.6	21.7	13.8	23.7	25.7	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.9	199.6	65.9	132.1	116.8	117.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	41.9	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 Thermal Information for Quad Channel

THERMAL METRIC (1)		TLV9044, TLV9044S			UNIT
		D (SOIC)	PW (TSSOP)	DYY (SOT-23-14)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	135.7	152.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.5	78.8	86.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.4	63.9	67.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.8	14.2	10.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72	78.3	67.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.7 Electrical Characteristics

For V_S = (V+) – (V–) = 1.2 V to 5.5 V (±0.6 V to ±2.75 V) at T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.6	±2.25	mV
			T_A = –40°C to 125°C			±2.5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±0.8		μV/℃
PSRR	Input offset voltage versus power supply	V_S = ±0.6 V to ±2.75 V , V_{CM} = V–			±20	±100	μV/V
	Channel separation	f = 10 kHz			±5.6		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current (1)				±1	±12	pA
I_{OS}	Input offset current (1)				±0.5	±10	pA
NOISE							
E_N	Input voltage noise	f = 0.1 to 10 Hz			6.5		μV_{PP}
e_N	Input voltage noise density	f = 100 Hz			85		nV/√Hz
		f = 1 kHz			66		
		f = 10 kHz			64		
i_N	Input current noise (2)	f = 1 kHz			20		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			(V–)		(V+)	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 0.7 V, V_S = 1.2 V	T_A = –40°C to 125°C	60	77		dB
		(V–) < V_{CM} < (V+) – 0.7 V, V_S = 5.5 V		75	89		
		(V–) < V_{CM} < (V+), V_S = 1.2 V			60		
		(V–) < V_{CM} < (V+), V_S = 5.5 V		57	72		
INPUT IMPEDANCE							
Z_{ID}	Differential				80 || 1.4		GΩ || pF
Z_{ICM}	Common-mode				100 || 0.5		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 1.2 V, (V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ to V_S / 2	T_A = –40°C to 125°C		98		dB
		V_S = 5.5 V, (V–) + 0.2 V < V_O < (V+) – 0.2 V, R_L = 10 kΩ to V_S / 2			125		
		V_S = 1.2 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 100 kΩ to V_S / 2			105		
		V_S = 5.5 V, (V–) + 0.1 V < V_O < (V+) – 0.1 V, R_L = 100 kΩ to V_S / 2		107	130		
FREQUENCY RESPONSE							
THD+N	Total harmonic distortion + noise (3)	V_S = 5.5 V, V_{CM} = 2.75 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz, R_L = 100 kΩ to V_S / 2			0.013		%
GBW	Gain-bandwidth product	R_L = 1 MΩ connected to V_S/2			350		kHz
SR	Slew rate	V_S = 5.5 V, G = +1, C_L = 10 pF			0.2		V/μs
t_S	Settling time	To 0.1%, V_S = 5.5 V, V_{STEP} = 4 V, G = +1, C_L = 10 pF			25		μs
		To 0.1%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, C_L = 10 pF			22		
		To 0.01%, V_S = 5.5 V, V_{STEP} = 4 V, G = +1, C_L = 10 pF			35		
		To 0.01%, V_S = 5.5 V, V_{STEP} = 2 V, G = +1, C_L = 10 pF			30		
	Phase margin	G = +1, R_L = 100 kΩ connected to V_S/2, C_L = 10 pF			65		°
	Overload recovery time	V_{IN} × gain > V_S			13		μs

7.7 Electrical Characteristics (continued)

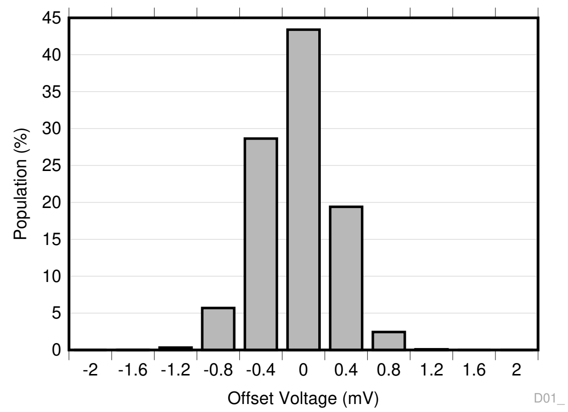
For V_S = (V+) – (V–) = 1.2 V to 5.5 V (±0.6 V to ±2.75 V) at T_A = 25°C, R_L = 100 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
EMIRR	Electro-magnetic interference rejection ratio	f = 1 GHz, V_{IN_EMIRR} = 100 mV			70		dB
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	V_S = 1.2 V, R_L = 100 kΩ to V_S / 2		0.75	7	mV
			V_S = 5.5 V, R_L = 10 kΩ to V_S / 2		10	21	mV
			V_S = 5.5 V, R_L = 100 kΩ to V_S / 2		1	8	mV
		Negative rail headroom	V_S = 1.2 V, R_L = 100 kΩ to V_S / 2		0.75	5	mV
			V_S = 5.5 V, R_L = 10 kΩ to V_S / 2		10	21	mV
			V_S = 5.5 V, R_L = 100 kΩ to V_S / 2		1	8	mV
I_{SC}	Short-circuit current (4)	V_S = 5.5 V			±40		mA
Z_O	Open-loop output impedance	f = 10 kHz			7500		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 A			10	13	µA
			T_A = –40°C to 125°C			13.5	µA
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 A, For TLV9041UIDBVR Only			10	13.5	µA
			T_A = –40°C to 125°C			14	µA
SHUTDOWN							
I_{QSD}	Quiescent current per amplifier	All amplifiers disabled, $\overline{SHDN}$ = V–			75	200	nA
Z_{SHDN}	Output impedance during shutdown	Amplifier disabled			43 ‖ 11.5		GΩ ‖ pF
V_{IH}	Logic high threshold voltage (amplifier enabled)			(V–) + 1 V			V
V_{IL}	Logic low threshold voltage (amplifier disabled)					(V–) + 0.2 V	V
t_{ON}	Amplifier enable time (full shutdown) (5) (6)	G = +1, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–			160		µs
	Amplifier enable time (partial shutdown) (5) (6)	G = +1, V_{CM} = V_S / 2, V_O = 0.9 × V_S / 2, R_L connected to V–			120		µs
t_{OFF}	Amplifier disable time (5)	G = +1, V_{CM} = V_S / 2, V_O = 0.1 × V_S / 2, R_L connected to V–			10		µs
	$\overline{SHDN}$ pin input bias current (per pin)	(V+) ≥ $\overline{SHDN}$ ≥ (V–) + 1 V			100		pA
		(V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.2 V			50		pA

(1) Max I_B and I_{OS} limits are specified based on characterization results. Input differential voltages greater than 2.5V can cause increased I_B
(2) Typical input current noise data is specified based on design simulation results
(3) Third-order filter; bandwidth = 80 kHz at –3 dB.
(4) Short circuit current is average of sourcing and sinking short circuit currents
(5) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(6) Full shutdown refers to the dual TLV9042S having both channels 1 and 2 disabled ($\overline{SHDN1}$ = $\overline{SHDN2}$ = V–) and the quad TLV9044S having all channels 1 to 4 disabled ($\overline{SHDN12}$ = $\overline{SHDN34}$ = V–). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in this mode, the internal biasing circuitry remains operational and the enable time is shorter.

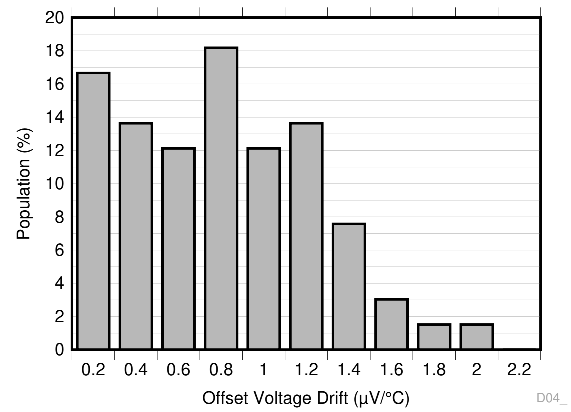
7.8 Typical Characteristics

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



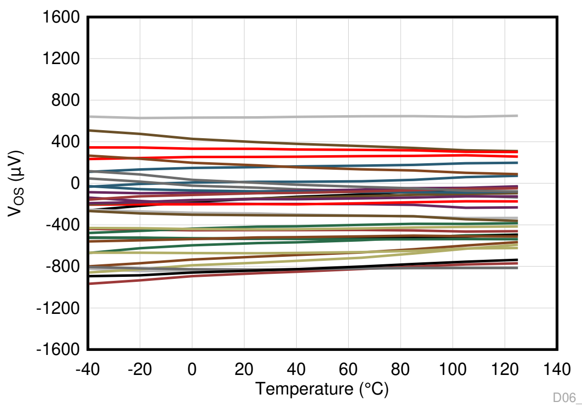
V_S = 5.5 V

图 7-1. Offset Voltage Distribution Histogram



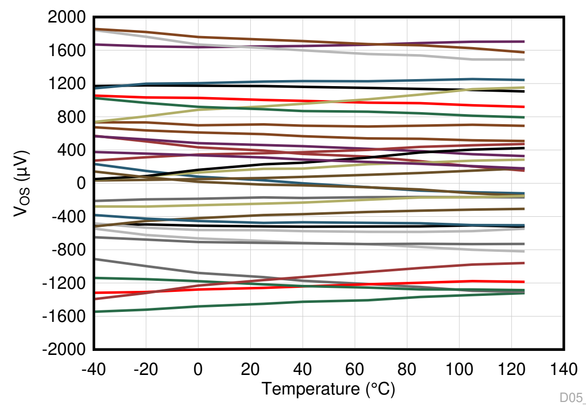
V_S = 5.5 V, T_A = –40°C to +125°C

图 7-2. Offset Voltage Drift Distribution Histogram



V_S = 5.5 V, V_{CM} = V–

图 7-3. Input Offset Voltage vs Temperature



V_S = 5.5 V, V_{CM} = V+

图 7-4. Input Offset Voltage vs Temperature

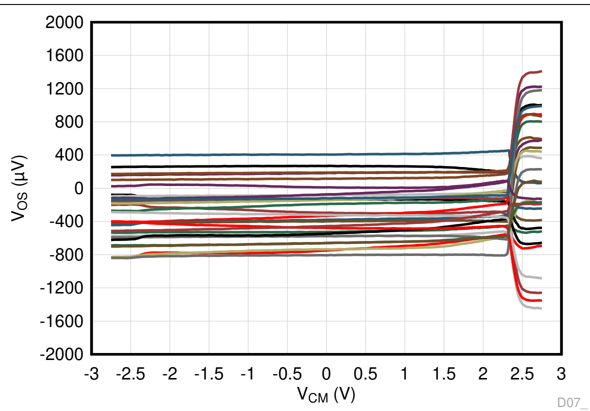
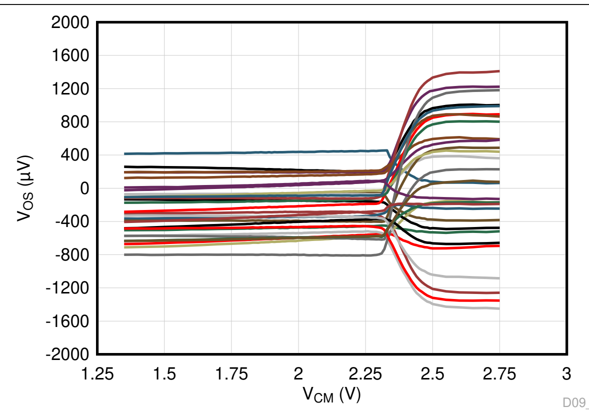


图 7-5. Offset Voltage vs Common-Mode

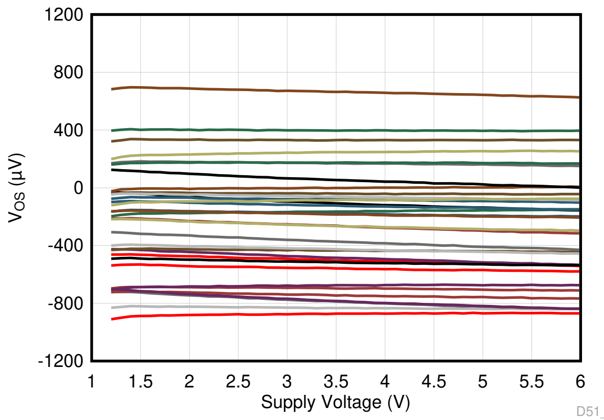


V_{CM} > (V+) – 1.4 V

图 7-6. Offset Voltage vs Common-Mode

7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_{CM} = (V–)

图 7-7. Offset Voltage vs Supply Voltage

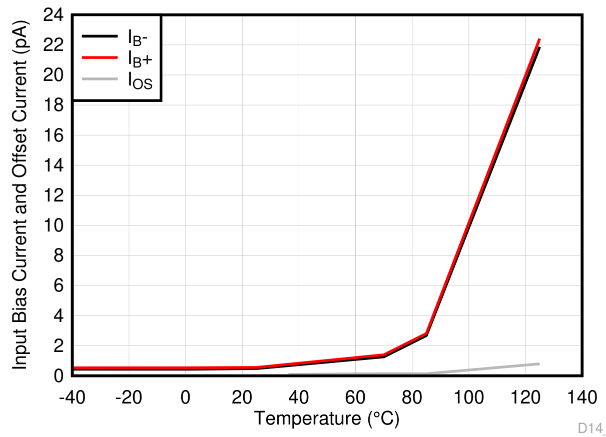


图 7-8. I_B and I_{OS} vs Temperature

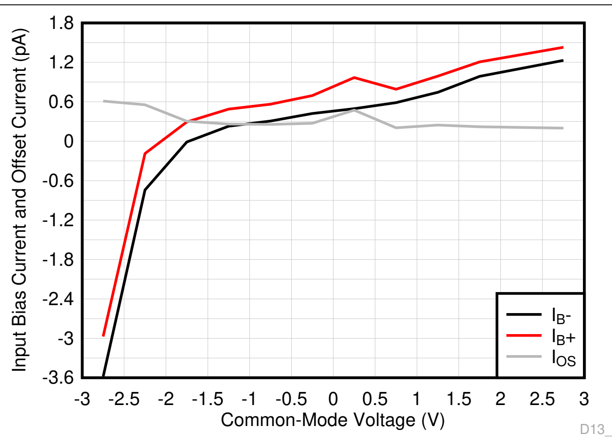


图 7-9. I_B and I_{OS} vs Common-Mode Voltage

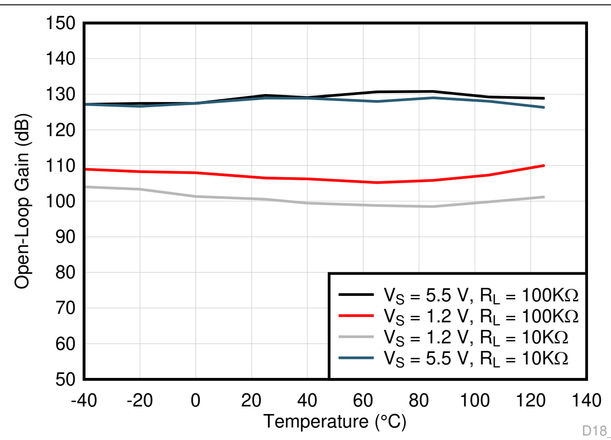
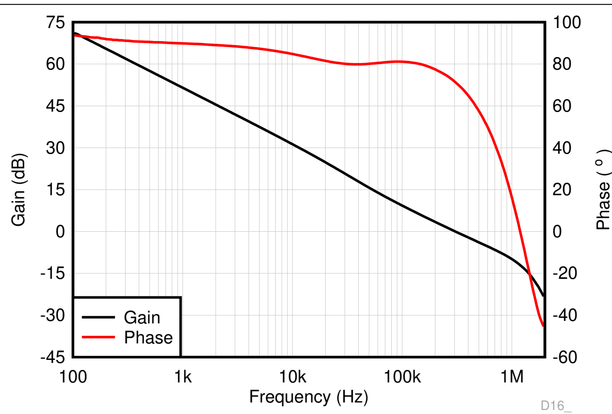


图 7-10. Open-Loop Gain vs Temperature



C_L = 10 pF

图 7-11. Open-Loop Gain and Phase vs Frequency

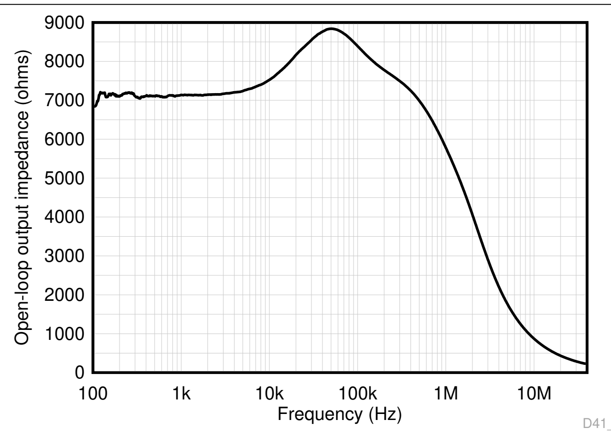
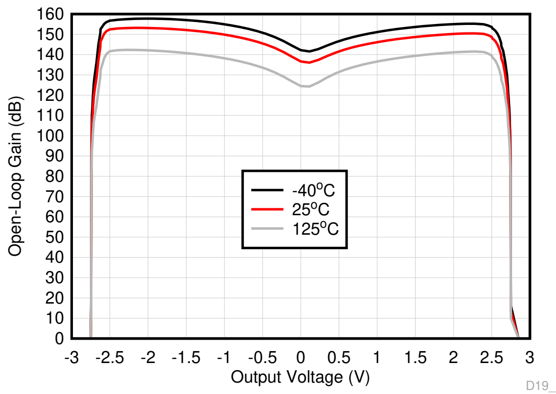


图 7-12. Open-Loop Output Impedance vs Frequency

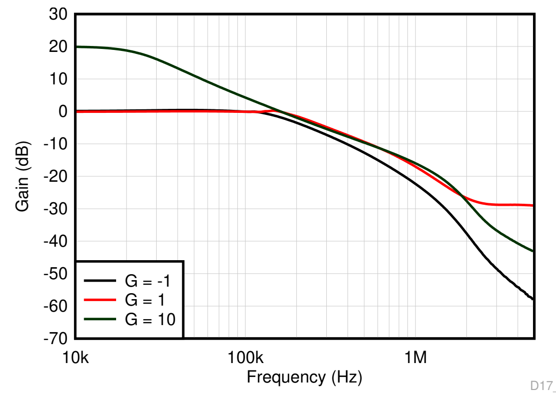
7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



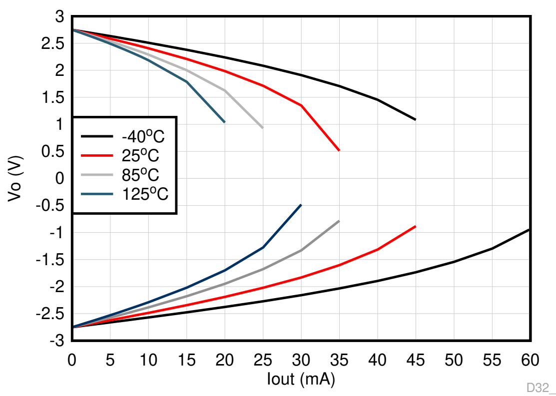
V+ = 2.75 V, V– = –2.75 V R_L = 10 kΩ

图 7-13. Open-Loop Gain vs Output Voltage



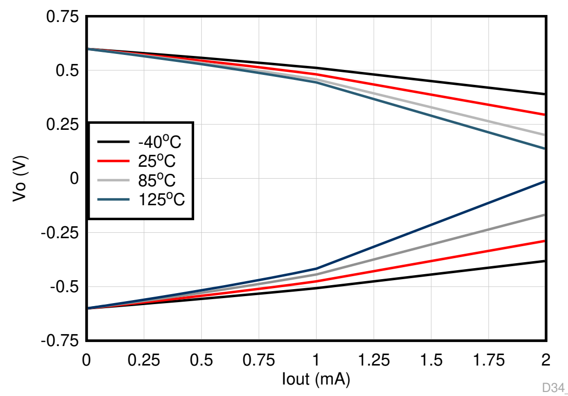
C_L = 10 pF

图 7-14. Closed-Loop Gain vs Frequency



V+ = 2.75 V, V– = –2.75 V

图 7-15. Output Voltage vs Output Current (Claw)



V+ = 0.6 V, V– = –0.6 V

图 7-16. Output Voltage vs Output Current (Claw)

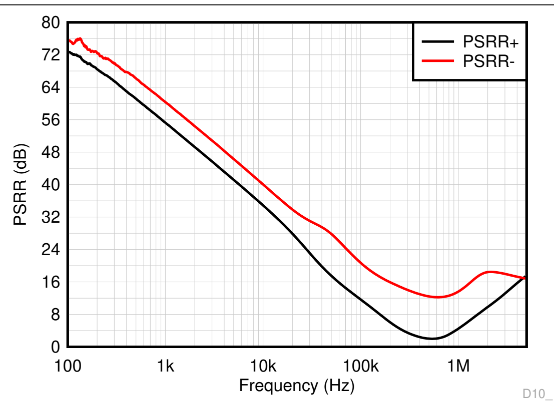
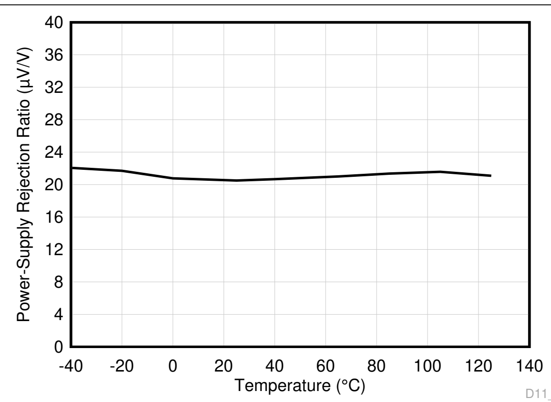


图 7-17. PSRR vs Frequency



V_S = 1.2 V to 5.5 V

图 7-18. DC PSRR vs Temperature

7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

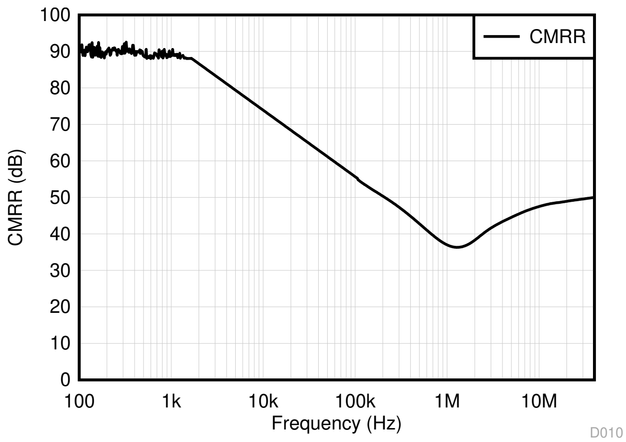


图 7-19. CMRR vs Frequency

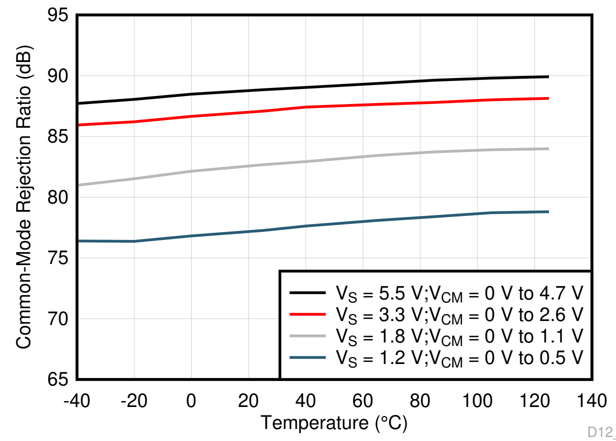


图 7-20. DC CMRR vs Temperature

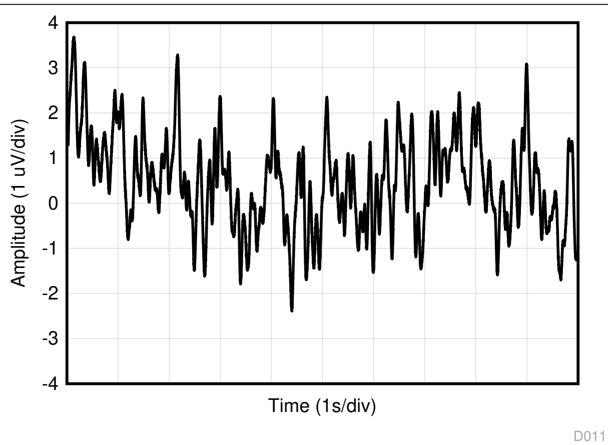


图 7-21. 0.1 Hz to 10 Hz Voltage Noise in Time Domain

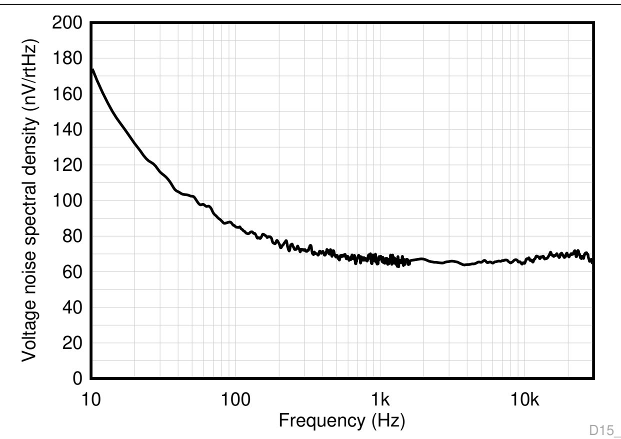
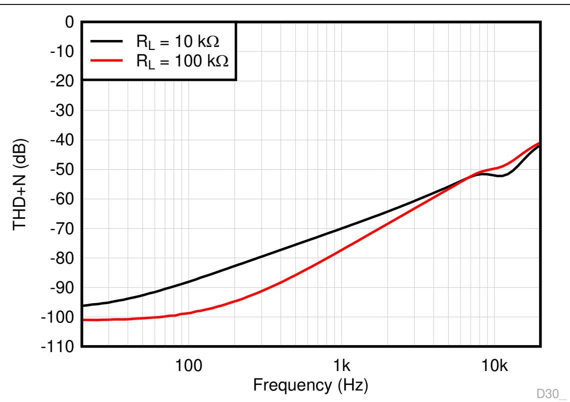


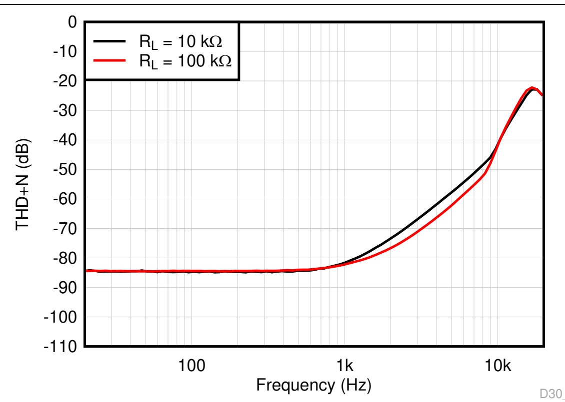
图 7-22. Input Voltage Noise Spectral Density



V_S = 5.5 V　V_{CM} = 2.5 V　G = 1

BW = 80 kHz　V_{OUT} = 0.5 V_{RMS}

图 7-23. THD + N vs Frequency



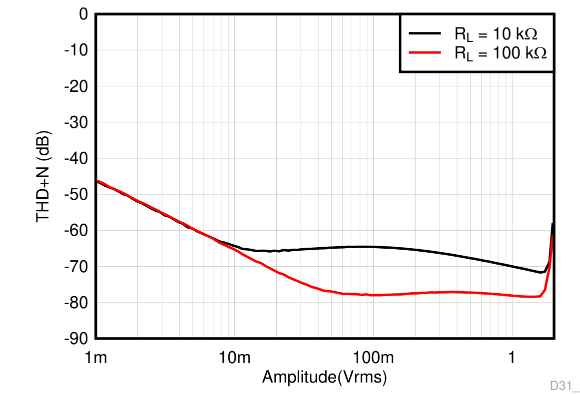
V_S = 5.5 V　V_{CM} = 2.5 V　G = –1

BW = 80 kHz　V_{OUT} = 0.5 V_{RMS}

图 7-24. THD + N vs Frequency

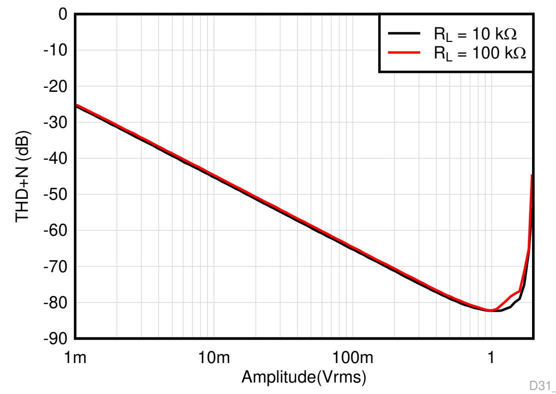
7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



V_S = 5.5 V　V_{CM} = 2.5 V　f = 1 kHz
G = 1　BW = 80 kHz

图 7-25. THD + N vs Amplitude



V_S = 5.5 V　V_{CM} = 2.5 V　f = 1 kHz
G = –1　BW = 80 kHz

图 7-26. THD + N vs Amplitude

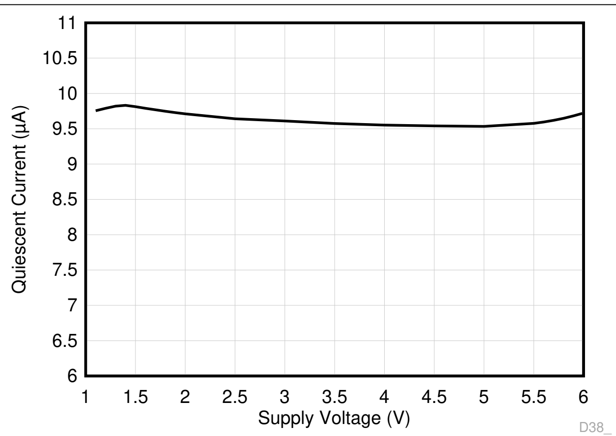


图 7-27. Quiescent Current vs Supply Voltage

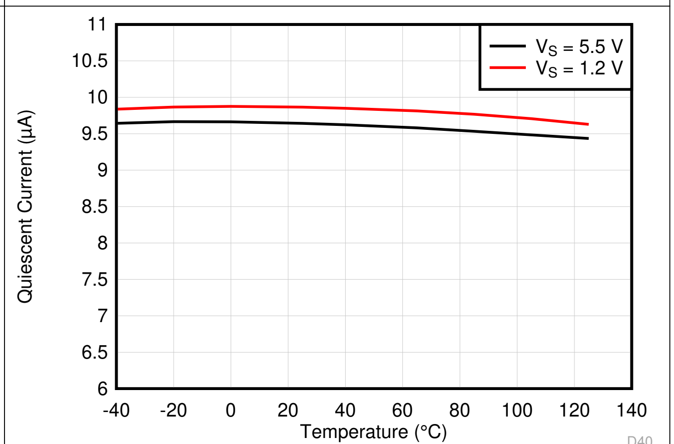
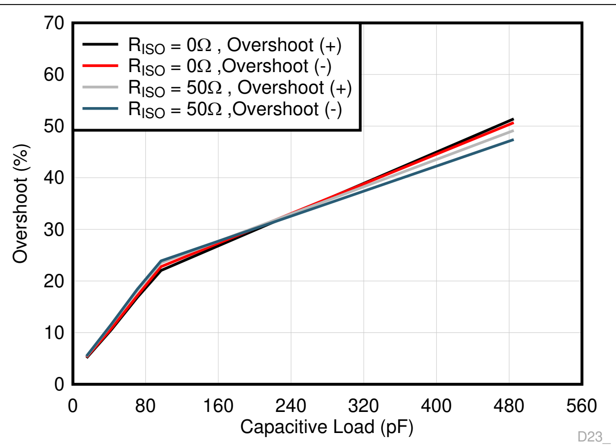
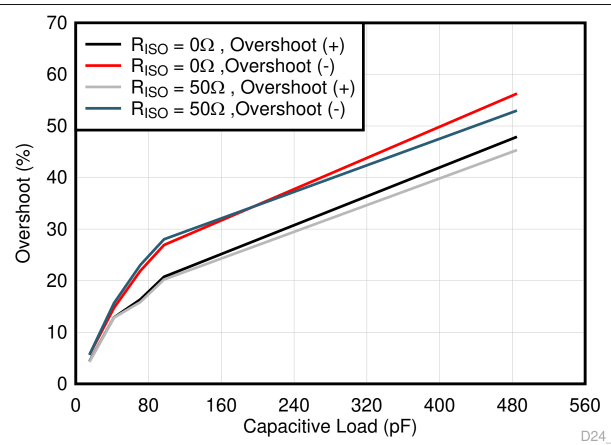


图 7-28. Quiescent Current vs Temperature



G = 1　V_{IN} = 100 mVpp

图 7-29. Small Signal Overshoot vs Capacitive Load



G = –1　V_{IN} = 100 mVpp

图 7-30. Small Signal Overshoot vs Capacitive Load

7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

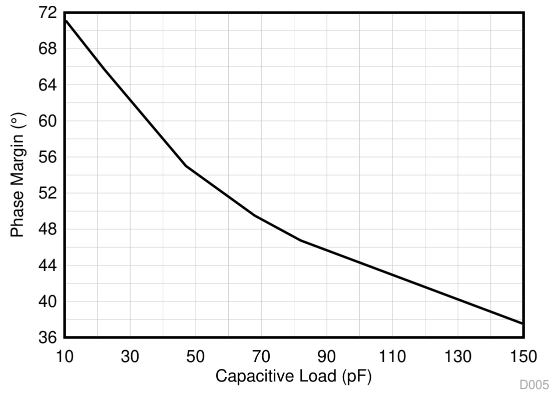
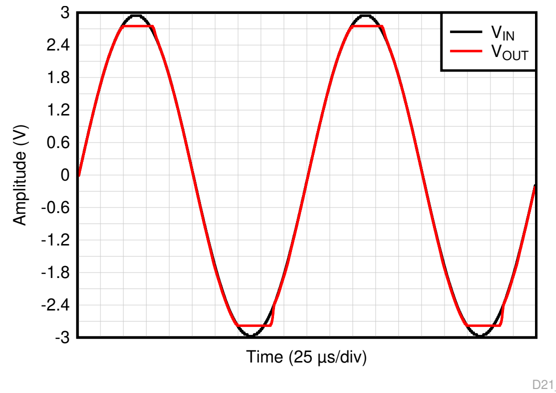
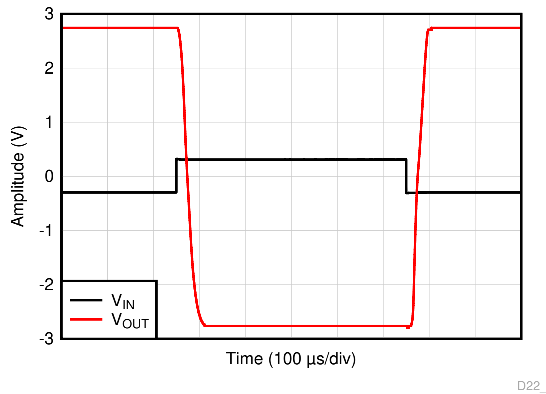


图 7-31. Phase Margin vs Capacitive Load



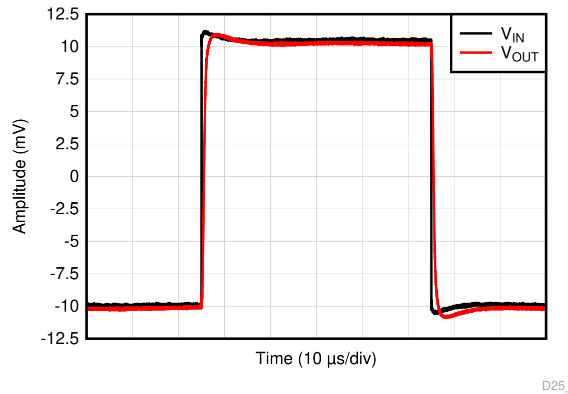
G = 1 V_{IN} = 6 V_{PP}

图 7-32. No Phase Reversal



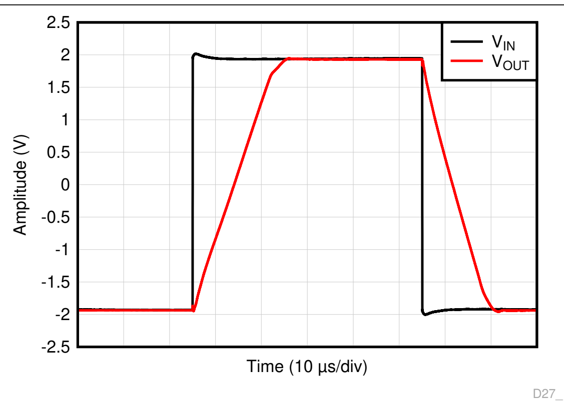
G = –10 V_{IN} = 600 mV_{PP}

图 7-33. Overload Recovery



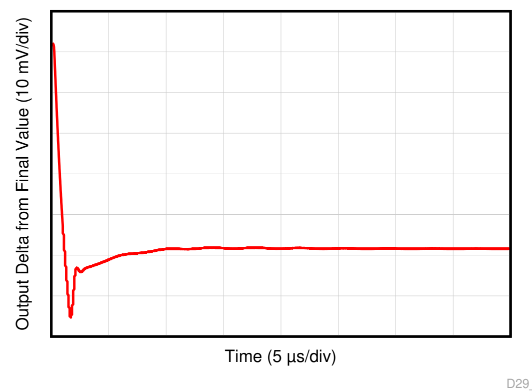
G = 1 V_{IN} = 20 mV_{PP} C_L = 10 pF

图 7-34. Small-Signal Step Response



G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

图 7-35. Large-Signal Step Response

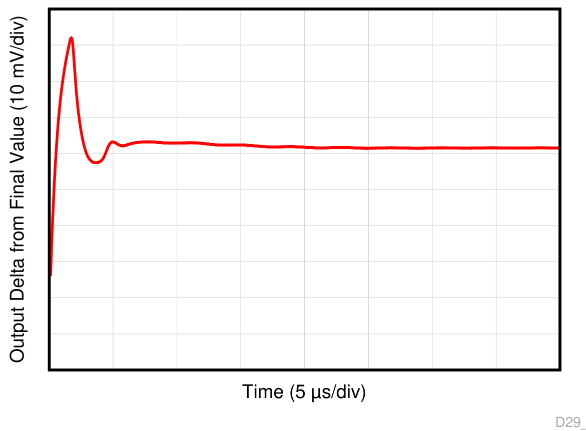


G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

图 7-36. Large-Signal Settling Time (Negative)

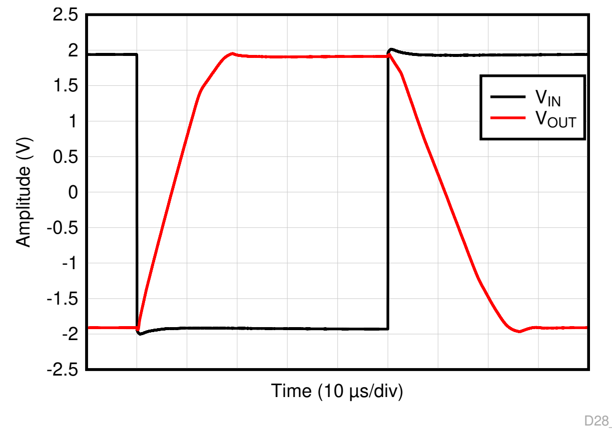
7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = 1 V_{IN} = 4 V_{PP} C_L = 10 pF

图 7-37. Large-Signal Settling Time (Positive)



G = –1 V_{IN} = 4 V_{PP} C_L = 10 pF

图 7-38. Large-Signal Step Response

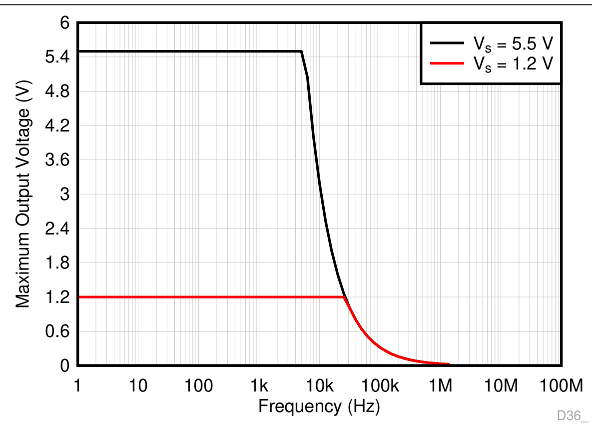


图 7-39. Maximum Output Voltage vs Frequency

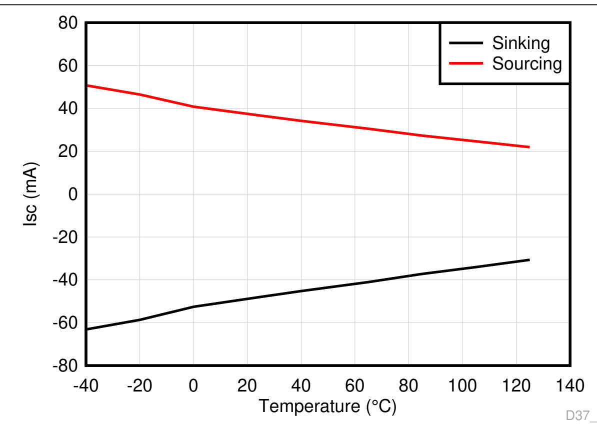


图 7-40. Short-Circuit Current vs Temperature

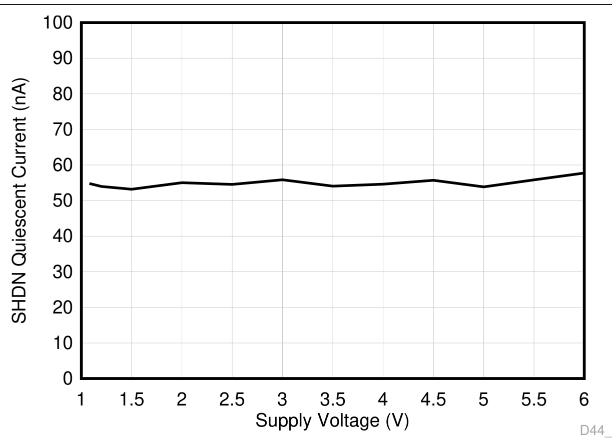


图 7-41. Shutdown Mode Quiescent Current vs Supply Voltage

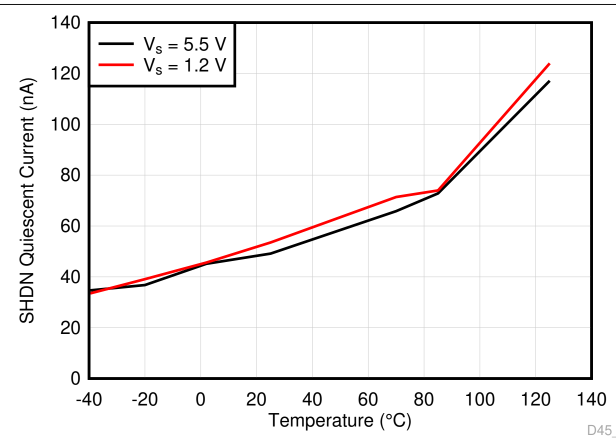


图 7-42. Shutdown Mode Quiescent Current vs Temperature

7.8 Typical Characteristics (continued)

at T_A = 25°C, V+ = 2.75 V, V– = –2.75 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

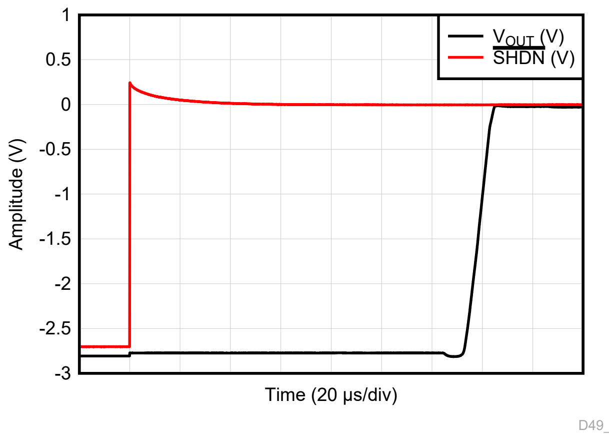


图 7-43. Amplifier Enable Response

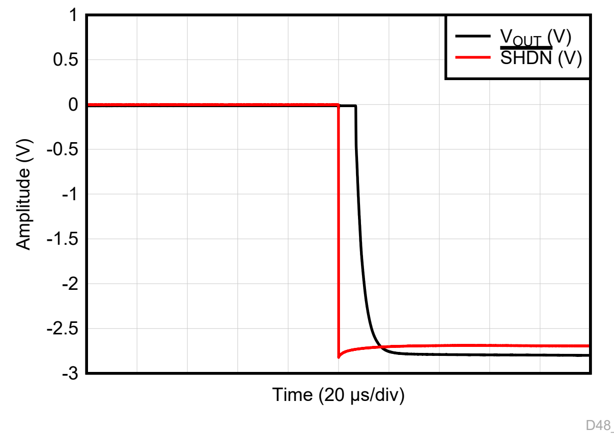


图 7-44. Amplifier Disable Response

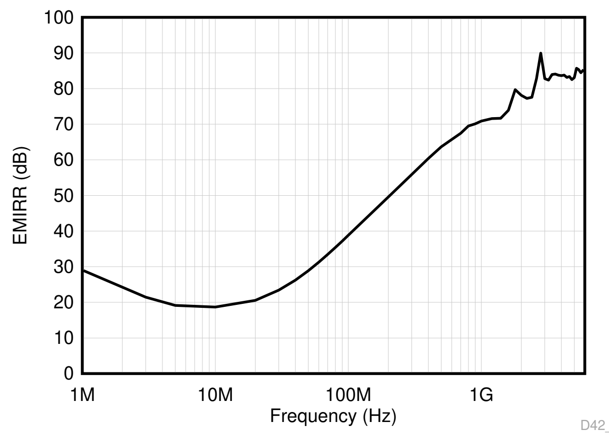


图 7-45. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

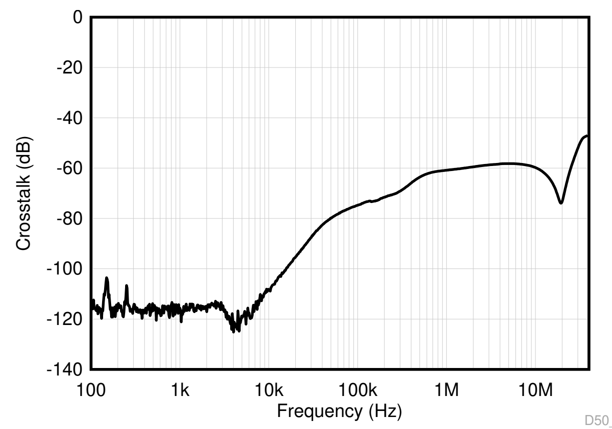


图 7-46. Channel Separation

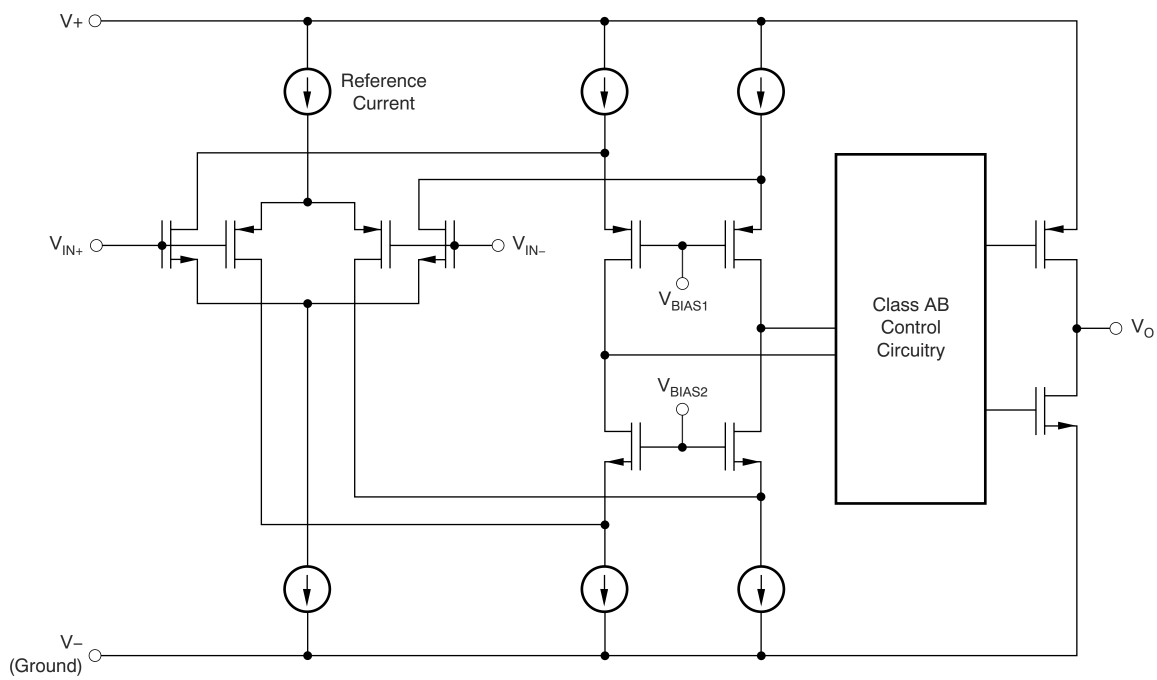
8 Detailed Description

8.1 Overview

The TLV904x is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for battery powered applications. This family of amplifiers utilizes unique transistors that enable operation from ultra low supply voltage of 1.2 V to a standard supply voltage of 5.5 V. These unity-gain stable amplifiers provide 350 kHz of GBW with an I_Q of only 10 µA. TLV904x also has short circuit current capability of 40 mA at 5.5 V. This combination of low voltage, low IQ, and high output current capability makes this device quite unique and suitable for suitable for a wide range of general-purpose applications. The input common-mode voltage range includes both rails, and allows the TLV904x series to be used in many single-supply or dual supply configurations. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices ideal for driving low speed sampling analog-to-digital converters (ADCs). Further, the class AB output stage is capable of driving resitive loads greater than 2-kΩ connected to any point between V+ and ground.

The TLV904x can drive up to 100 pF with a typical phase margin of 45° and features 350-kHz gain bandwidth product, 0.2-V/µs slew rate with 6.5-µV_{p-p} integrated noise (0.1 to 10 Hz) while consuming only 10-µA supply current per channel, thus providing a good AC performance at a very low power consumption. DC applications are also well served with a low input bias current of 1 pA (typical), an input offset voltage of 0.6 mV (typical) and a good PSRR, CMRR, and A_{OL}.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV904x series of operational amplifiers is fully specified and ensured for operation from 1.2 V to 5.5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are provided in 节 7.8. It is highly recommended to bypass power-supply pins with at least 0.01-µF ceramic capacitors.

8.3.2 Rail-to-Rail Input

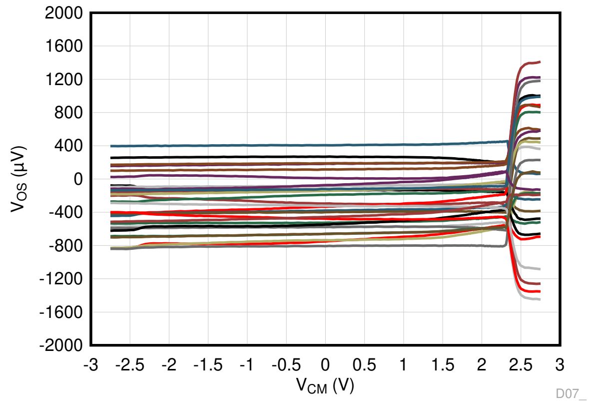
The input common-mode voltage range of the TLV904x series extends to either supply rails. This is true even when operating at the ultra-low supply voltage of 1.2 V, all the way up to the standard supply voltage of 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair. Refer to 节 8.2 for more details.

For most amplifiers with a complementary input stage, one of the input pairs, usually the P-channel input pair, is designed to deliver slightly better performance in terms of input offset voltage, offset drift over the N-channel pair. Consequently, the P-channel pair is designed to cover the majority of the common mode range with the N-channel pair slated to slowly take over at a certain threshold voltage from the positive rail. Just after the threshold voltage, both the input pairs are in operation for a small range referred to as the transition region. Beyond this region, the N-channel pair completely takes over. Within the transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region. Hence, most applications generally prefer operating in the P-channel input range where the performance is slightly better.

For the TLV904x, the P-channel pair is typically active for input voltages from the negative rail to (V+) – 0.4 V and the N-channel pair is typically active for input voltages from the positive supply to (V+) – 0.4 V. The transition region occurs typically from (V+) – 0.5 V to (V+) – 0.3 V, in which both pairs are on. These voltage levels mentioned above can vary with process variations associated with threshold voltage of transistors. In the TLV904x, 200-mV transition region mentioned above can vary up to 200 mV in either direction. Thus, the transition region (both stages on) can range from (V+) – 0.7 V to (V+) – 0.5 V on the low end, up to (V+) – 0.3 V to (V+) – 0.1 V on the high end.

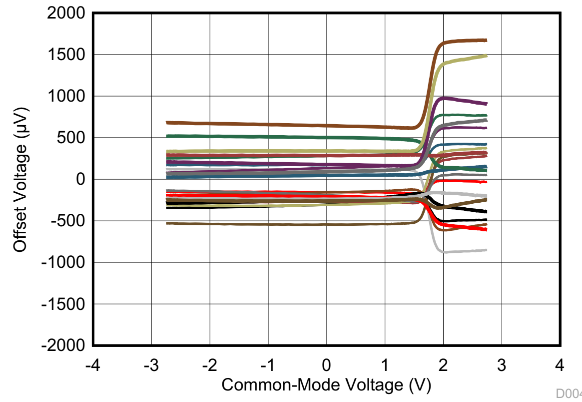
Recollecting the fact that a P-channel input pair usually offers better performance over a N-channel input pair, the TLV904x is designed to offer a much wider P-channel input pair range, in comparison to most complimentary input amplifiers in the industry. A side by side comparison of the TLV904x and the TLV900x is provided below. Note, that the TLV900x guarantees P-channel pair operation only until 1.4 V from the positive rail while the TLV904x guarantees P-channel pair operation all the way till 0.7 V from the positive rail. This additional 700mV of P-channel input pair range for the TLV904x is particularly useful when operating at lower supply voltages (1.2 V, 1.8 V etc) where the P-channel input range usually gets limited to a great extent.

Thus the wide common mode swing of input signal can be accommodated more easily within the P-channel input pair of the TLV904x, while likely avoiding the transition region, thereby maintaining linearity.



V+ = 2.75 V, V– = –2.75 V

图 8-1. TLV904x Offset Voltage vs Common-Mode



V+ = 2.75 V, V– = –2.75 V

图 8-2. TLV900x Offset Voltage vs Common-Mode

8.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the TLV904x delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 5 kΩ, the output typically swings to within 20 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 Common-Mode Rejection Ratio (CMRR)

The CMRR for the TLV904x is specified in several ways so the best match for a given application can be used; see the Electrical Characteristics table. First, the CMRR of the device in the common-mode range below the transition region [VCM < (V+) – 0.7 V] is given. This specification is the best indicator of the capability of the device when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (VCM = 0 V to 5.5 V). This last value includes the variations measured through the transition region.

8.3.5 Capacitive Load and Stability

The TLV904x is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLV904x can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the TLV904x remains stable with a pure capacitive load up to approximately 100 pF with a good phase margin of 45° typical. The equivalent series resistance (ESR) of some very large capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains.

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10 Ω to 20 Ω) in series with the output, as shown in 图 8-3. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

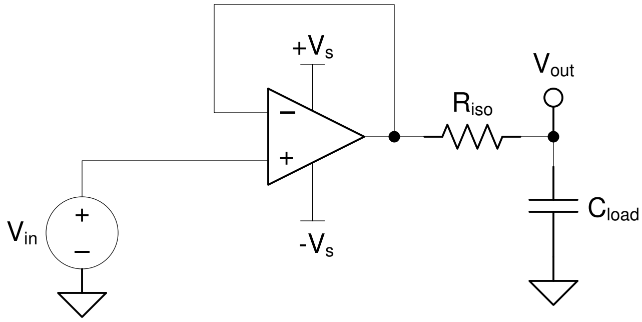


图 8-3. Improving Capacitive Load Drive

8.3.6 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. Once one of the output devices enters the saturation region, the output stage requires additional time to return to the linear operating state which is referred to as overload recovery time. After the output stage returns to its linear operating state, the amplifier begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV904x family is approximately 13-μs typical.

8.3.7 EMI Rejection

The TLV904x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV904x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 8-4 shows the results of this testing on the TLV904x. 表 8-1 shows the EMIRR IN+ values for the TLV904x at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

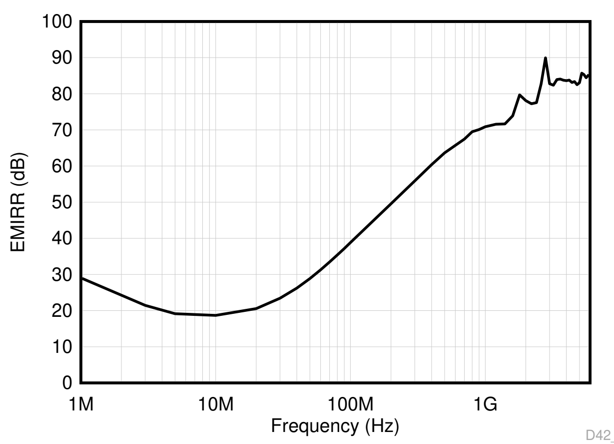


图 8-4. EMIRR Testing

表 8-1. TLV904x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	60 dB

表 8-1. TLV904x EMIRR IN+ for Frequencies of Interest (continued)

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	70 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	75 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	79.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	85 dB

8.3.8 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 8-5 shows the ESD circuits contained in the TLV904x devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

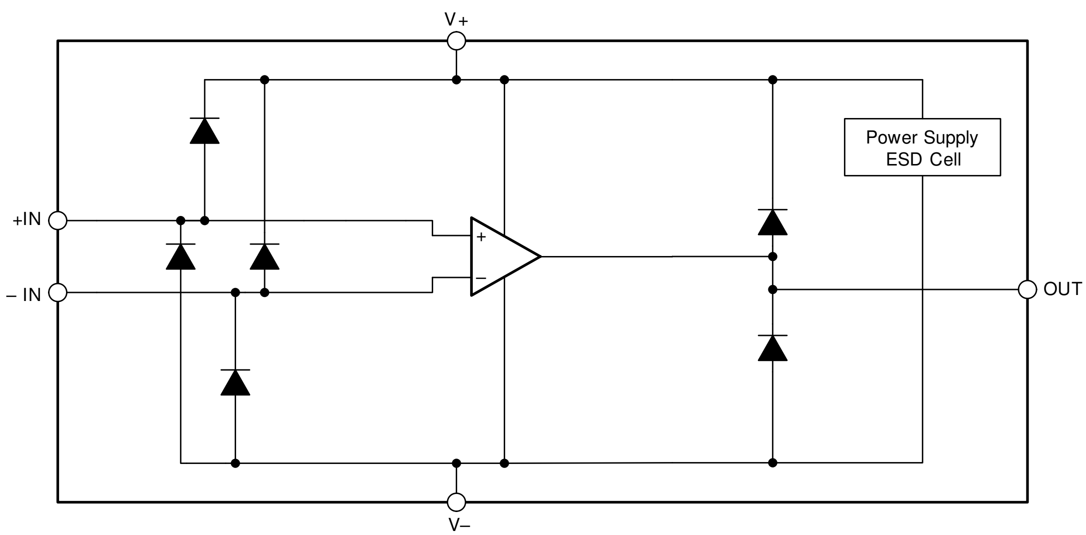


图 8-5. Equivalent Internal ESD Circuitry

8.3.9 Input and ESD Protection

The TLV904x family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA. 图 8-6 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

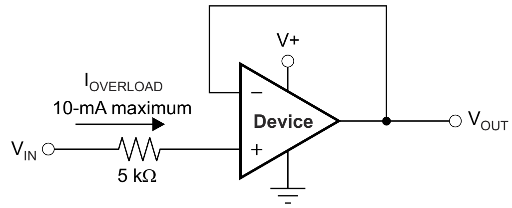


图 8-6. Input Current Protection

8.3.10 Shutdown Function

The TLV904xS devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 150 nA. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 500 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1 V and V+. To enable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. We highly recommend that the shutdown pin be connected to a valid high or a low voltage or driven. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5 V. Exceeding this voltage level will damage the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 160 µs for full shutdown of all channels; disable time is 10 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV904xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 100-kΩ load to midsupply (V_S / 2) is required. If using the TLV904xS without a load, the resulting turnoff time is significantly increased.

8.3.11 Packages With an Exposed Thermal Pad

The TLV904x family is available in packages such as the WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other then V– is not allowed, and the performance of the device is not assured when doing so.

8.4 Device Functional Modes

The TLV904x devices have a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.2 V (±0.6 V) and 5.5 V (±2.75 V).

The TLV904xS devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See 节 8.3.10 for more information.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TLV904x family of low-power, rail-to-rail input and output operational amplifiers is specifically designed for portable applications. The devices operate from 1.2 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving resitive loads greater than 2-kΩ connected to any point between V+ and V–. The input common-mode voltage range includes both rails and allows the TLV904x series to be used in many single-supply or dual supply configurations.

9.2 Typical Application

9.2.1 TLV904x Low-Side, Current Sensing Application

图 9-1 shows the TLV904x configured in a low-side current sensing application.

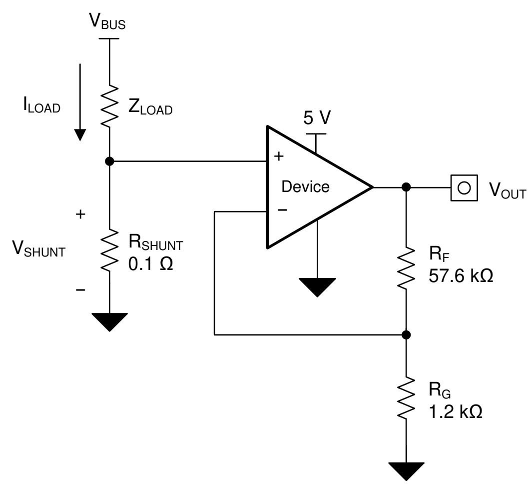


图 9-1. TLV904x in a Low-Side, Current-Sensing Application

9.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Maximum output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

9.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 图 9-1 is given in 方程式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is shown using 方程式 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100mV}{1A} = 100m\Omega \quad (2)$$

Using 方程式 2, R_{SHUNT} is calculated to be 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV904x to produce an output voltage of approximately 0 V to 4.9 V. The gain needed by the TLV904x to produce the necessary output voltage is calculated using 方程式 3.

$$Gain = \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \quad (3)$$

Using 方程式 3, the required gain is calculated to be 49 V/V, which is set with resistors R_F and R_G. 方程式 4 sizes the resistors R_F and R_G, to set the gain of the TLV904x to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F as 57.6 kΩ and R_G as 1.2 kΩ provides a combination that equals 49 V/V. 图 9-2 shows the measured transfer function of the circuit shown in 图 9-1. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistors values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system; you must choose an impedance that is ideal for your system parameters.

9.2.1.3 Application Curve

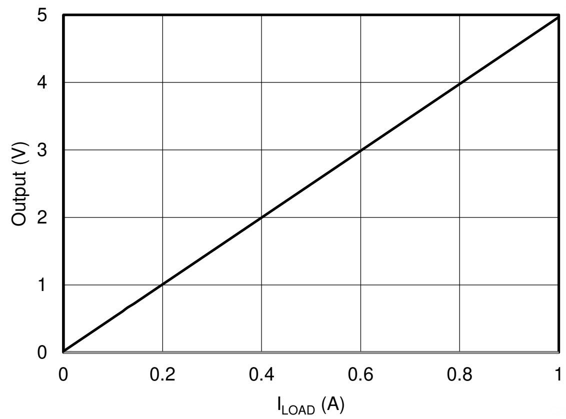


图 9-2. Low-Side, Current-Sense Transfer Function

10 Power Supply Recommendations

The TLV904x family is specified for operation from 1.2 V to 5.5 V (±0.6 V to ±2.75 V); many specifications apply from –40°C to 125°C. 节 7.7 presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V may permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-μF bypass capacitors close to the power-supply pins to reduce coupling errors from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see 节 11.1.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power connections of the board and propagate to the power pins of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing a low-impedance path to ground.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible, as shown in 图 11-2. Keeping R_F and R_G close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

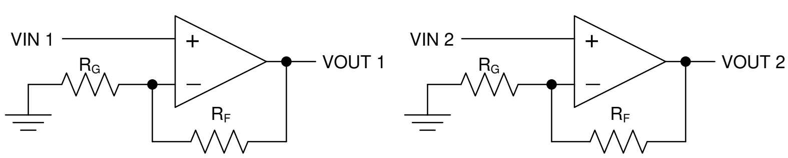


图 11-1. Schematic Representation

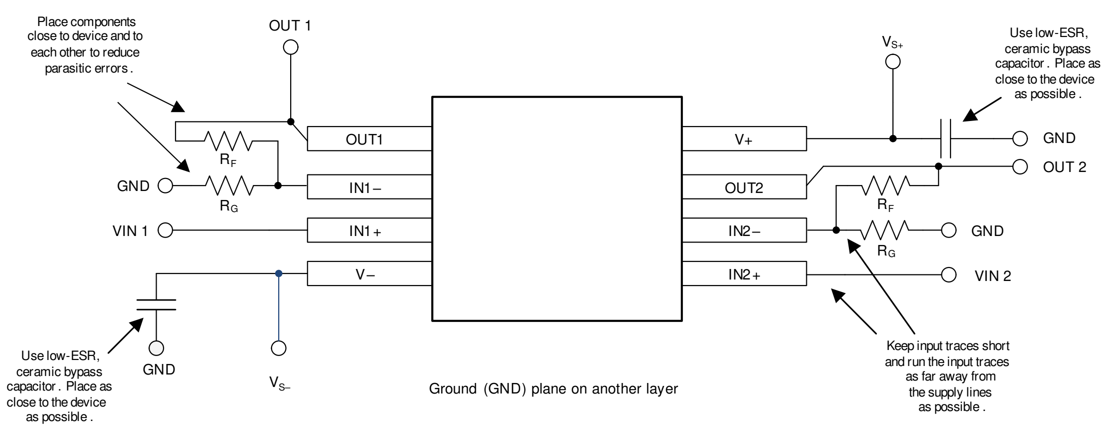


图 11-2. Layout Example

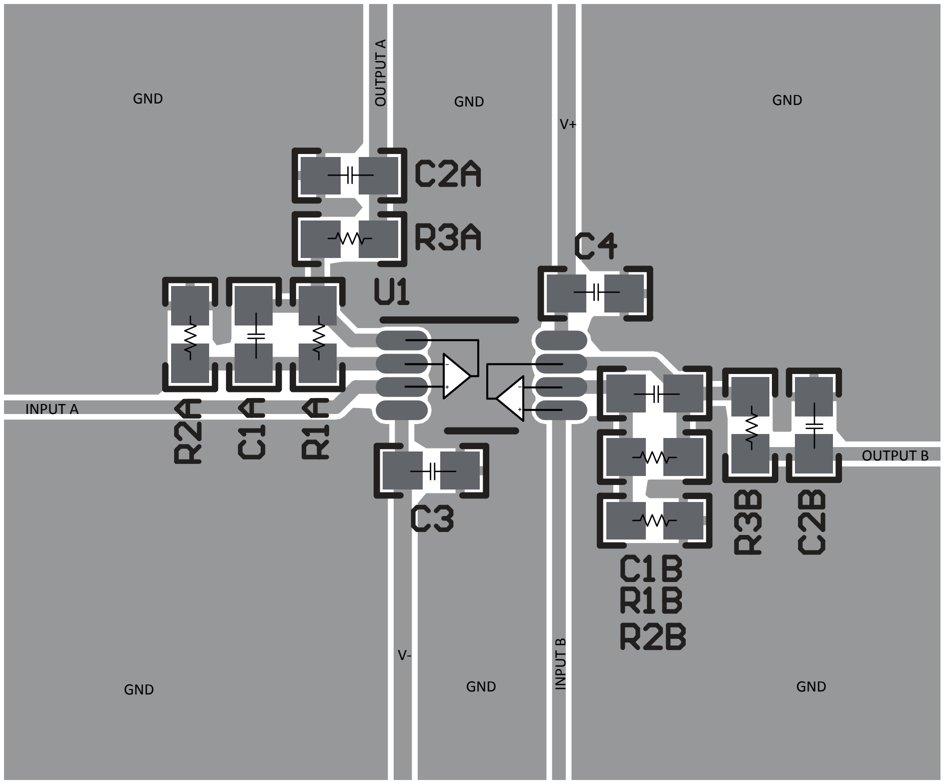


图 11-3. Example Layout for VSSOP-8 (DGK) Package

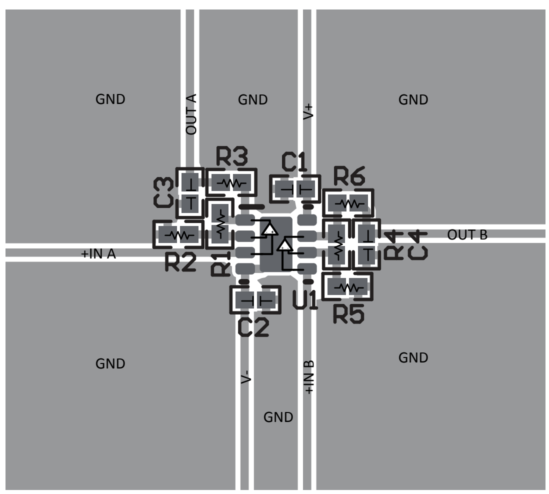


图 11-4. Example Layout for WSON-8 (DSG) Package

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *EMI rejection ratio of operational amplifiers*
- *QFN/SON PCB attachment*
- *Quad flatpack no-lead logic packages*

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTLV9041IDPWR	ACTIVE	X2SON	DPW	5	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TLV9041IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T041	Samples
TLV9041IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1IV	Samples
TLV9041IDPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(L, LE)	Samples
TLV9041SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41S	Samples
TLV9041UIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U041	Samples
TLV9042IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T042	Samples
TLV9042IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2H7T	Samples
TLV9042IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9042D	Samples
TLV9042IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42G	Samples
TLV9042IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9042P	Samples
TLV9042SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	HTF	Samples
TLV9044IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9044D	Samples
TLV9044IDYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL944DYY	Samples
TLV9044IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T9044PW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

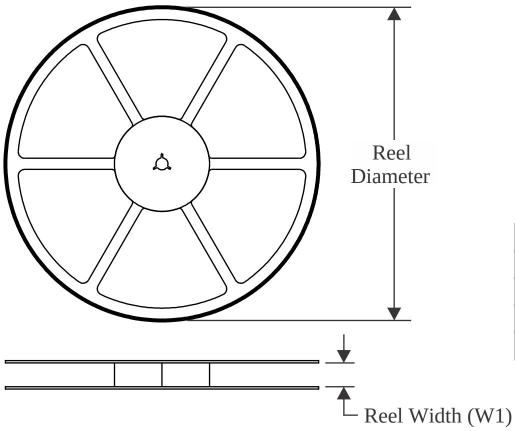
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

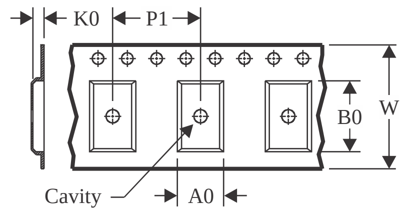
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

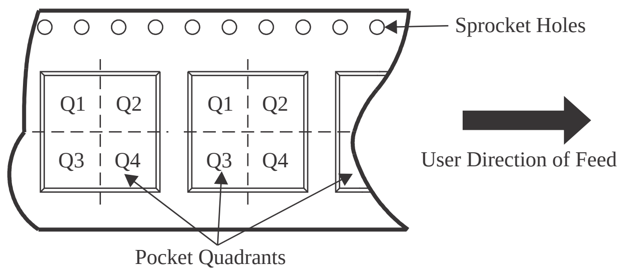


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

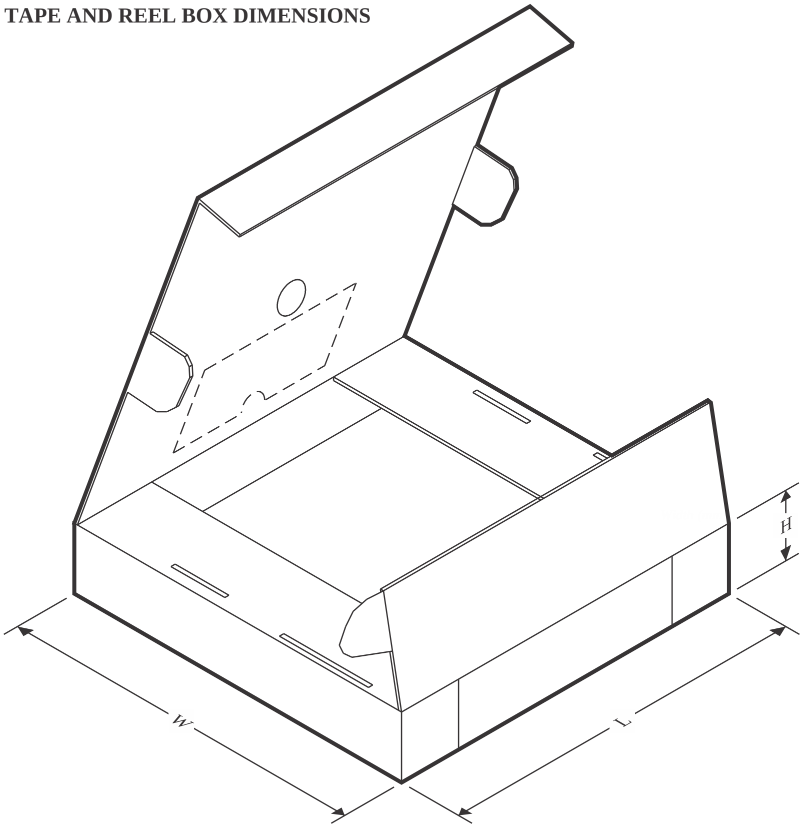
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

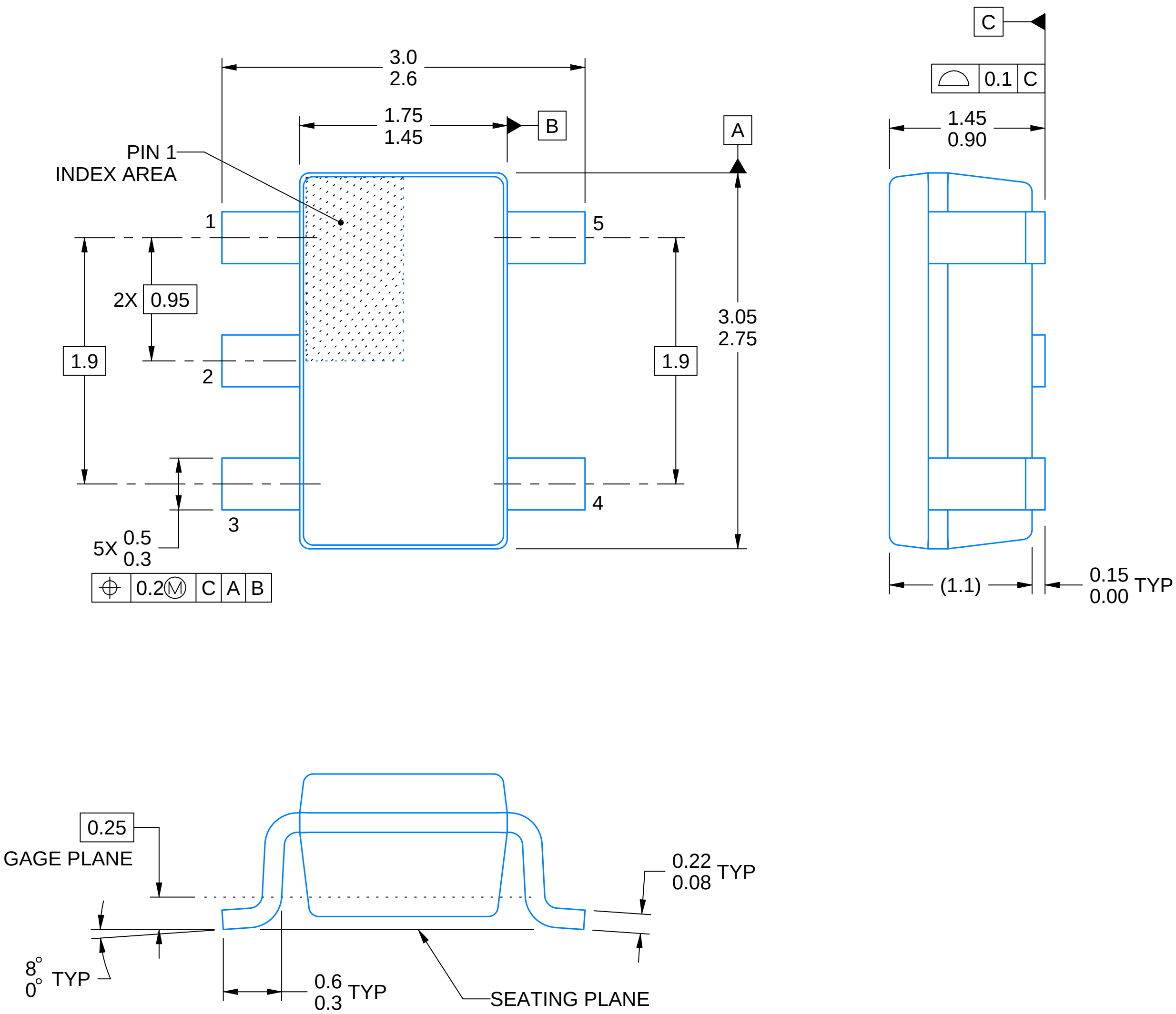
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9041IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9041IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9041IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9041IDPWR	X2SON	DPW	5	3000	180.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9041SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9042IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9042IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9042IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9042IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9042IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9042SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9044IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9044IDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TLV9044IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

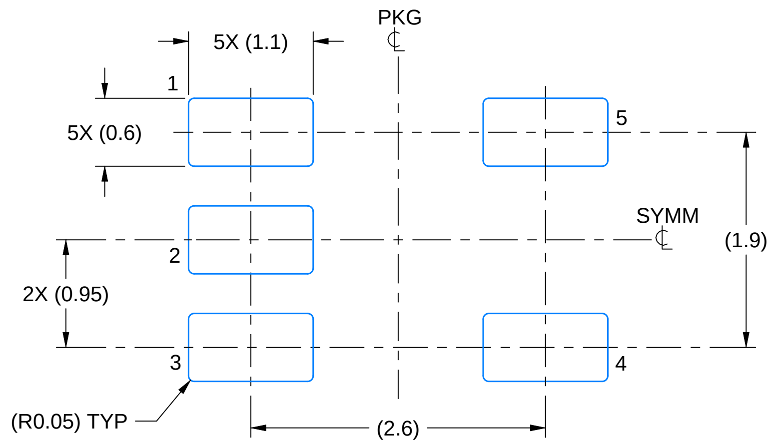
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9041IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9041IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TLV9041IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9041IDPWR	X2SON	DPW	5	3000	210.0	185.0	35.0
TLV9041SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9042IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9042IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9042IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV9042IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9042IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV9042SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9044IDR	SOIC	D	14	2500	356.0	356.0	35.0
TLV9044IDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TLV9044IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0



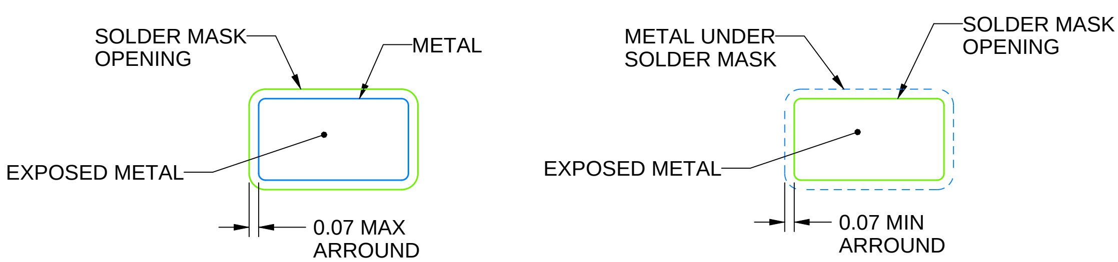
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

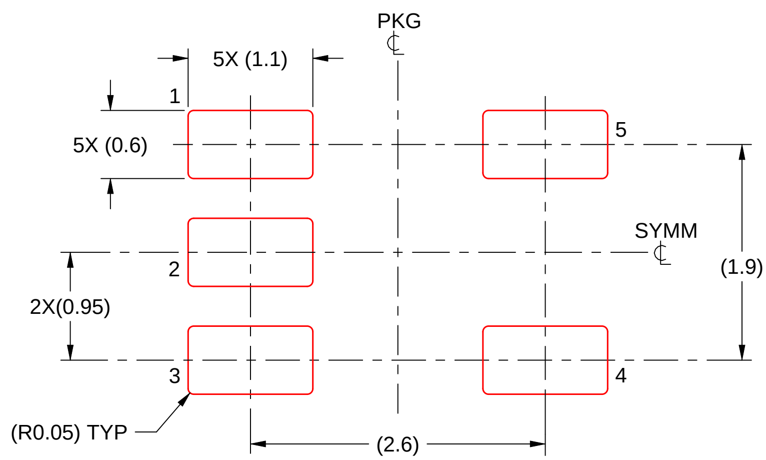
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



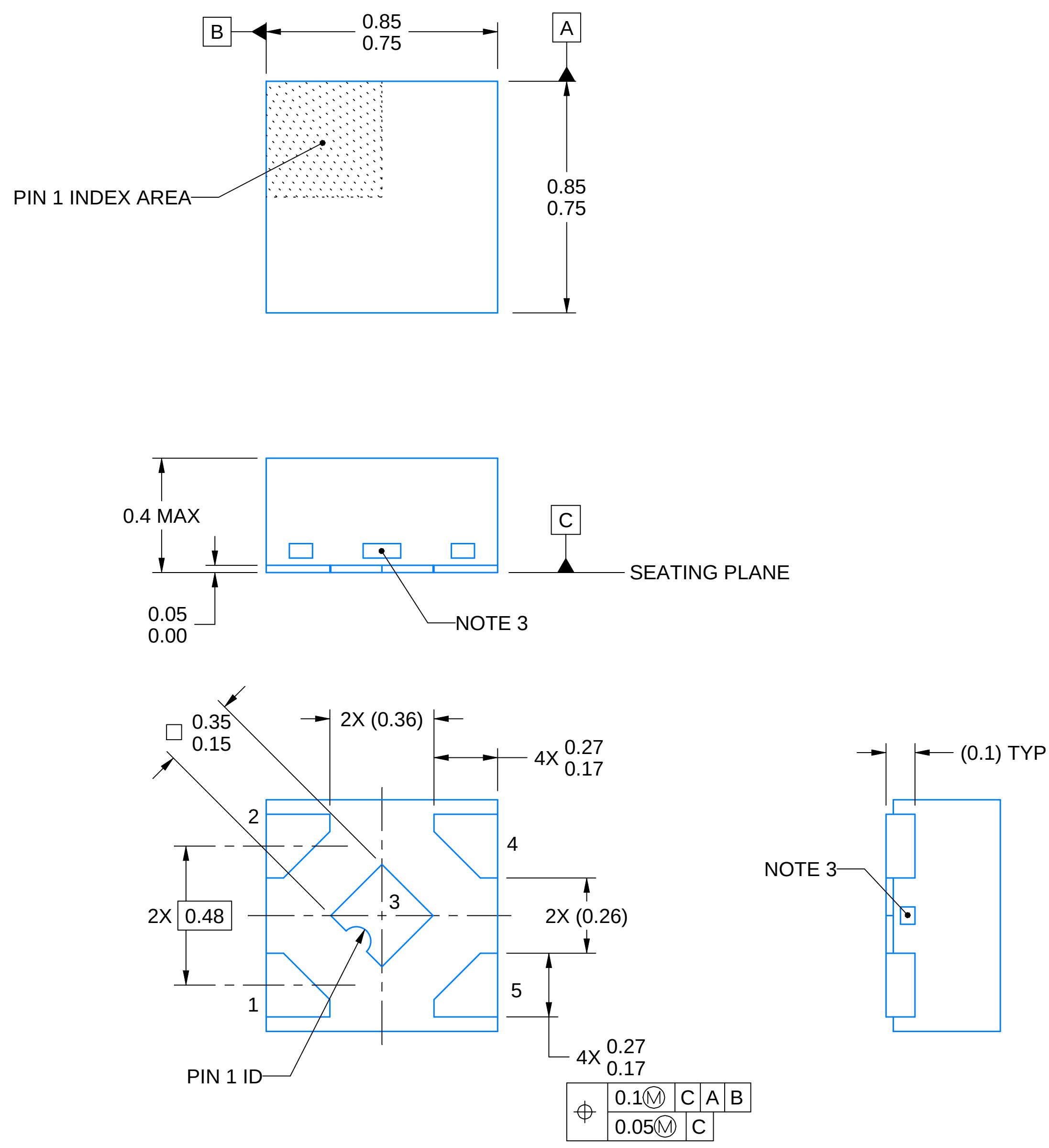
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

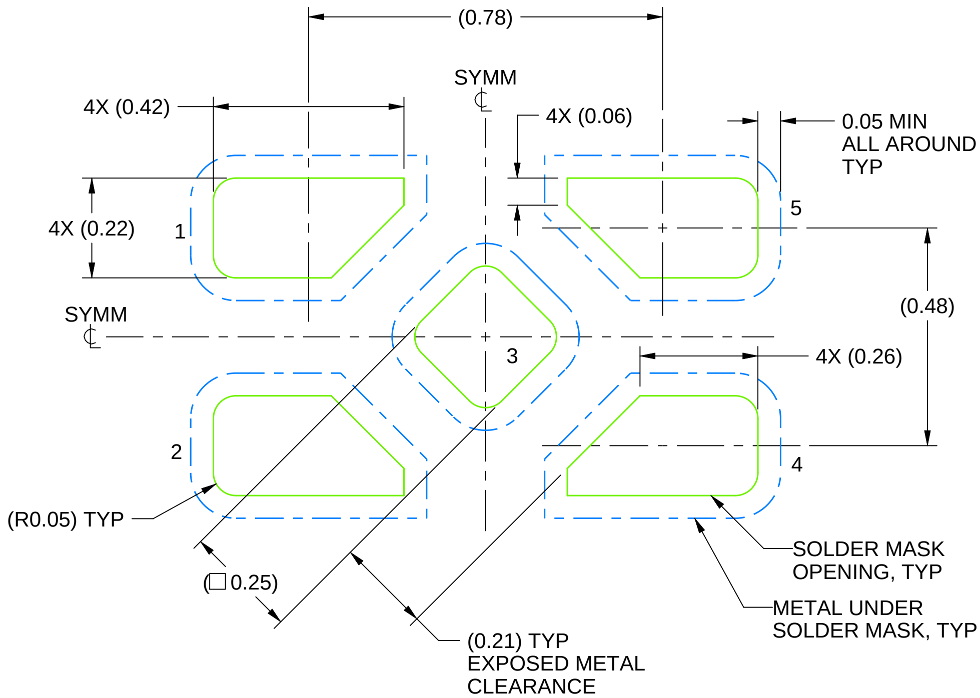
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4228233/C 02/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

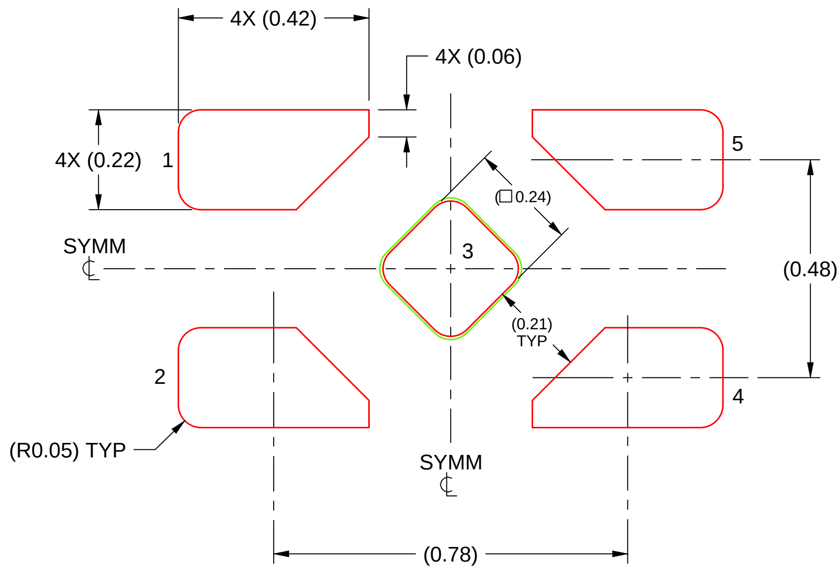


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4228233/C 02/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



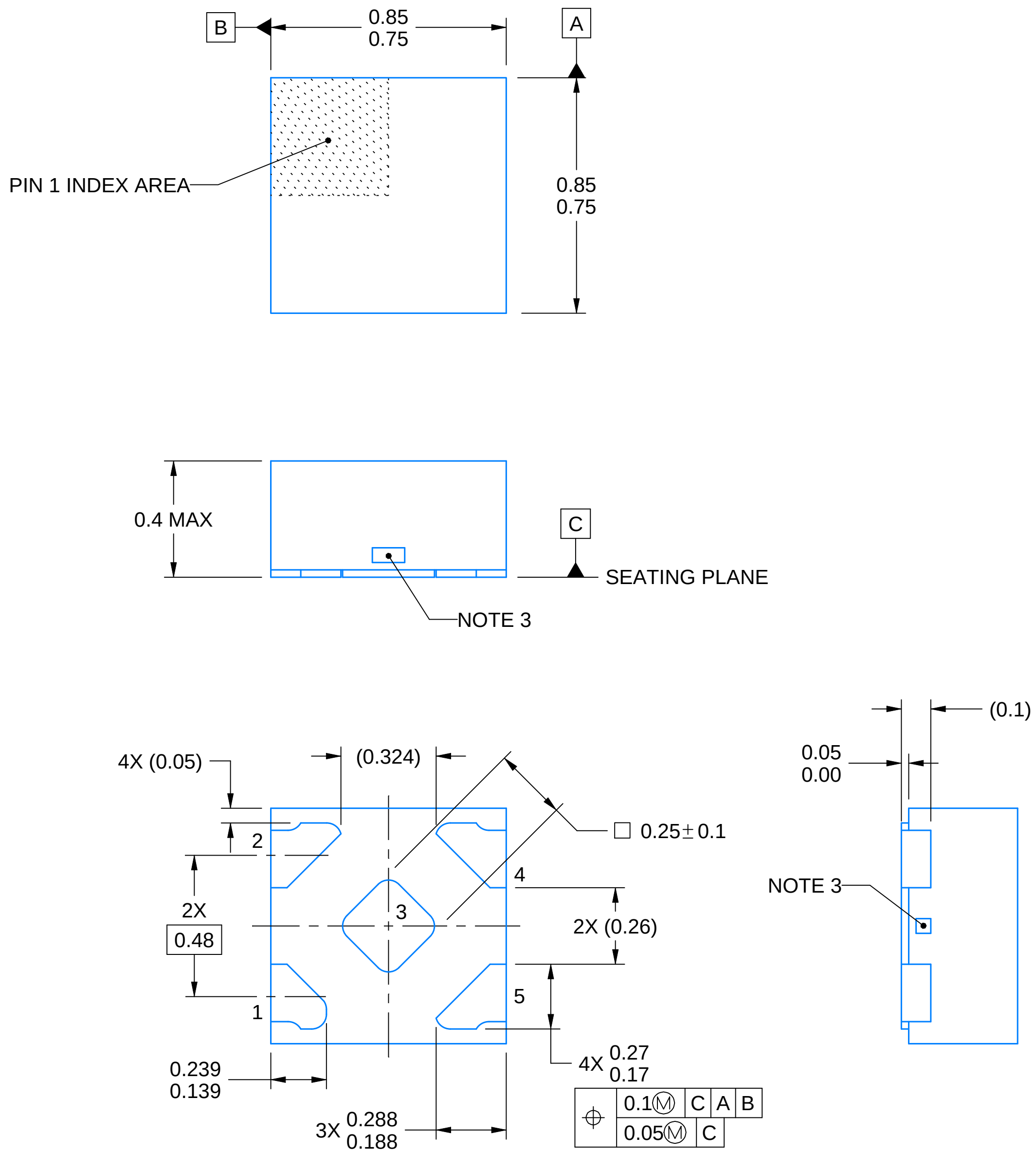
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:60X

4228233/C 02/2022

NOTES: (continued)

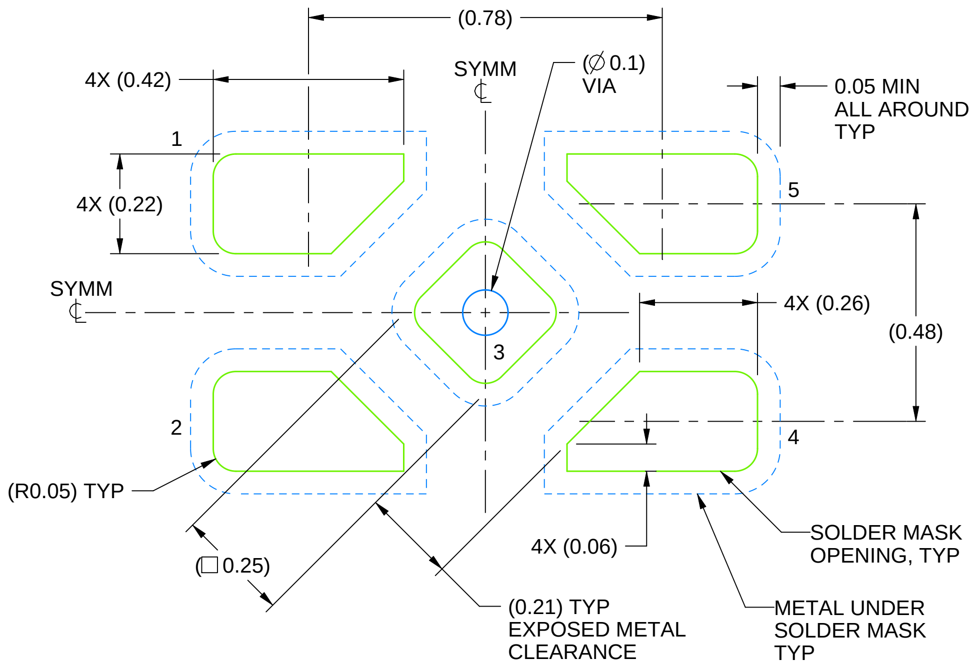
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

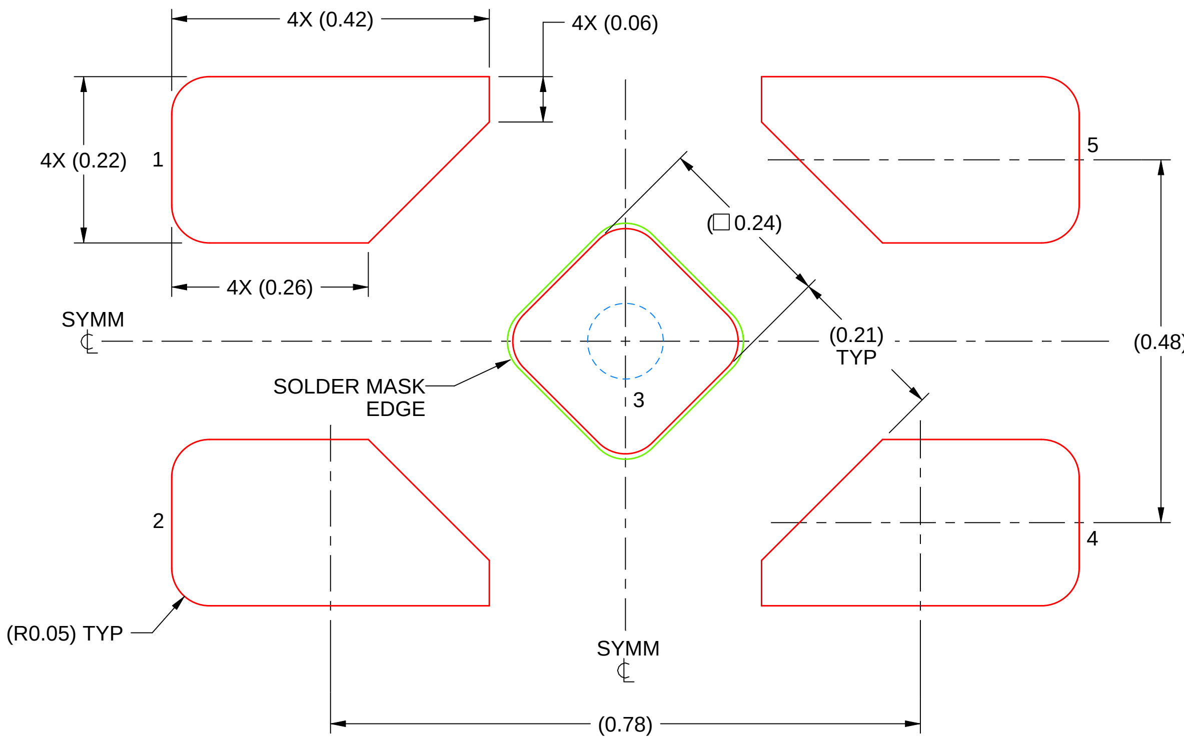


LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

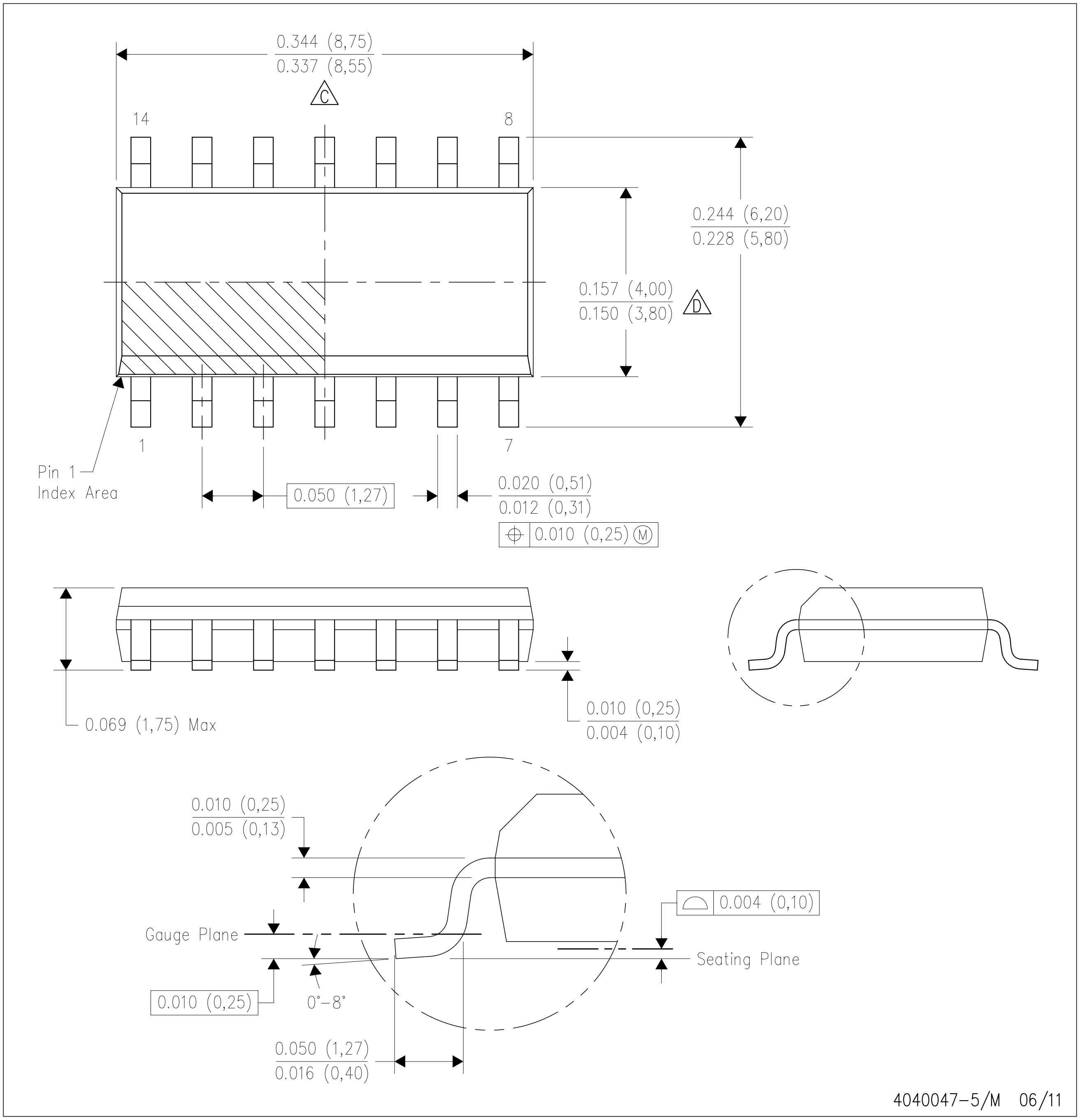
EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

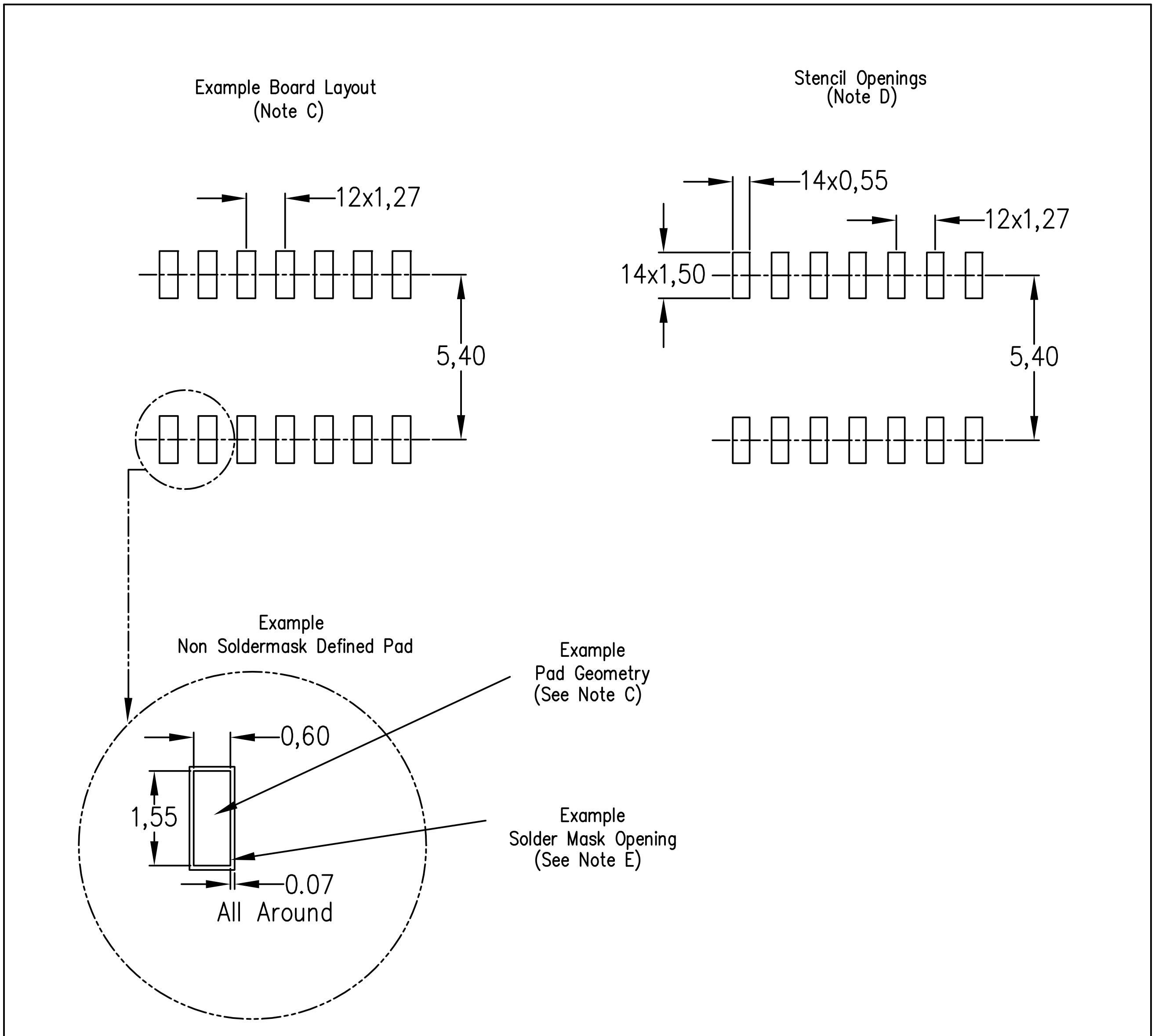
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

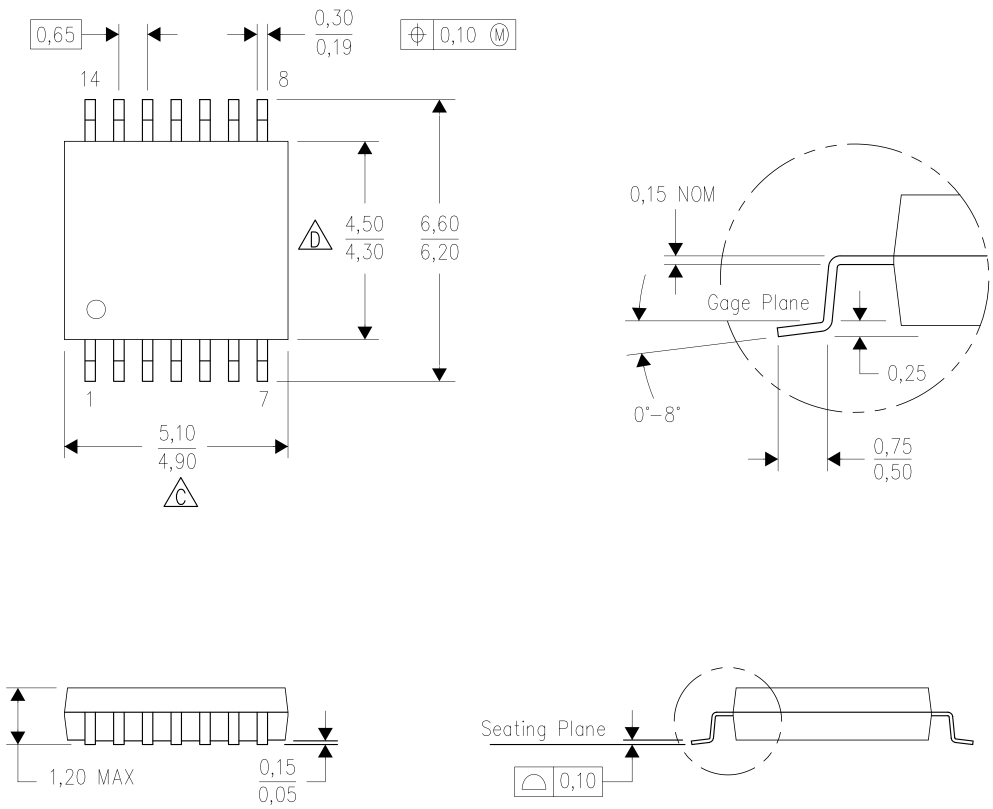
D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211283-3/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

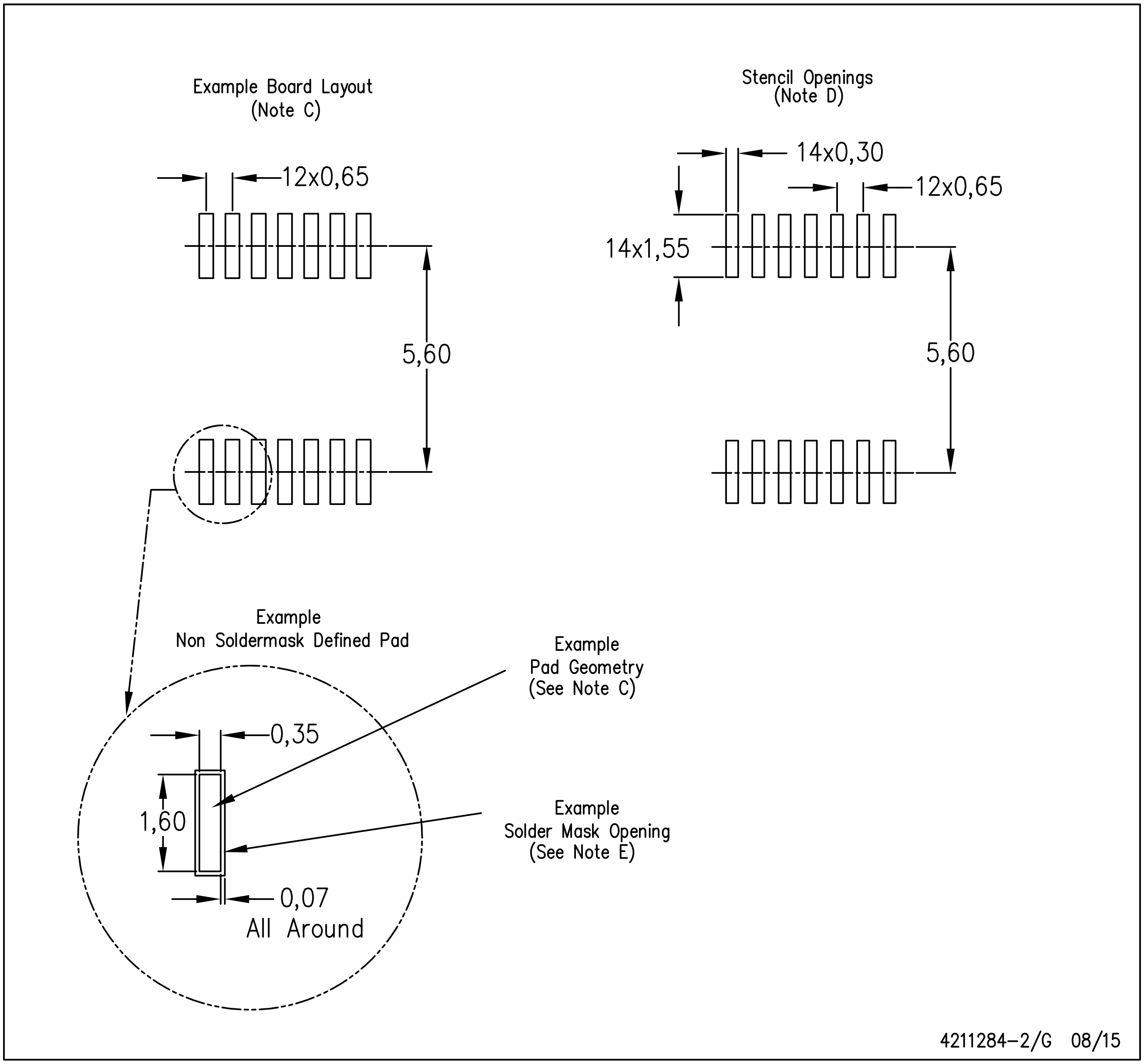
PW (R–PDSO–G14)   PLASTIC SMALL OUTLINE



4040064–3/G 02/11

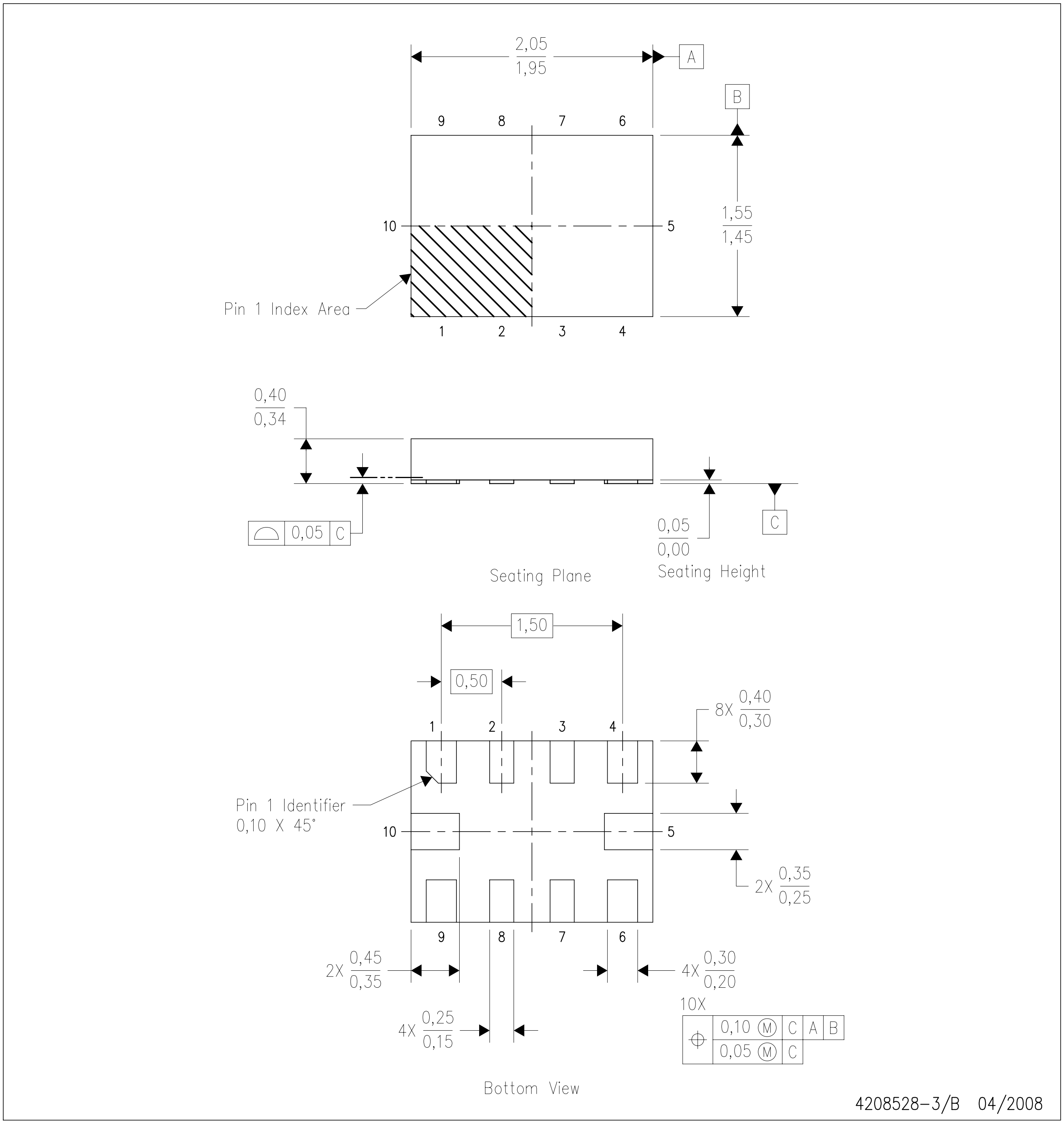
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



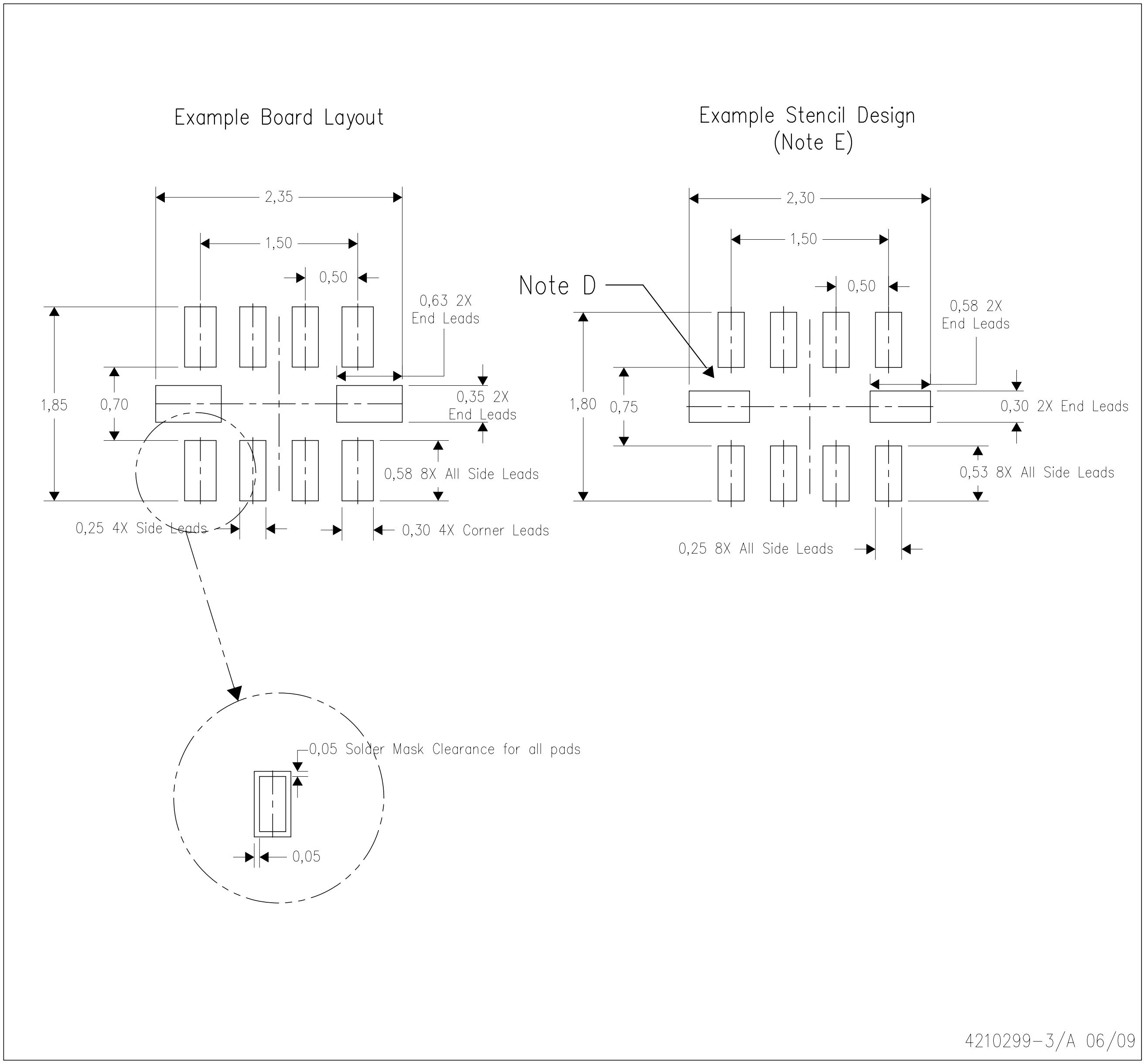
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUG (R-PQFP-N10) PLASTIC QUAD FLATPACK

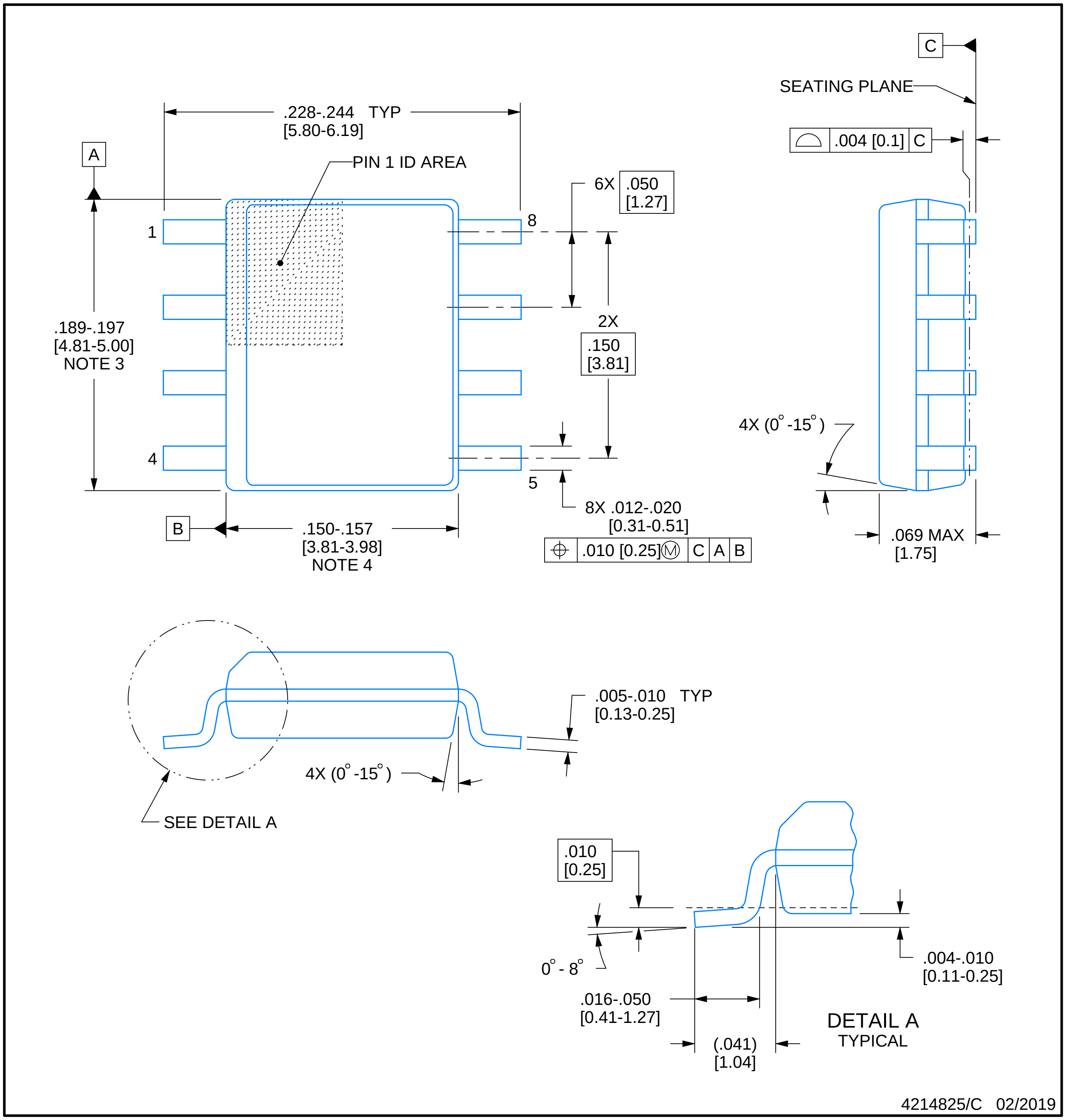


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R–PQFP–N10)

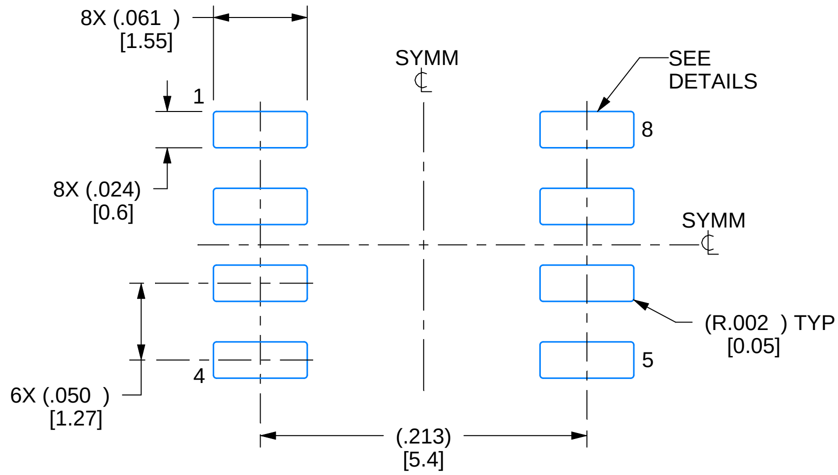


NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

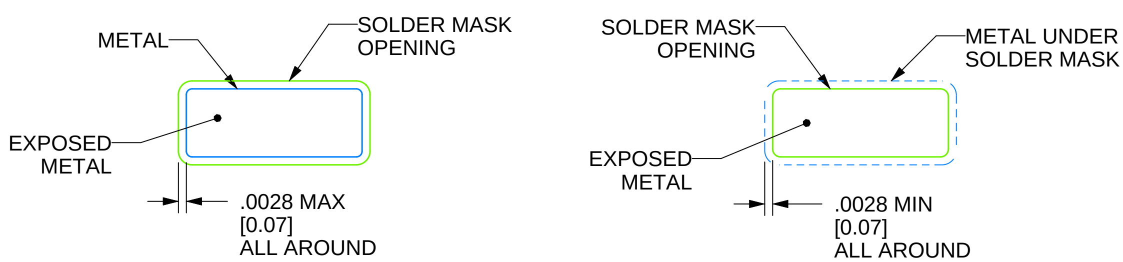


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

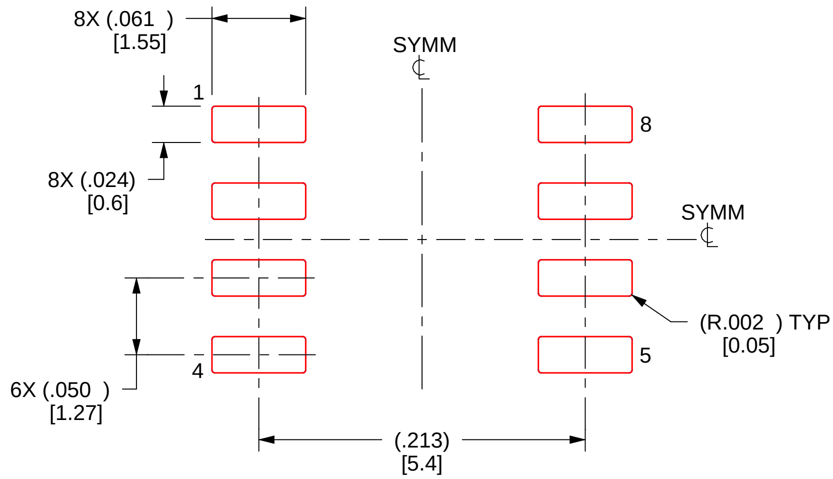
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

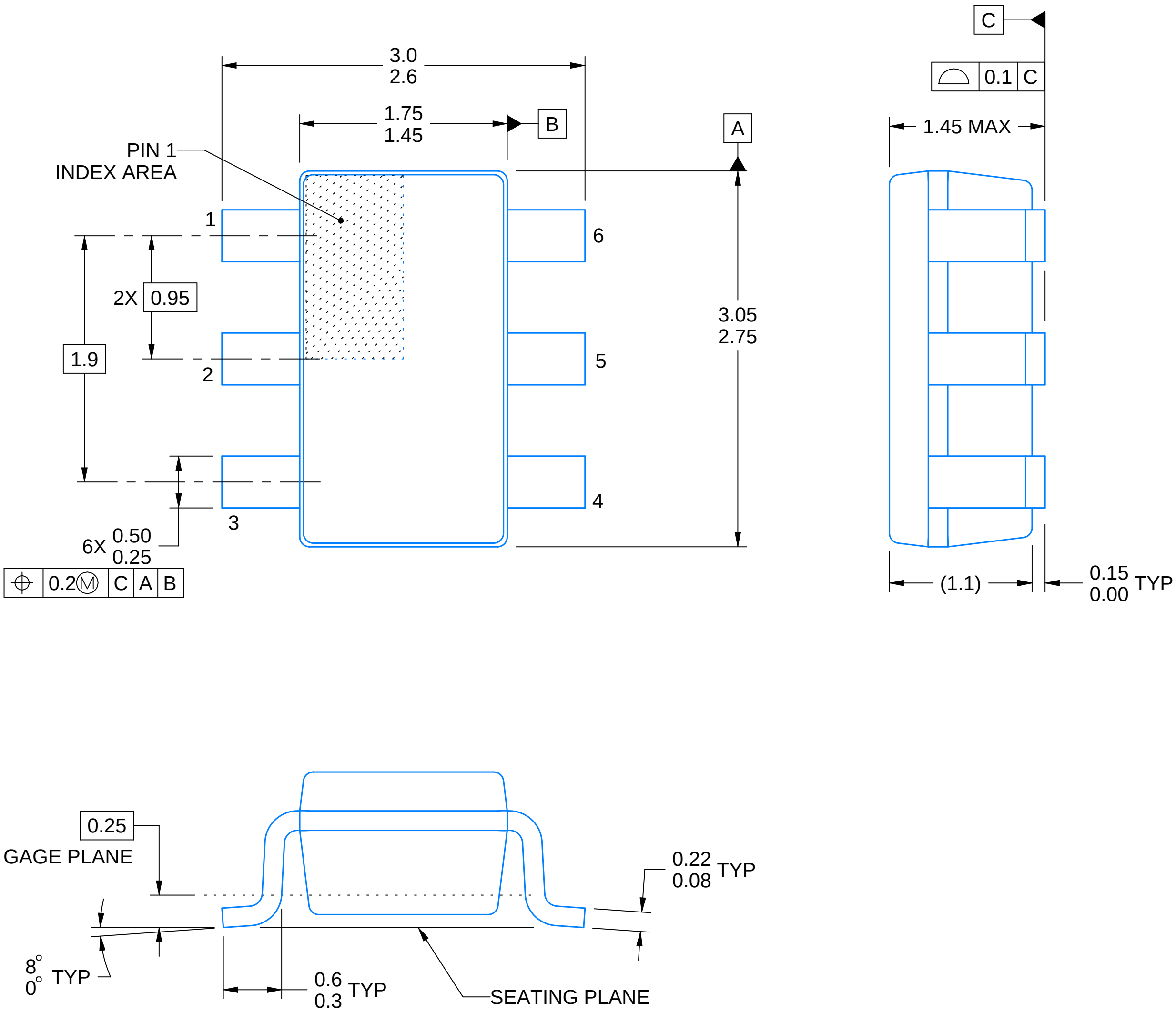


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

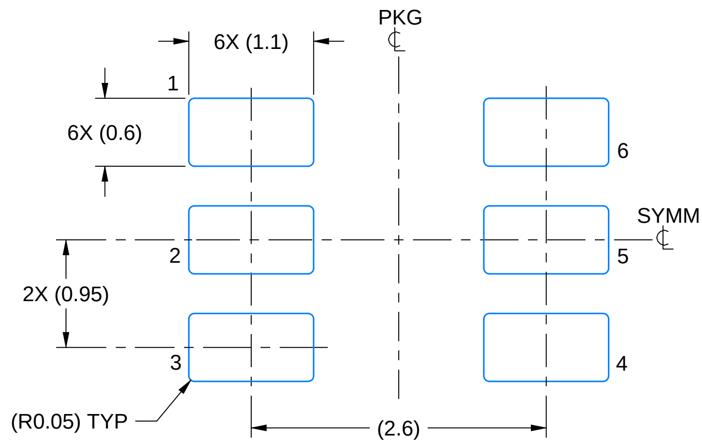
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



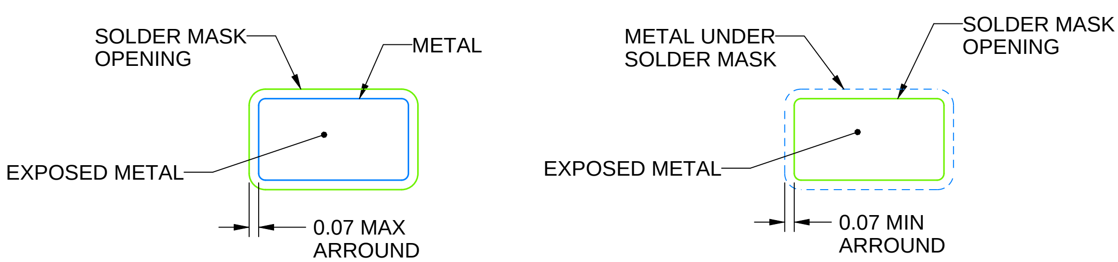
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED (PREFERRED)

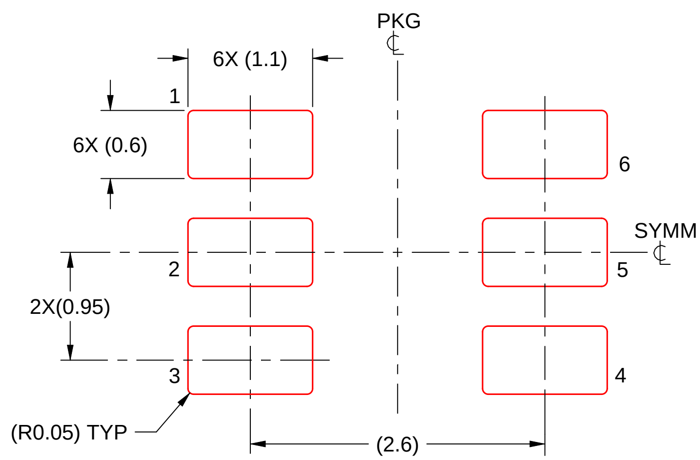
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



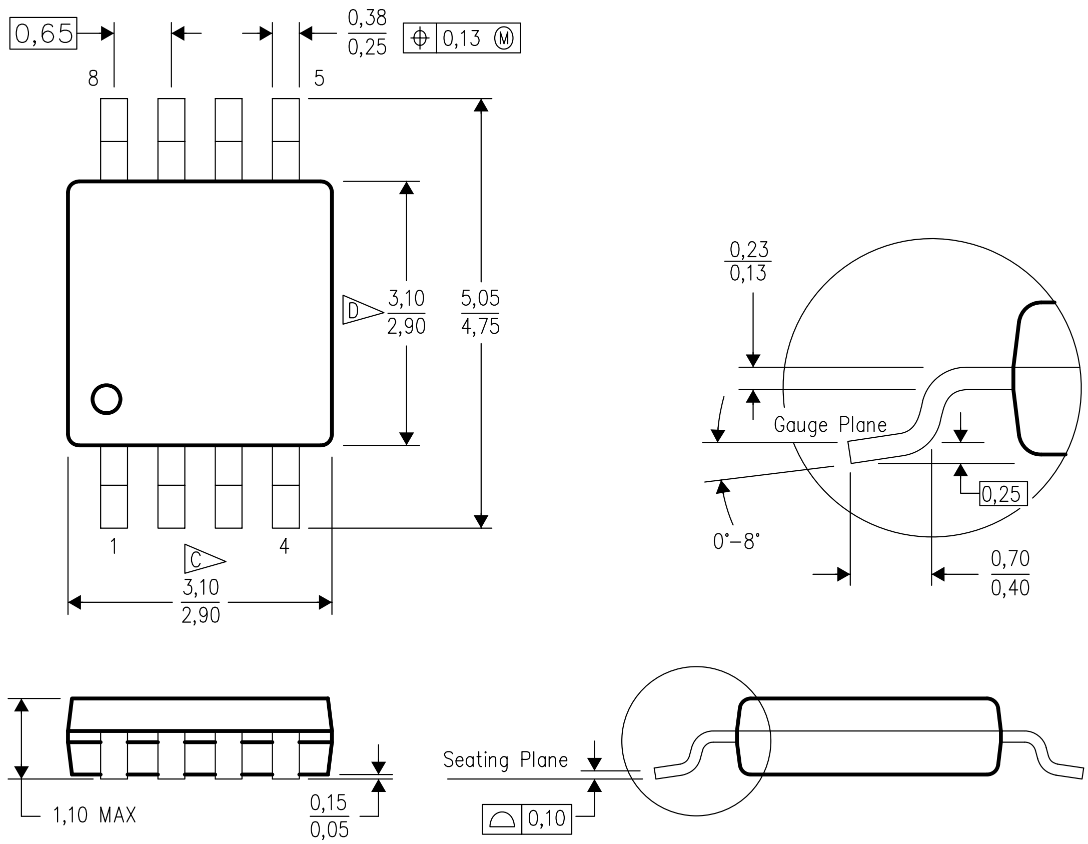
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

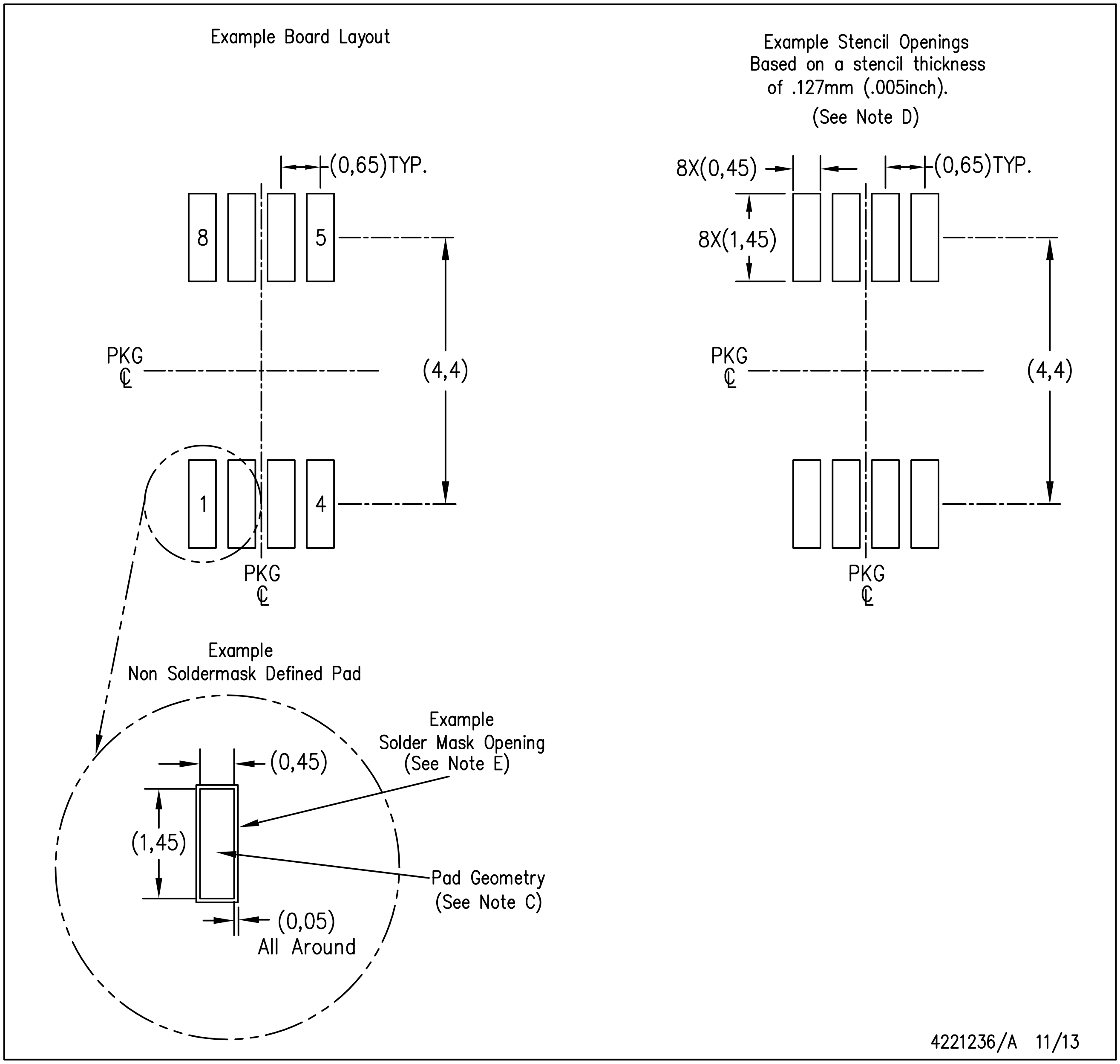
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

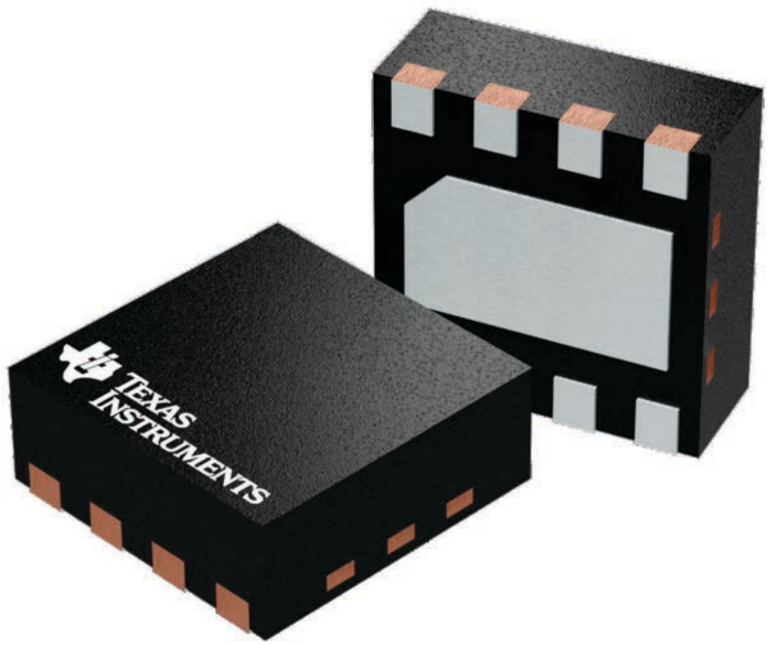
DSG 8

WSON - 0.8 mm max height

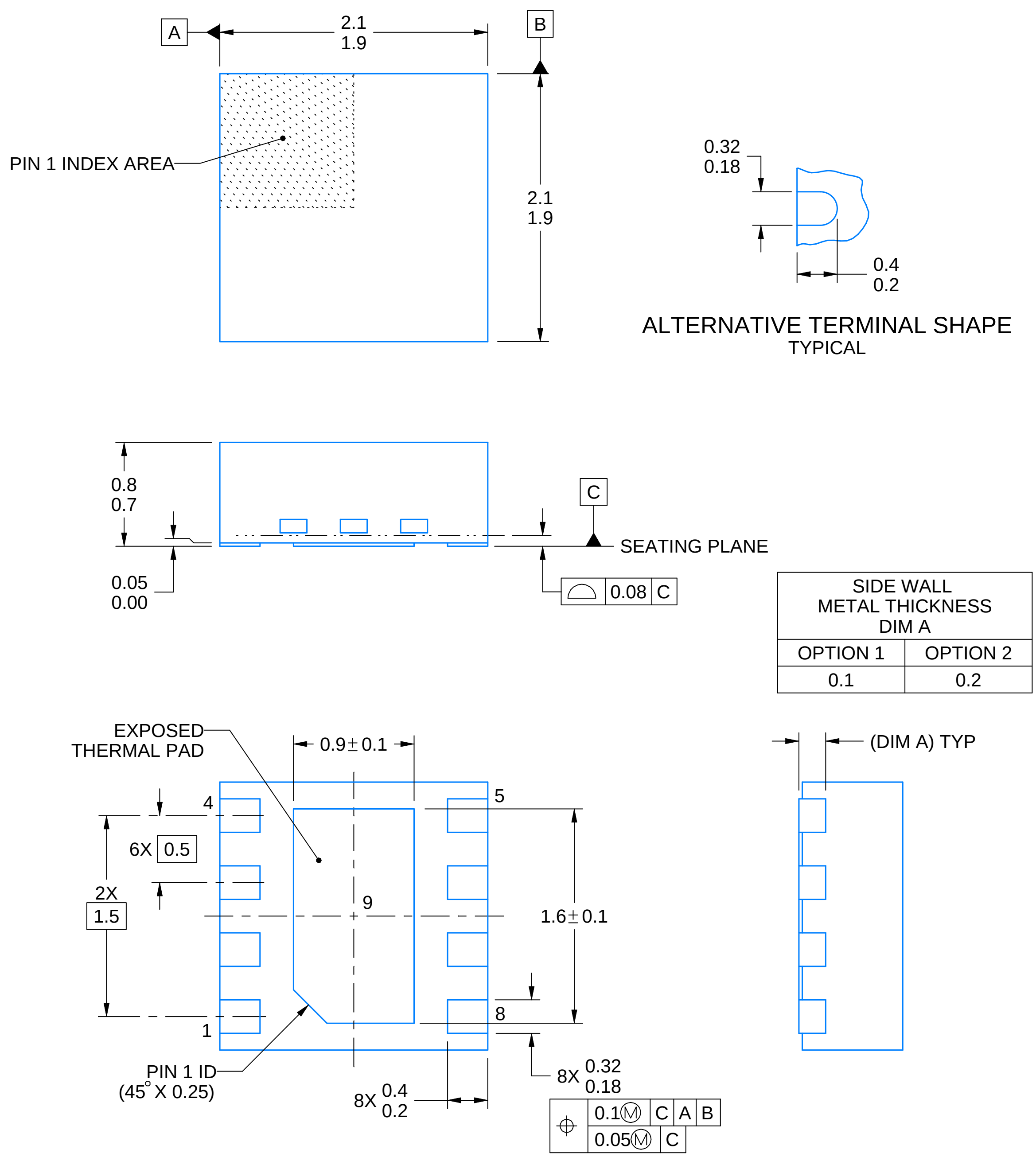
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

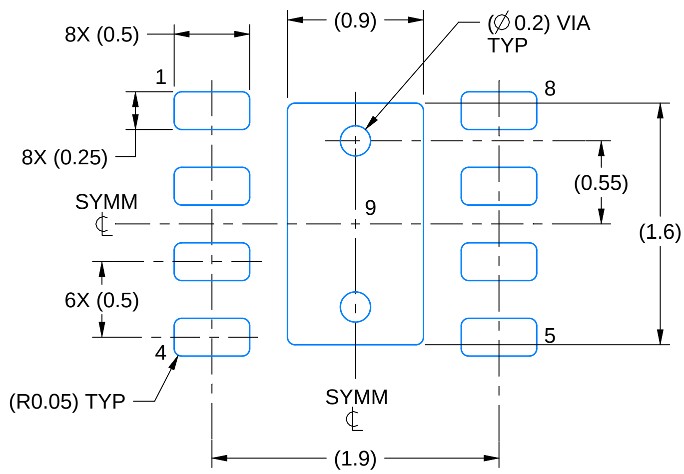


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

NON SOLDER MASK
DEFINED
(PREFERRED)

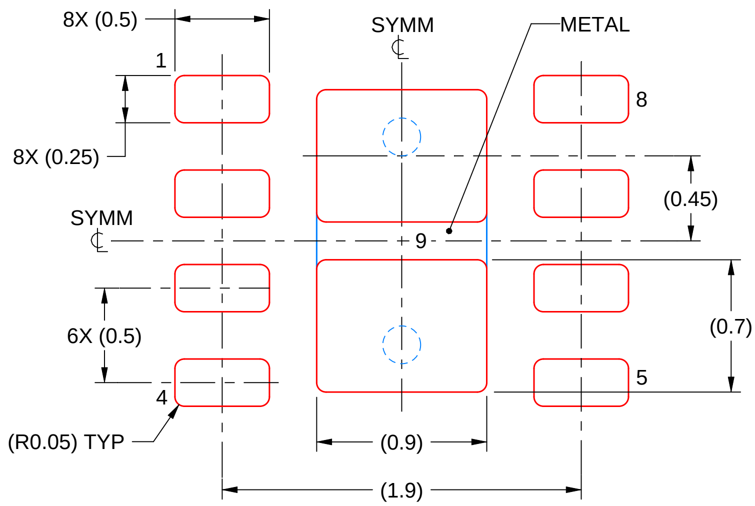
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



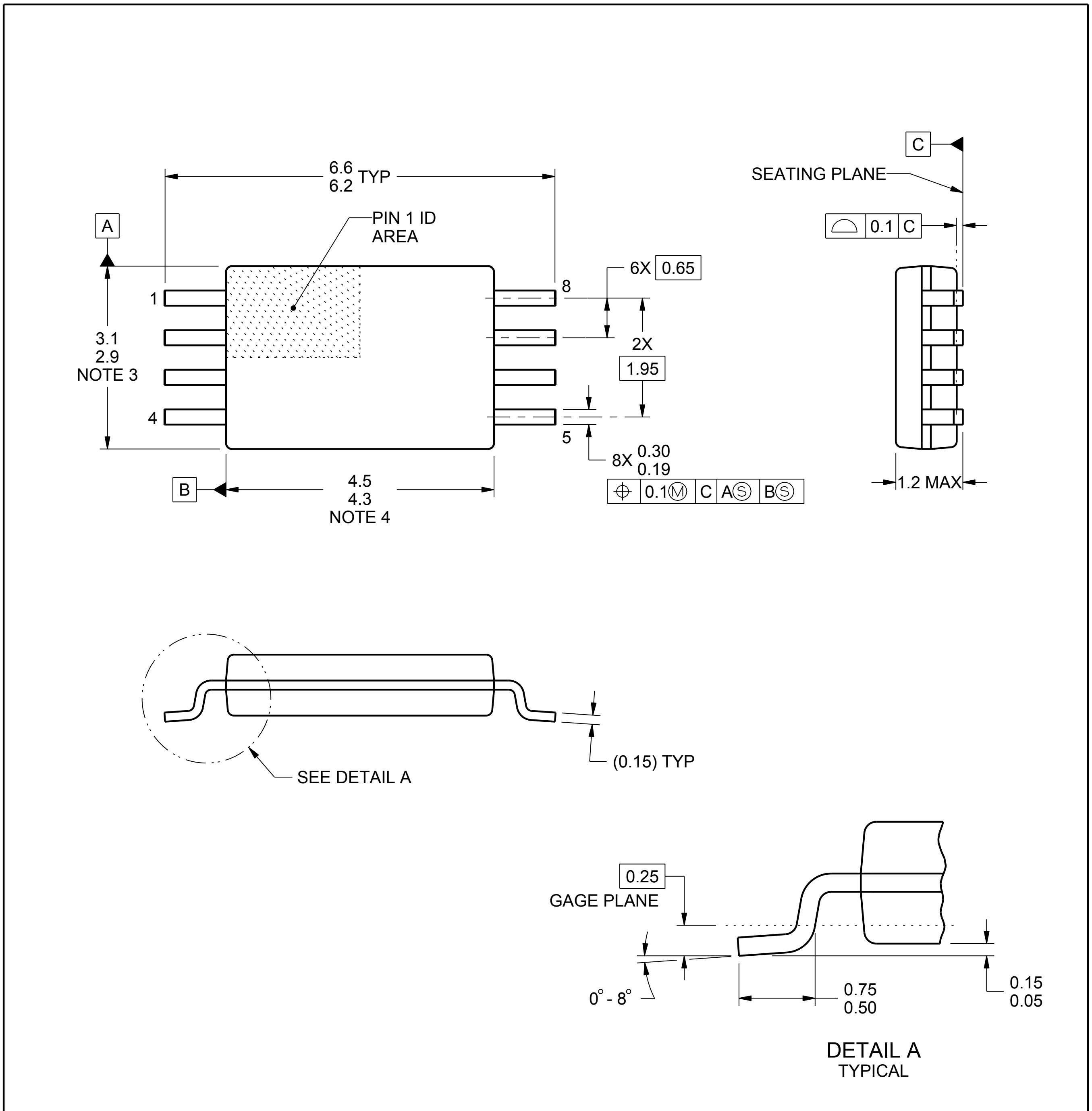
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

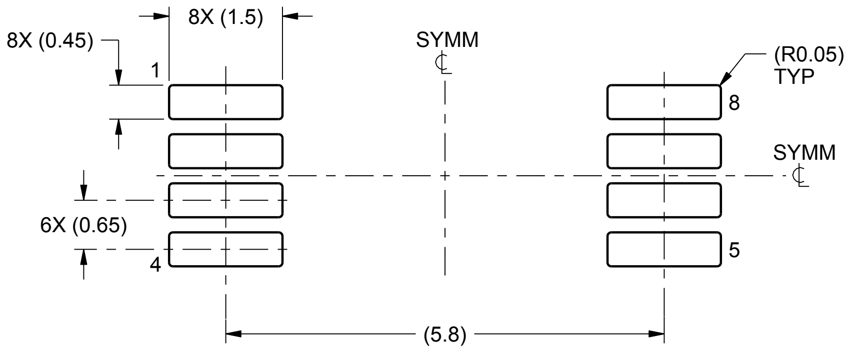
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



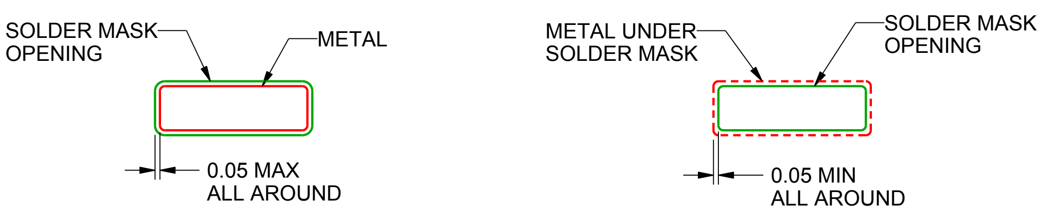
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK DEFINED

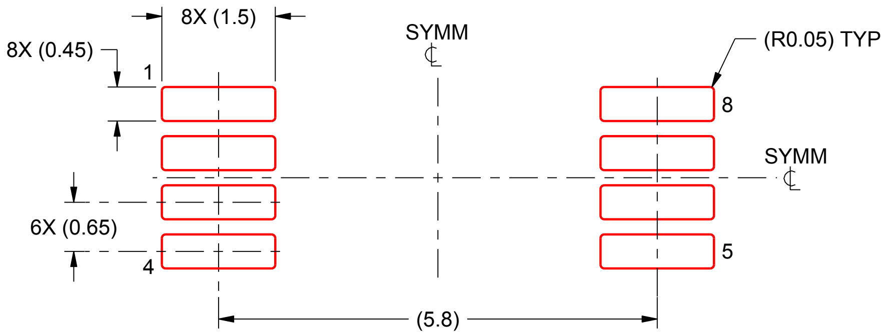
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



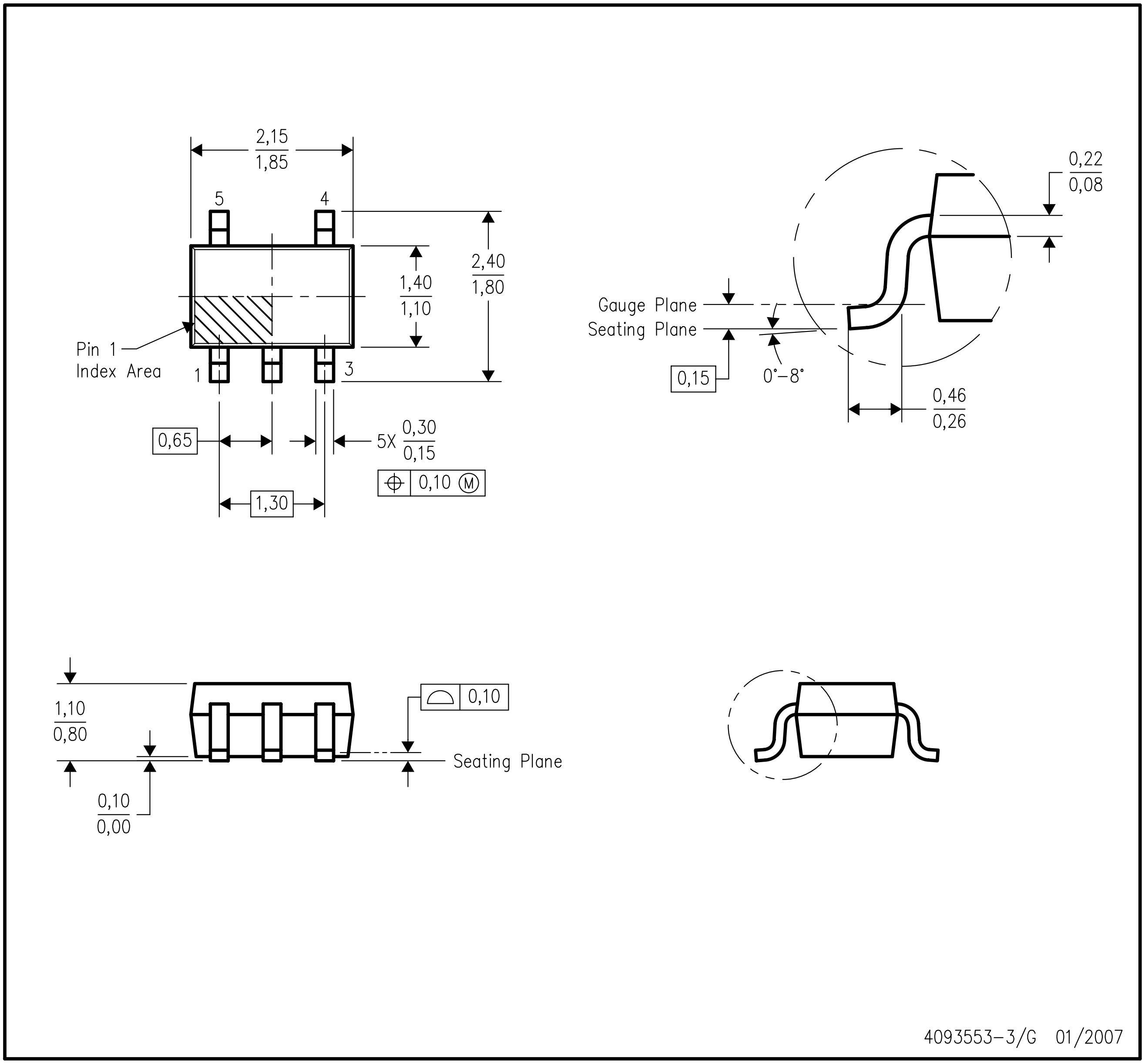
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

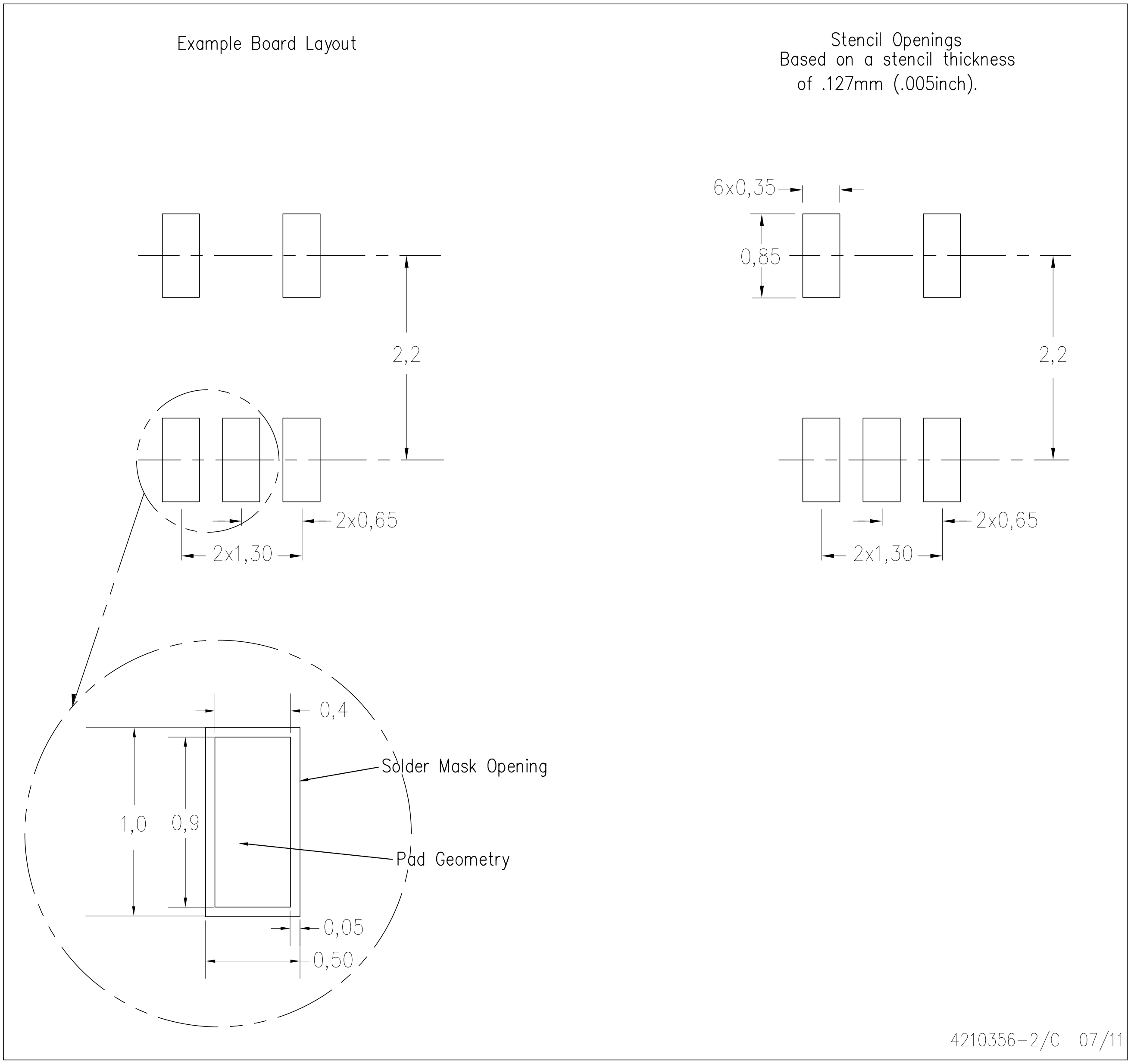
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:

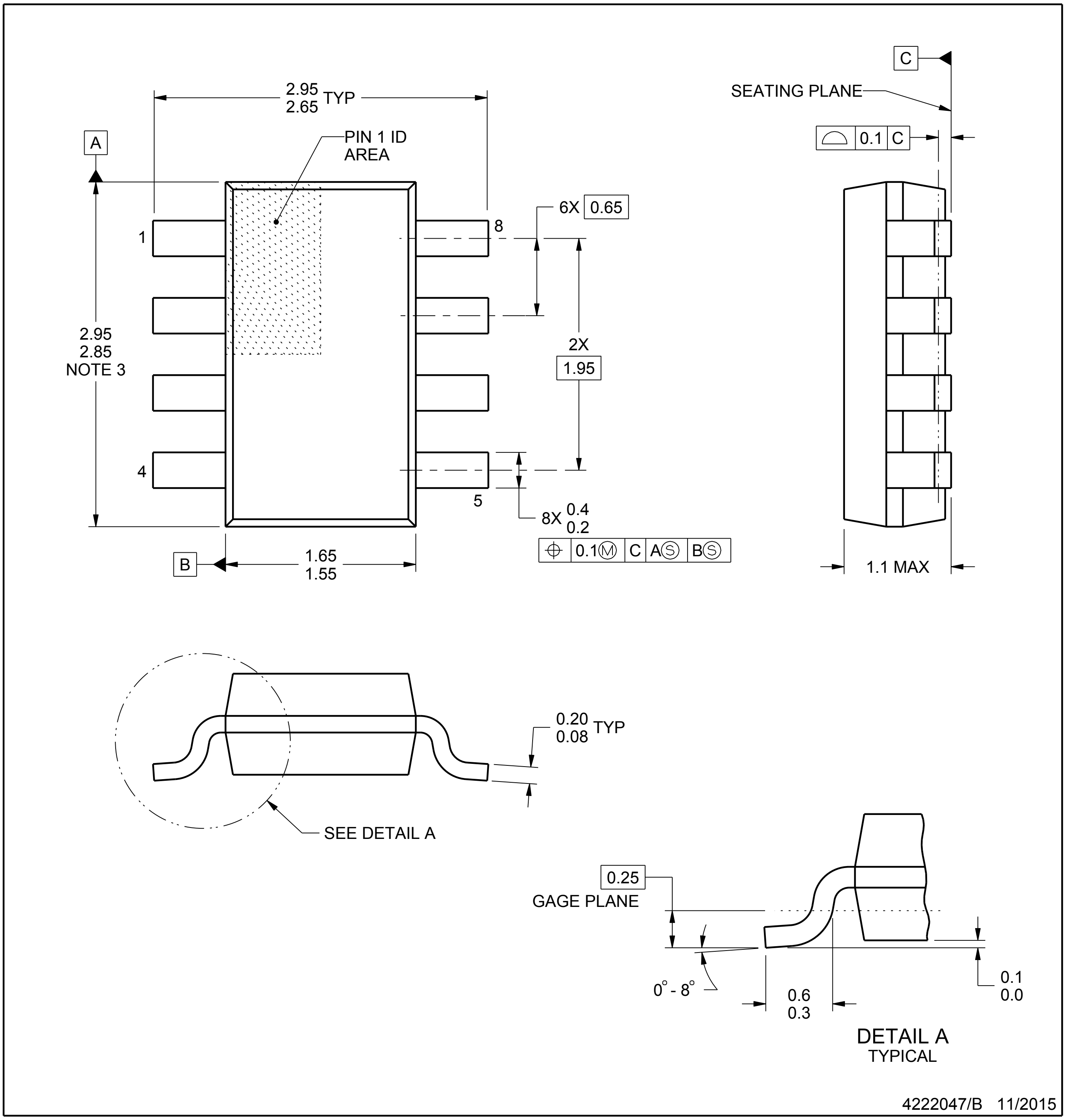
A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

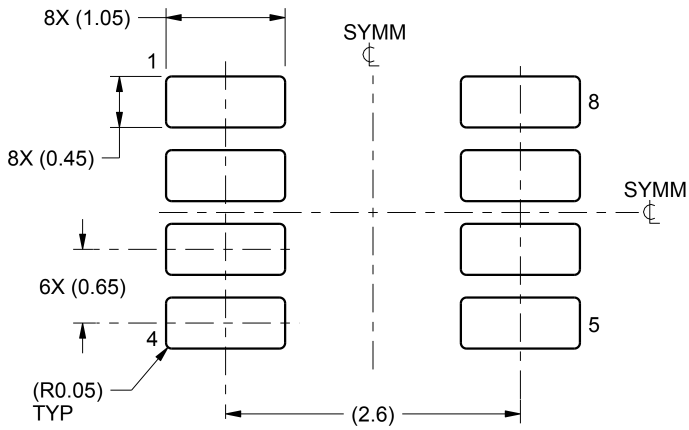
D. Publication IPC–7351 is recommended for alternate designs.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

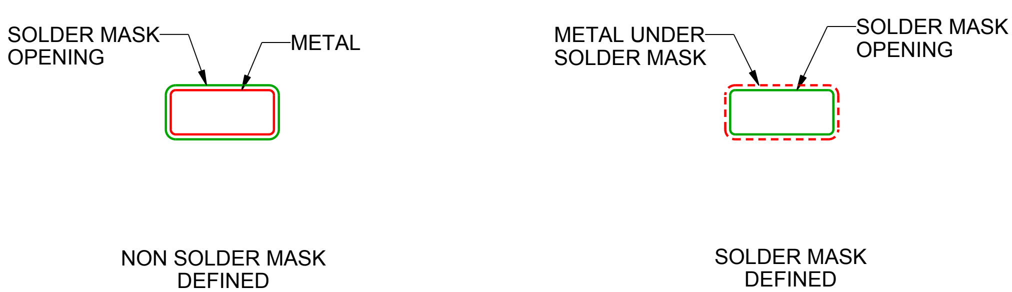


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

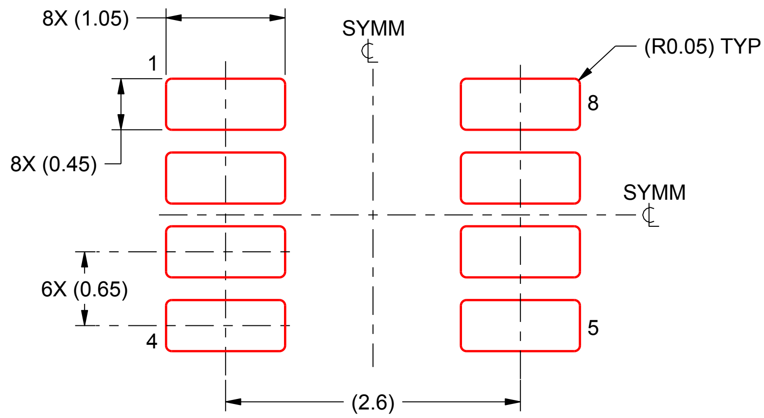


SOLDER MASK DETAILS

4222047/B 11/2015

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

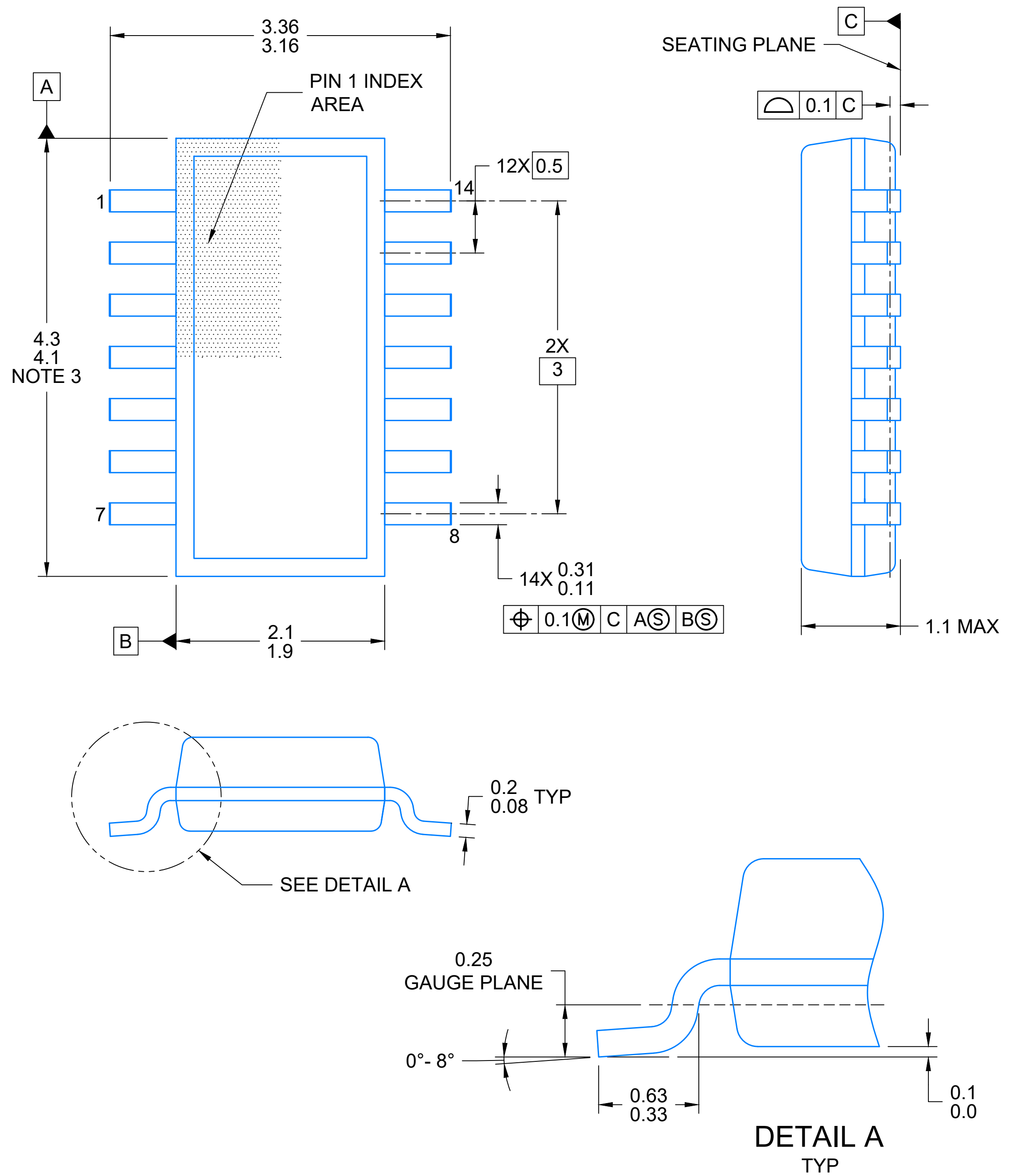


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

NOTES: (continued)

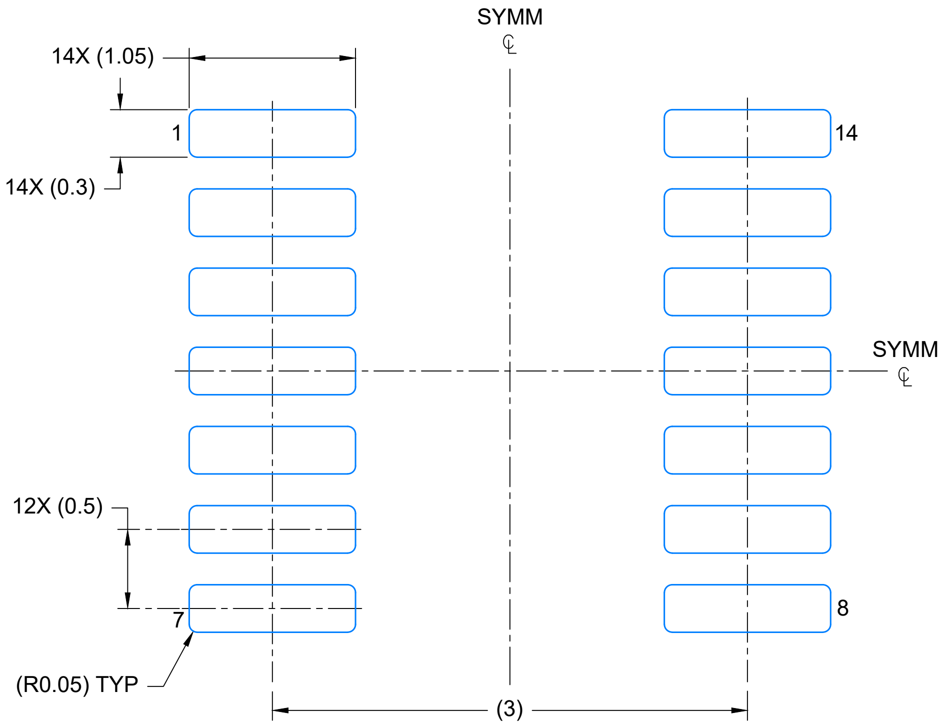
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



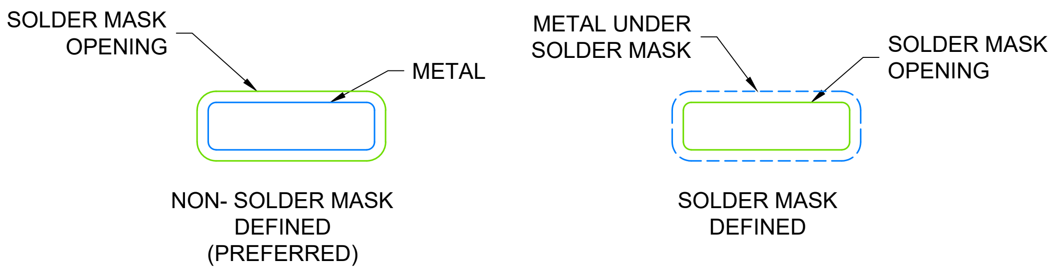
4224643/B 07/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

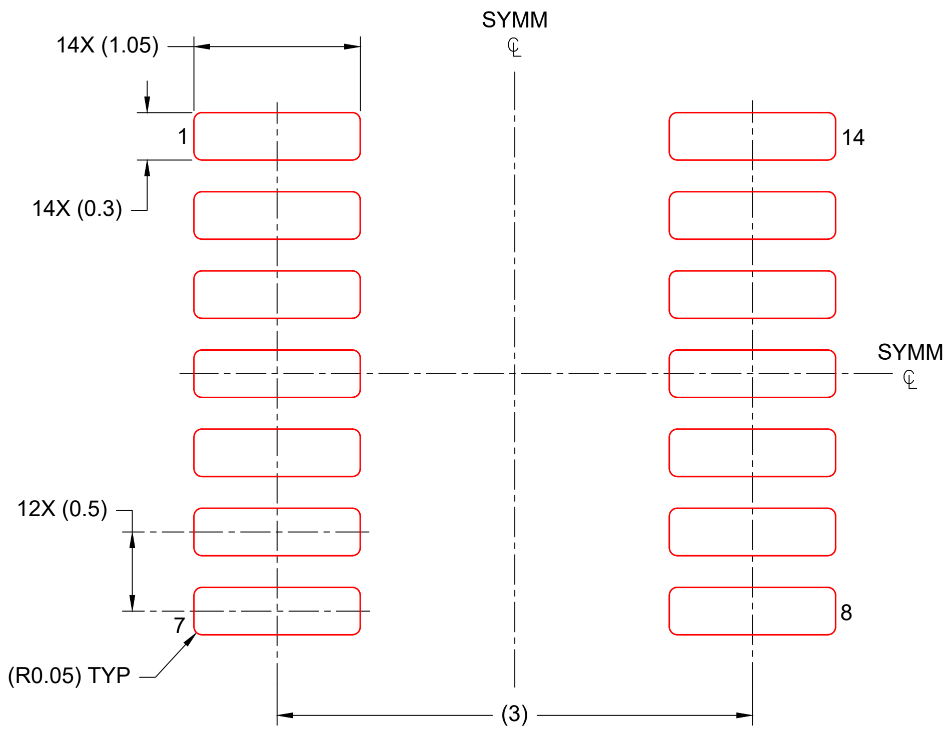


SOLDER MASK DETAILS

4224643/B 07/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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