

TPD1E10B09 采用 0402 封装的单通道 ESD 保护二极管

1 特性

- 可为高达 $\pm 9\text{V}$ 的 I/O 接口提供系统级 ESD 保护
- IEC 61000-4-2 4 级
 - $\pm 20\text{kV}$ (气隙放电)
 - $\pm 20\text{kV}$ (接触放电)
- IEC 61000-4-5 浪涌保护
 - 4.5A (8/20 μs)
- I/O 电容: 10pF (典型值)
- R_{DYN} : 0.5Ω (典型值)
- 直流击穿电压: $\pm 9.5\text{V}$ (最小值)
- 超低泄漏电流: 100nA (最大值)
- 钳位电压: 13V ($I_{\text{PP}} = 1\text{A}$ 时的最大值)
- 工业温度范围: -40°C 至 125°C
- 采用节省空间的 0402 封装 ($1\text{mm} \times 0.6\text{mm} \times 0.5\text{mm}$)

2 应用

- 终端设备:
 - 平板电脑
 - 远程控制器
 - 可穿戴产品
 - 机顶盒
 - 电子销售点 (EPOS)
 - 电子书阅读器
- 接口:
 - 音频线路
 - 按钮
 - 通用输入/输出 (GPIO)

3 说明

TPD1E10B09 器件是一款采用小型 0402 封装的单通道 ESD 瞬态电压抑制 (TVS) 二极管。这款 ESD 保护二极管提供 $\pm 20\text{kV}$ IEC 61000-4-2 (4 级) 接触和气隙 ESD 保护。该器件提供背靠背 TVS 二极管配置以支持 bipolar 或双向信号。线路电容为 10pF , 适用于支持高达 500Mbps 数据传输速率的广泛应用。0402 封装符合行业标准, 便于将元件安装到空间受限型应用中。

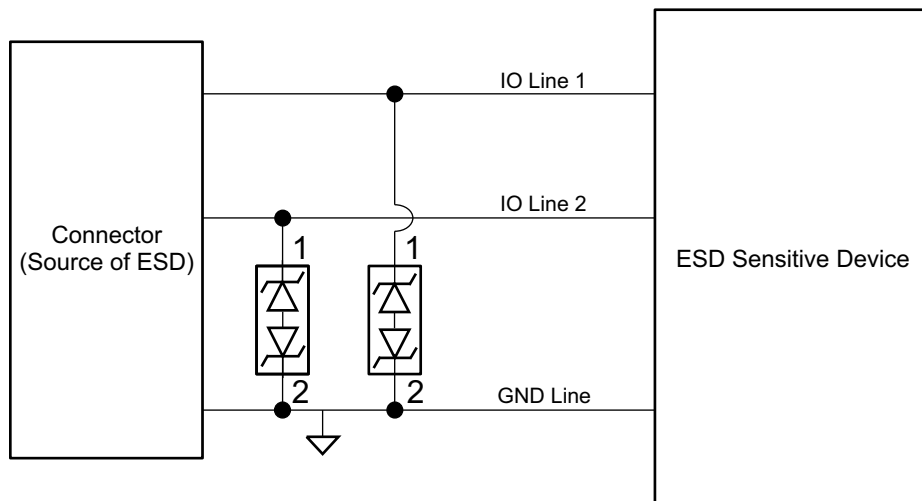
这款 ESD 保护 TVS 二极管的典型应用是为音频线路 (麦克风、耳机和扬声器)、SD 接口、键盘或其他按钮、USB 端口的 V_{BUS} 引脚和 ID 引脚以及通用 I/O 端口等提供电路保护。该 ESD 钳位有利于为电子书阅读器、平板电脑、远程控制器、可穿戴设备、机顶盒以及电子销售点等终端设备提供保护。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPD1E10B09	X1SON (2)	0.60mm x 1.00mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

应用电路原理图



目录

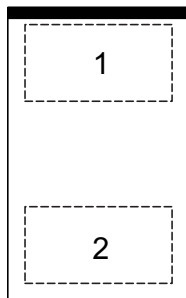
<p>1 特性 1</p> <p>2 应用 1</p> <p>3 说明 1</p> <p>4 修订历史记录 2</p> <p>5 Pin Configuration and Functions 3</p> <p>6 Specifications 3</p> <p> 6.1 Absolute Maximum Ratings 3</p> <p> 6.2 ESD Ratings 3</p> <p> 6.3 Recommended Operating Conditions 3</p> <p> 6.4 Thermal Information 4</p> <p> 6.5 Electrical Characteristics 4</p> <p> 6.6 Typical Characteristics 5</p> <p>7 Detailed Description 7</p> <p> 7.1 Overview 7</p> <p> 7.2 Functional Block Diagram 7</p>	<p> 7.3 Feature Description 7</p> <p> 7.4 Device Functional Modes 7</p> <p>8 Application and Implementation 8</p> <p> 8.1 Application Information 8</p> <p> 8.2 Typical Application 8</p> <p>9 Power Supply Recommendations 10</p> <p>10 Layout 10</p> <p> 10.1 Layout Guidelines 10</p> <p> 10.2 Layout Example 10</p> <p>11 器件和文档支持 11</p> <p> 11.1 社区资源 11</p> <p> 11.2 商标 11</p> <p> 11.3 静电放电警告 11</p> <p> 11.4 Glossary 11</p> <p>12 机械、封装和可订购信息 11</p>
--	--

4 修订历史记录

Changes from Revision C (Aug 2015) to Revision D	Page
<ul style="list-style-type: none"> • Added capacitive measurement frequency 4 	4
Changes from Revision B (June 2015) to Revision C	Page
<ul style="list-style-type: none"> • 已添加 <i>ESD</i> 额定值表, 特性 描述部分, 器件功能模式, 应用和实施部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分 1 	1
Changes from Revision A (March 2012) to Revision B	Page
<ul style="list-style-type: none"> • Added THERMAL INFORMATION table 4 	4
Changes from Original (February 2012) to Revision A	Page
<ul style="list-style-type: none"> • 已更新 特性。 1 • Added graphs to TYPICAL CHARACTERISTICS section 5 • Added APPLICATION INFORMATION section 8 	1 5 8

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN	I/O	DESCRIPTION
1	I/O	ESD protected I/O
2		

6 Specifications

6.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Operating temperature	-40	125	°C
I_{PP} Peak pulse current (tp = 8/20 μ s)		4.5	A
P_{PP} Peak pulse power (tp = 8/20 μ s)		90	W
T_{stg} Storage temperature	-65	155	°C

6.2 ESD Ratings

	VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000
	IEC 61000-4-2 Contact Discharge	20000
	IEC 61000-4-2 Air-Gap Discharge	20000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A	-40		125	°C
Operating voltage	Pin 1 to 2 or pin 2 to 1		9	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPD1E10B09	UNIT
		DPY (X1SON)	
		2 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	615.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	404.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	493.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	127.7	°C/W
ψ _{JB}	Junction-to-board characterization parameter	493.3	°C/W
P	Power Dissipation ⁽²⁾	162	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) Max junction temperature: 125°C; power dissipation calculated at 25°C ambient temperature using JEDEC High K board Standard. Not to be used for steady state power dissipation in the breakdown region.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V _{RWM}	Reverse stand-off voltage	Pin 1 to 2 or pin 2 to 1			9	V
I _{LEAK}	Leakage current	Pin 1 = 5 V, pin 2 = 0 V			100	nA
V _{Clamp1,2}	Clamp voltage with ESD strike on pin 1, pin 2 grounded.	I _{PP} = 1 A, t _p = 8/20 μSec ⁽¹⁾			13	V
		I _{PP} = 5 A, t _p = 8/20 μSec ⁽¹⁾			17	
V _{Clamp2,1}	Clamp voltage with ESD strike on pin 2, pin 1 grounded.	I _{PP} = 1 A, t _p = 8/20 μSec ⁽¹⁾			13	V
		I _{PP} = 4.5 A, t _p = 8/20 μSec ⁽¹⁾			20	
R _{DYN}	Dynamic resistance	Pin 1 to pin 2 ⁽²⁾		0.5		Ω
		Pin 2 to pin 1 ⁽²⁾		0.5		
C _{IO}	I/O capacitance	V _{IO} = 2.5 V; f = 1 MHz		10		pF
V _{BR1,2}	Break-down voltage, pin 1 to pin 2	I _{IO} = 1 mA	9.5			V
V _{BR2,1}	Break-down voltage, pin 2 to pin 1	I _{IO} = 1 mA	9.5			V

(1) Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.

(2) Extraction of R_{DYN} using least squares fit of TLP characteristics from I_{PP} = 10 A to I_{PP} = 20 A.

6.6 Typical Characteristics

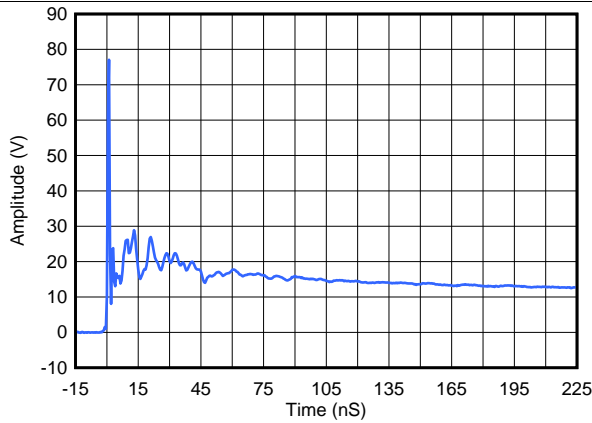


Figure 1. ESD Clamp Voltage +8 kV Contact ESD

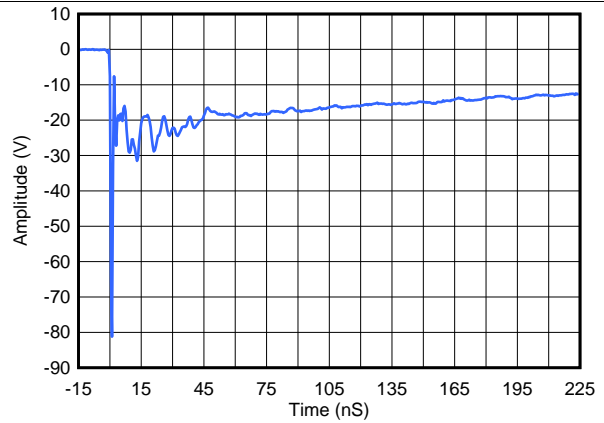


Figure 2. ESD Clamp Voltage -8 kV Contact ESD

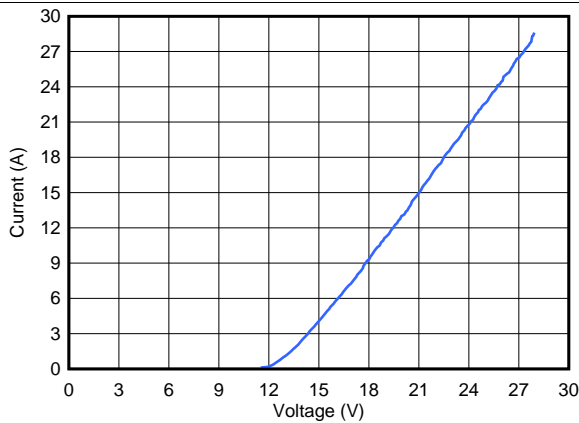


Figure 3. Transmission Line Pulse (TLP) Waveform Pin 1 to Pin 2

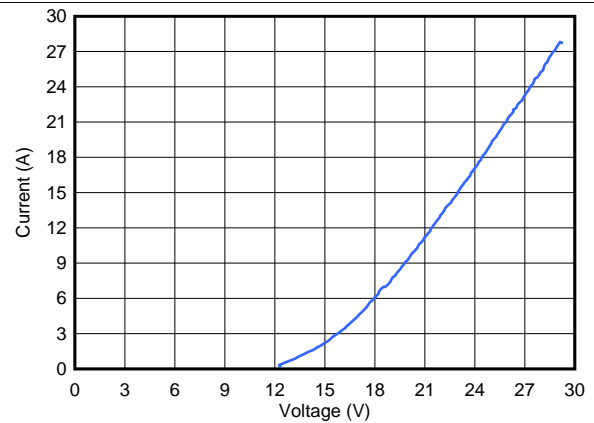


Figure 4. Transmission Line Pulse (TLP) Waveform Pin 2 to Pin 1

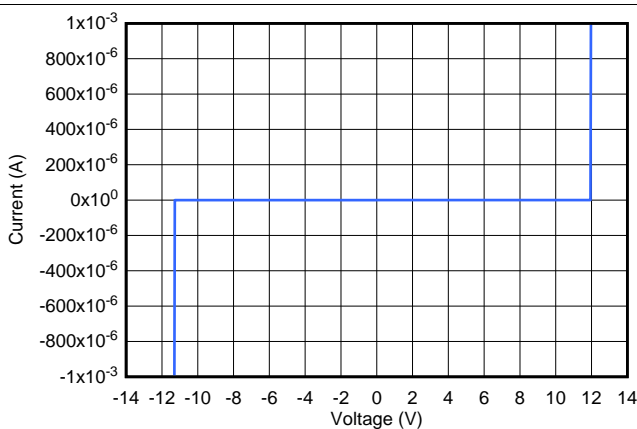


Figure 5. IV Curve

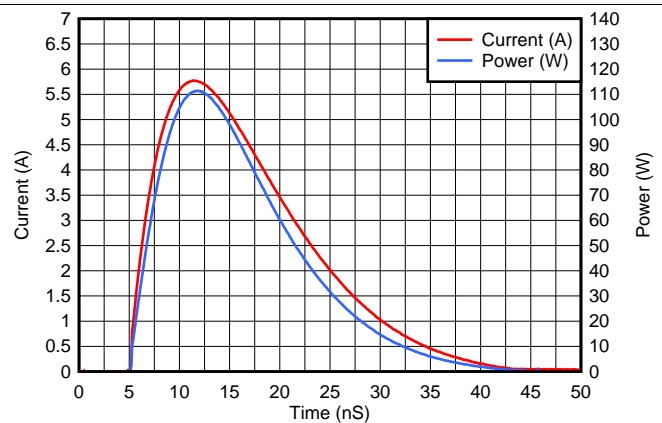
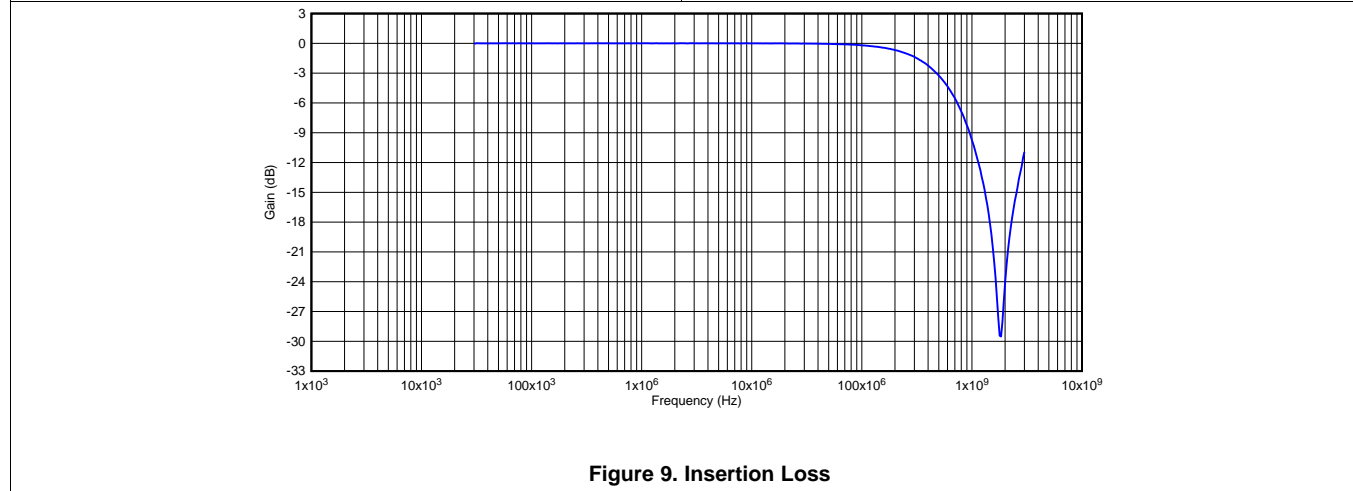
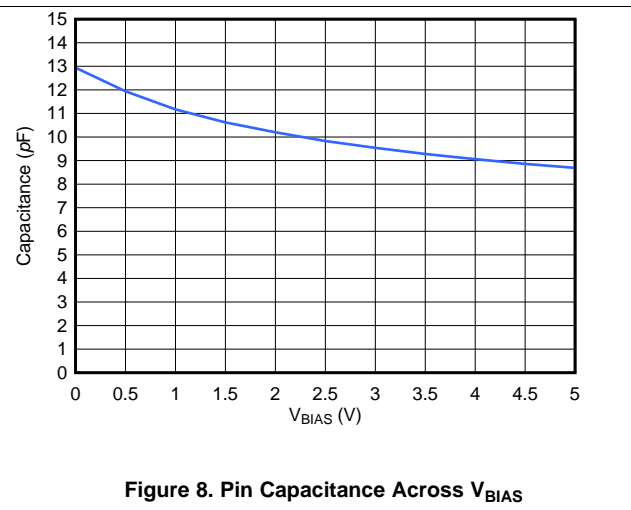
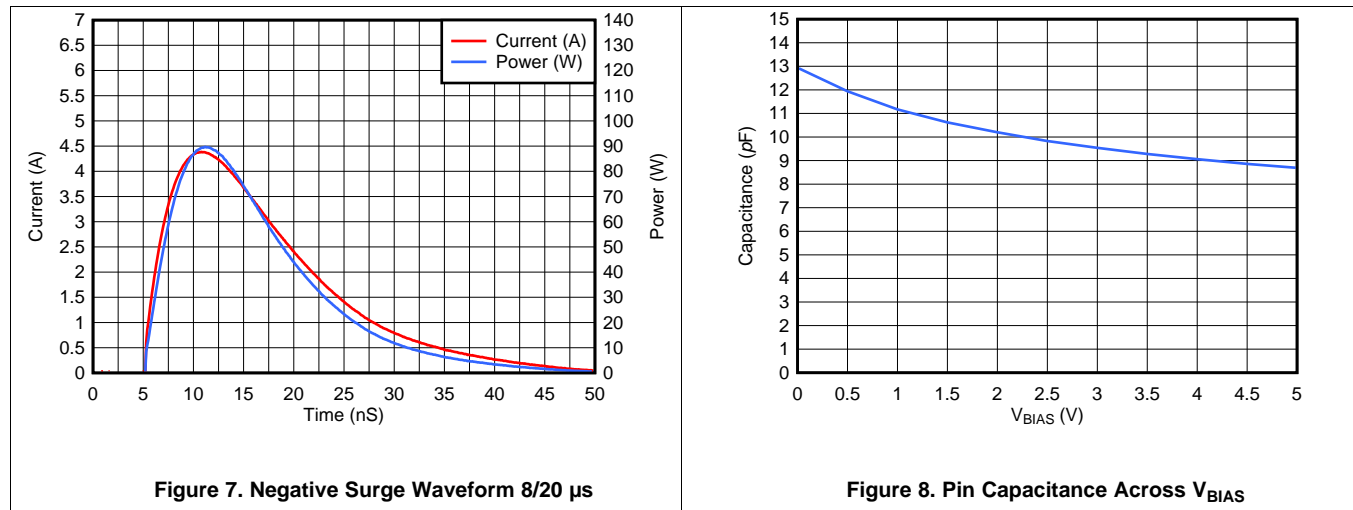


Figure 6. Positive Surge Waveform 8/20 μs

Typical Characteristics (continued)

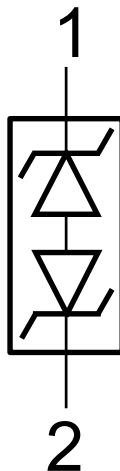


7 Detailed Description

7.1 Overview

TPD1E10B09 is a single-channel ESD TVS that provides ± 20 -kV IEC 61000-4-2 (Level 4) contact and air-gap ESD protection. The 10-pF back-to-back diode architecture is suitable for signals that range from -9 V to 9 V and supports data rates up to 500 Mbps. The industry-standard 0402 package is convenient for placement in applications with limited space.

7.2 Functional Block Diagram



7.3 Feature Description

TPD1E10B09 is a bidirectional TVS with high ESD protection level. This device protects circuit from ESD strikes up to ± 20 -kV contact and ± 20 -kV air-gap specified in the IEC 61000-4-2 level 4 international standard. The device can also handle up to 4.5-A surge current (IEC 61000-4-5 8/20 μ s). The I/O capacitance of 10 pF supports a data rate up to 500 Mbps. This clamping device has a small dynamic resistance of 0.5Ω typically. This makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 13 V when the device is taking 1-A transient current. The breakdown is bidirectional so that this protection device is a good fit for GPIO, especially audio lines which carry bidirectional signals. Low leakage allows the diode to conserve power when working below the V_{RWM} . The industrial temperature range of -40°C to 125°C makes this ESD device work at extensive temperatures in most environments. The space-saving 0402 package can fit into small electronic devices like mobile equipment and wearables.

7.4 Device Functional Modes

TPD1E10B09 is a passive clamp that has low leakage during normal operation when the voltage between pin 1 and pin 2 is below V_{RWM} and activates when the voltage between pin 1 and pin 2 goes above V_{BR} . During IEC ESD events, transient voltages as high as ± 20 kV can be clamped between the two pins. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E10B09 is a single-channel back-to-back diode that protects one bidirectional signal line from electrostatic discharge and surge pulses. Because the diode is bidirectional, TPD1E10B09 protects signals that have positive or negative polarity. During normal operation, the diode behaves as a 10-pF capacitance to ground. Board layout is critical for optimal performance of any diode.

Placement: The diode should be placed very close to the external connector for optimal performance. Ideally, the diode should be placed on the line that it is protecting.

Layout: Pin 1 of the diode should be right over the protected signal line. There should a thick and short trace from pin 2 to ground. An example is shown in [Layout](#).

8.2 Typical Application

A system with a human interface is vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these connectors. TPD1E10B09 is a single-channel ESD protection device containing back-to-back TVS diodes, which is typically used to provide a path to ground for dissipating ESD events on bidirectional signal lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP} , to a tolerable level to the protected IC.

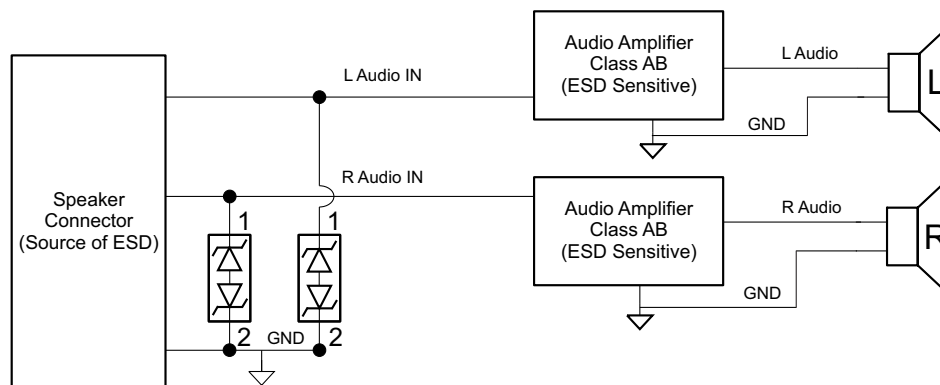


Figure 10. Typical Application Schematic

8.2.1 Design Requirements

For this design example, two TPD1E10B09s will be used to protect left and right audio channels. [Table 1](#) lists the known system parameters for this audio application.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Audio Amplifier Class	AB
Audio signal voltage range	–8 V to 8 V
Audio frequency content	20 Hz to 20 kHz
Required IEC 61000-4-2 ESD Protection	±15-kV Contact/ ±15-kV Air-Gap

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

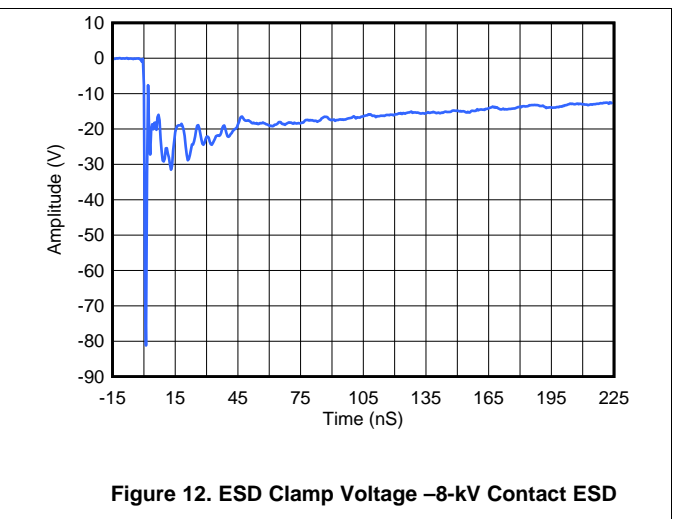
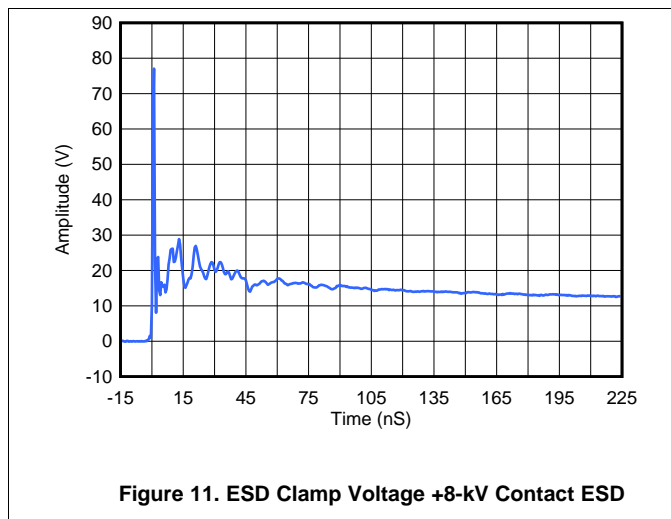
- The voltage range on the protected line does not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM}).
- The operating frequency is supported by the I/O capacitance, C_{IO} , of the TVS diode.
- The IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the audio signal voltage range is -8 V to 8 V . The V_{RWM} for the TVS is -9.5 V to 9.5 V ; therefore, the bidirectional TVS will not break down during normal operation, and normal operation of the audio signal will not be affected due to the signal voltage range. In this application, a bidirectional TVS like TPD1E10B09 is required.

Next, consider the frequency content of this audio signal. In this application with the class AB amplifier, the frequency content is from 20 Hz to 20 kHz ; ensure that the TVS I/O capacitance will not distort this signal by filtering it. With TPD1E10B09 typical capacitance of 10 pF , which leads to a typical cutoff frequency of just under 500 MHz , this diode has sufficient bandwidth to pass the audio signal without distorting it.

Finally, the human interface in this application requires protection for $\pm 15\text{-kV}$ Contact and $\pm 15\text{-kV}$ Air-Gap ESD, which is above the standard Level 4 IEC 61000-4-2 system-level ESD protection. A standard TVS cannot survive this level of IEC ESD stress. However, TPD1E10B09 can survive at least $\pm 20\text{-kV}$ Contact and $\pm 20\text{-kV}$ Air-Gap ESD. Therefore, the device can provide sufficient ESD protection for the interface, even though the requirements are stringent. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. See [Layout](#) for instructions on properly laying out TPD1E10B09.

8.2.3 Application Curves



9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, so there is no need to power it. Do not violate the maximum specifications for each pin.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
 - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
 - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Use rounded corners with the largest radii possible on the protected traces between the TVS and the connector, thus eliminating any sharp corners.
 - Electric fields tend to build up on corners, increasing EMI coupling.
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path.

10.2 Layout Example

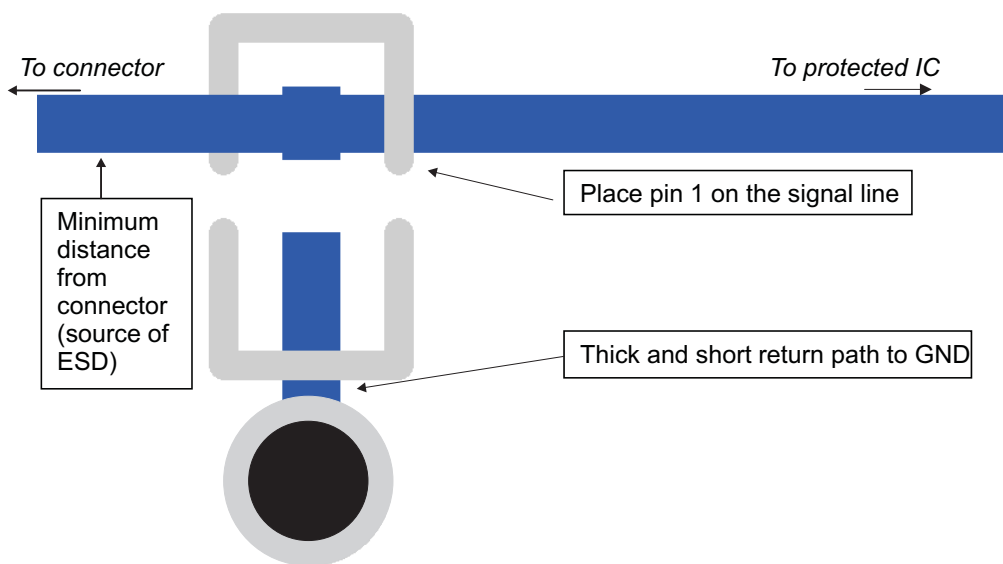


Figure 13. Layout Example

11 器件和文档支持

11.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E10B09DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(A1, A2, A6, BJ)	Samples
TPD1E10B09DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		(A1, A2, A6, BJ)	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E10B09DPYR	X1SON	DPY	2	10000	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E10B09DPYR	X1SON	DPY	2	10000	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B09DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	8.4	0.07	1.1	0.47	2.0	8.0	Q1
TPD1E10B09DPYT	X1SON	DPY	2	250	180.0	9.5	0.73	1.13	0.5	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E10B09DPYR	X1SON	DPY	2	10000	203.2	196.8	33.3
TPD1E10B09DPYR	X1SON	DPY	2	10000	184.0	184.0	19.0
TPD1E10B09DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0
TPD1E10B09DPYT	X1SON	DPY	2	250	205.0	200.0	33.0
TPD1E10B09DPYT	X1SON	DPY	2	250	184.0	184.0	19.0
TPD1E10B09DPYT	X1SON	DPY	2	250	203.2	196.8	33.3
TPD1E10B09DPYT	X1SON	DPY	2	250	189.0	185.0	36.0

DPY (R-PX1SON-N2)

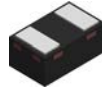
PLASTIC SMALL OUTLINE NO-LEAD



4211012/D 08/14

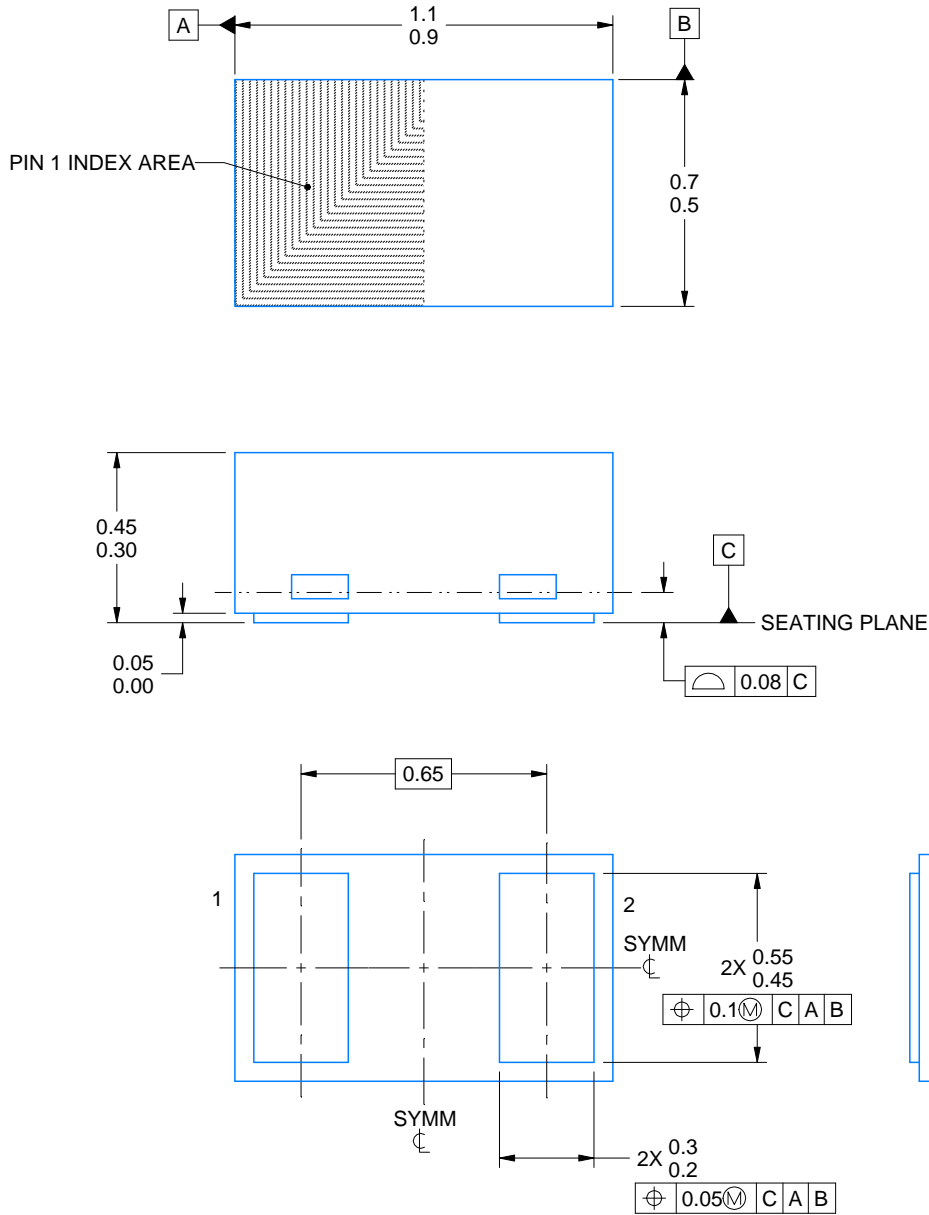
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - This drawing is subject to change without notice.
 - SON (Small Outline No-Lead) package configuration.

DPY0002A



PACKAGE OUTLINE
X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4224561/B 03/2021

NOTES:

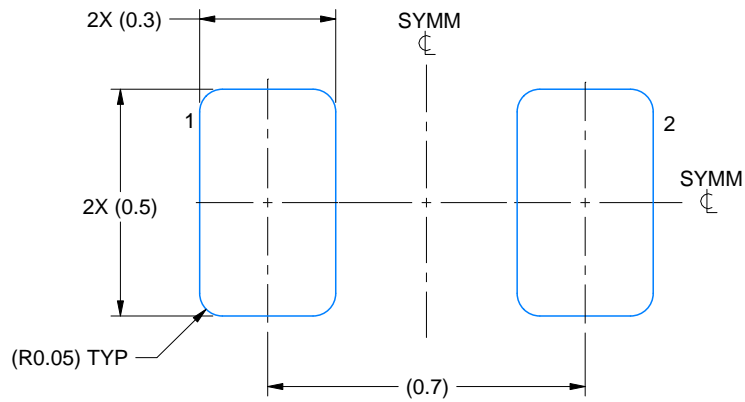
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

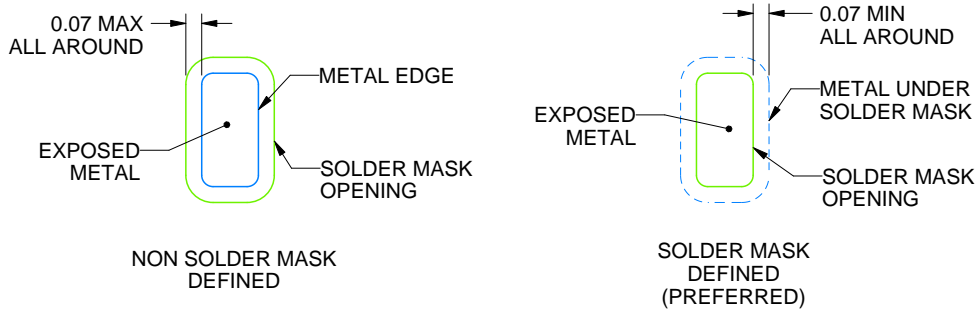
DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

4224561/B 03/2021

NOTES: (continued)

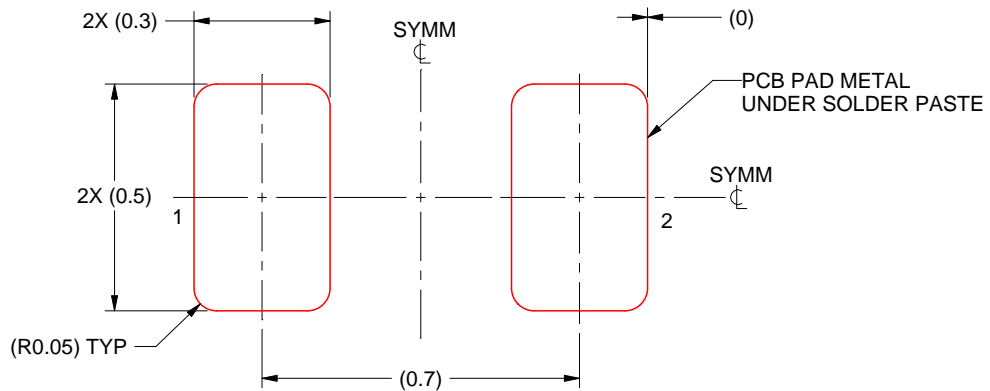
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224561/B 03/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021，德州仪器 (TI) 公司