TPD6F002-Q1 面向 LCD 显示屏和 FPD-Link 的汽车类 ESD 保护和 EMI 滤波器

1 特性

- 符合 AEC-Q101 标准
- 针对数据端口的 6 通道电磁干扰 (EMI) 滤波
  - 100MHz 频率下的串扰衰减为 –47dB
  - 800MHz 频率下的插入损耗为 –30dB
  - 100MHz 频率下的的带宽为 –3dB
- Pi 型 (C-R-C) 滤波器配置
  （R = 100Ω，C_{TOTAL} = 34pF）
- 优异的静电放电 (ESD) 保护，超过了 IEC 61000-4-2
  标准（4 级）
  - ±20kV IEC 61000-4-2 接触放电
  - ±30kV IEC 61000-4-2 气隙放电
- 低泄漏电流 20nA（最大值）
- 采用节省空间的小外形尺寸无引线 (SON) 封装 (3mm × 1.35mm)

2 应用

- 液晶显示屏 (LCD) 显示接口
- 通用输入/输出 (GPIO)
- 存储器接口
- 采用柔性电缆的数据线
- FPD-Link

3 说明

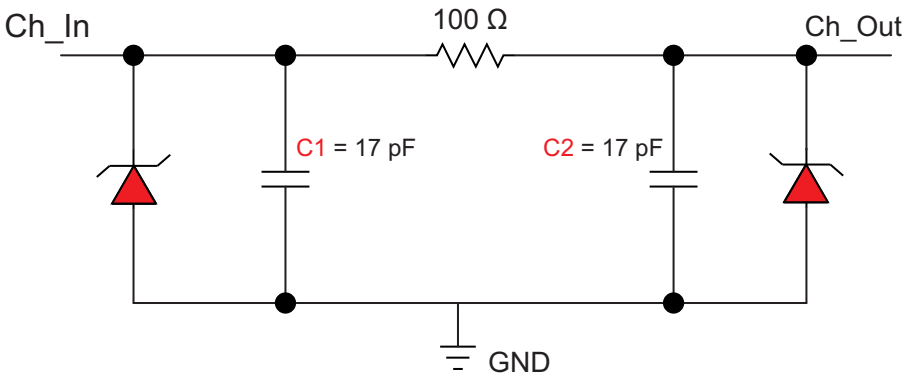
TPD6F002-Q1 是一款高度集成的器件，该器件提供有 6 通道 EMI 滤波器和基于瞬态电压抑制器 (TVS) 的 ESD 保护二极管阵列。 低通滤波器阵列可为数据端口抑制 EMI/射频干扰 (RFI) 辐射，防止其受到电磁干扰。 TVS 二极管阵列的额定 ESD 冲击消散值高于 IEC 61000-4-2 国际标准中规定的最高水平。 此器件高度集成，并且采用易于布线的小型 DSV 封装，可对 LCD 显示屏、存储器接口、GPIO 线和 FPD-Link 提供强力的电路保护。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD6F002-Q1	SON (12)	3.00mm x 1.35mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

4 简化电路原理图



9.2 Typical Application

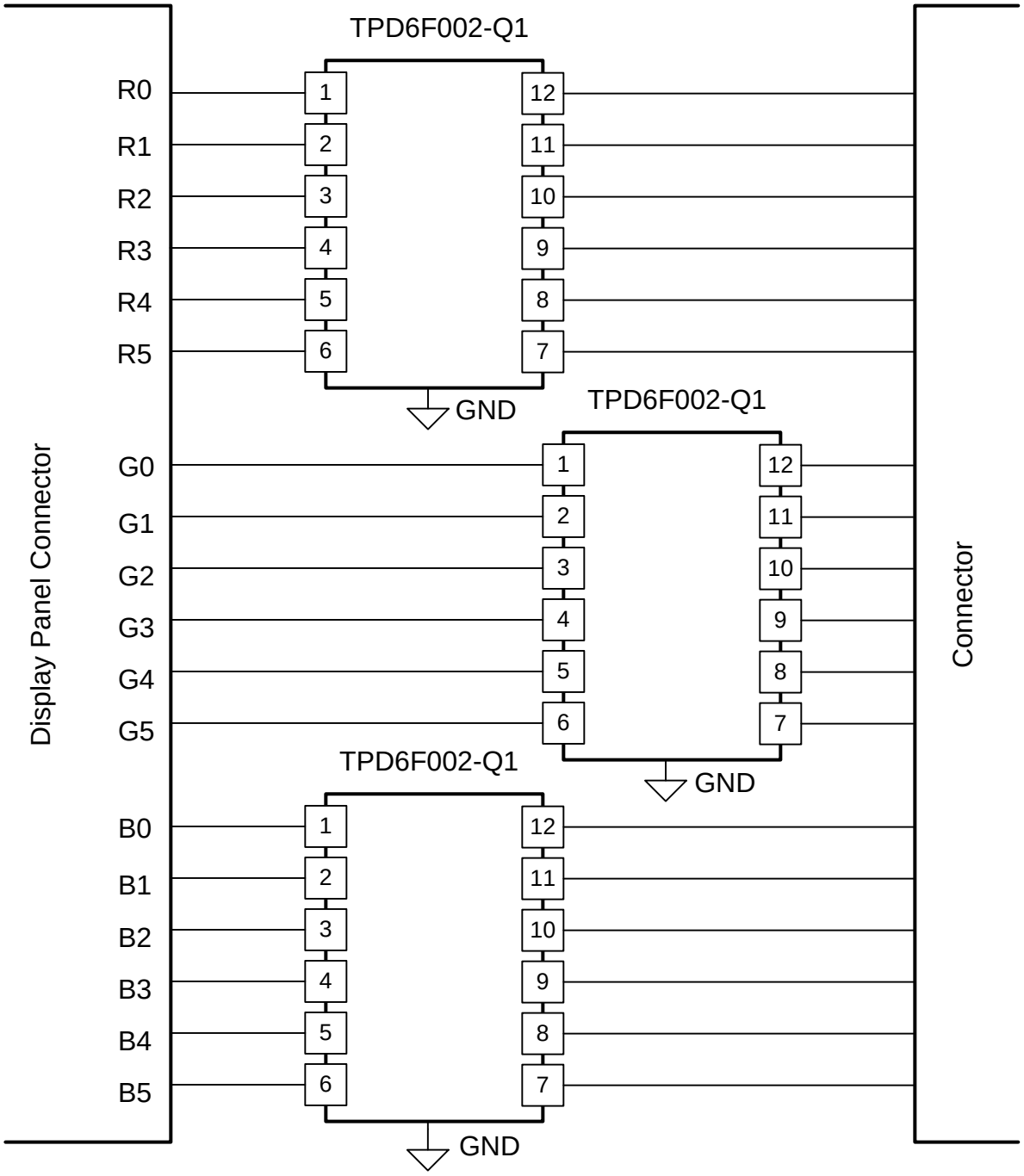


Figure 7. Display Panel Schematic

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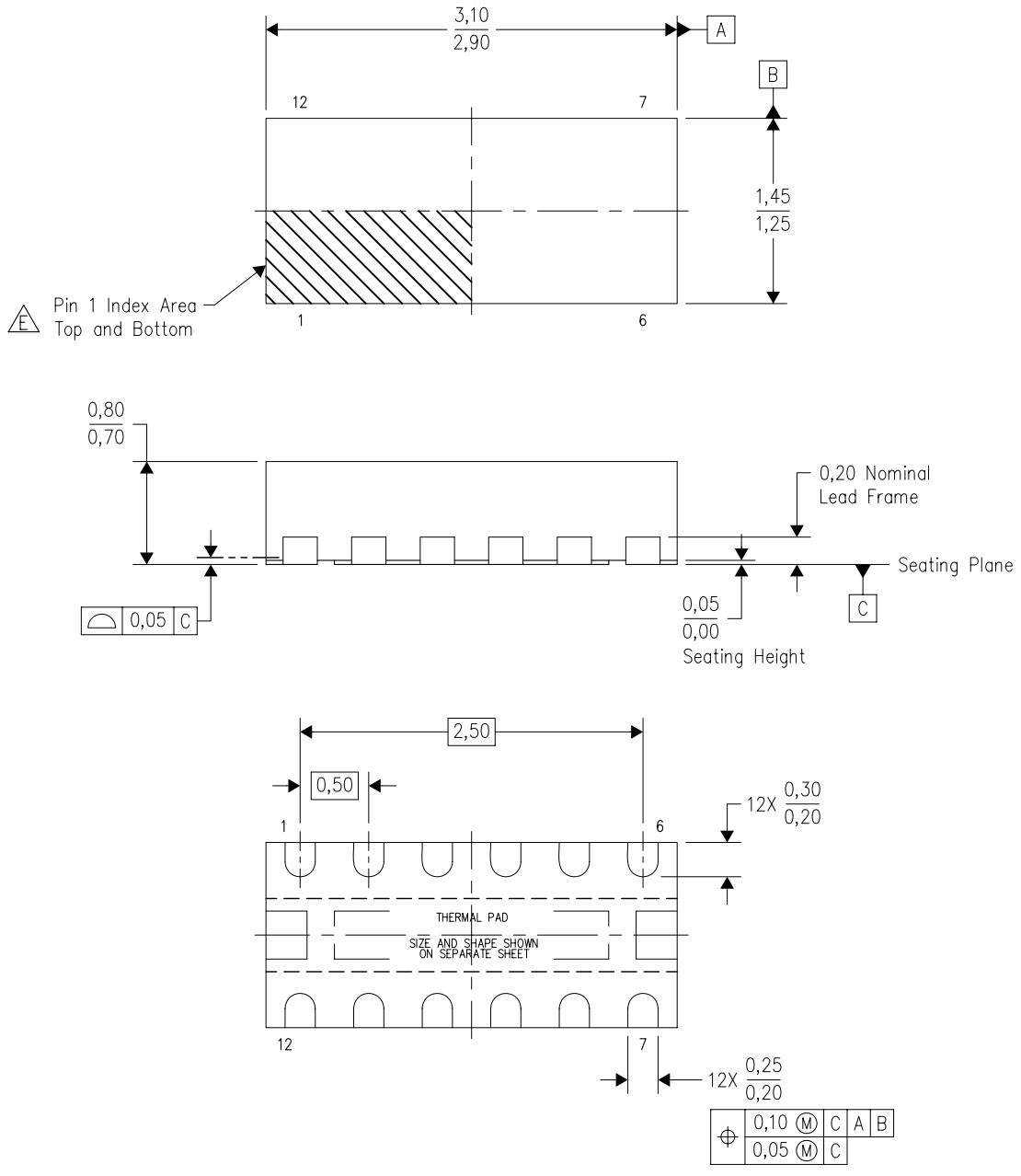
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD6F002QDSVRQ1	SON	DSV	12	3000	213.0	191.0	35.0

DSV (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

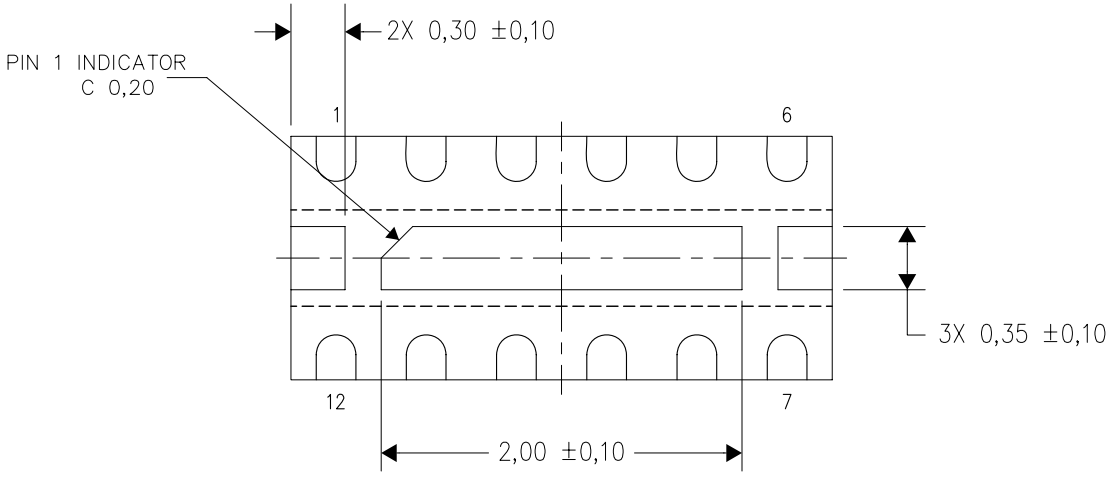
DSV (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



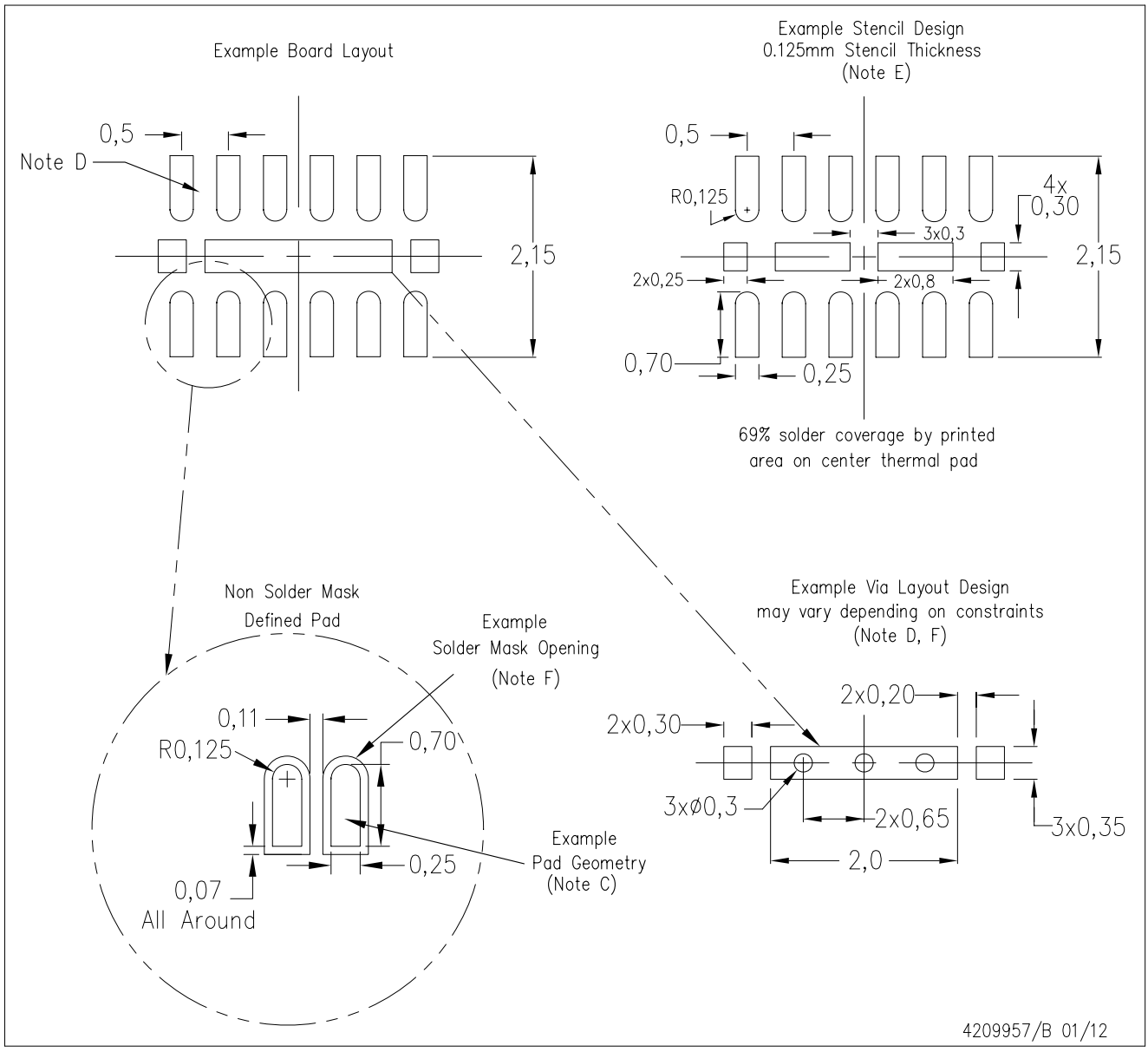
Bottom View

Exposed Thermal Pad Dimensions

4209318/B 12/11

NOTE: All linear dimensions are in millimeters

DSV (R–PWSON–N12) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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