TEXAS INSTRUMENTS
TPS62933, TPS62932, TPS62933F, TPS62933P, TPS62933O
ZHCSO99D – JUNE 2021 – REVISED AUGUST 2022

TPS6293x 采用 SOT583 封装的 3.8V 至 30V、2A/3A 同步降压转换器

1 特性

- 广泛地为各种应用配置
  - 3.8V 至 30V 输入电压范围
  - 0.8V 至 22V 输出电压范围
  - 超低静态电流：12 μA（TPS62932、TPS62933 和 TPS62933P）
  - 集成式 76mΩ 和 32mΩ MOSFET
  - 0.8 V ± 1% 基准电压 (25°C)
  - 以最大 98% 的占空比运行
  - 精密 EN 阈值
  - 2A (TPS62932) 和 3A（TPS62933 和 TPS62933x）持续输出电流
  - –40°C 至 150°C 的工作结温范围
- 大量兼容引脚的选件
  - TPS62932、TPS62933 和 TPS62933F 的 SS 引脚可实现可调软启动时间
  - TPS62933P 和 TPS62933O 的 PG 引脚用作电源良好指示器
  - TPS62932、TPS62933 和 TPS62933P 可通过脉冲频率调制 (PFM) 实现高轻负载效率
  - TPS62933F 具有强制连续电流调制 (FCCM) 功能
  - TPS62933O 具有 Out-of-Audio (OOA) 功能
- 解决方案尺寸小巧且易于使用
  - 具有内部补偿的峰值电流模式
  - 200kHz 至 2.2MHz 的可选频率
  - 低电磁干扰，具有展频频谱（TPS62932、TPS62933、TPS62933P 和 TPS62933O）
  - 支持预偏置输出启动
  - 用于高侧和低侧 MOSFET 的逐周期过流限制
  - 非闭锁 OTP、OCP、OVP、UVP 和 UVLO 保护
  - 1.6mm × 2.1mm SOT583 封装
- 借助 TPS6293x 并使用 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 楼宇自动化、电器、工业 PC
- 多功能打印机、企业投影仪
- 便携式电子产品、联网外设
- 智能扬声器、监视器
- 具有 5V、12V、19V 和 24V 输入的分布式电源系统

3 说明

TPS6293x 是一款易于使用的高效同步降压转换器，具有 3.8V 至 30V 的宽输入电压范围，并支持高达 2A (TPS62932) 和 3A（TPS62933 和 TPS62933x）的持续输出电流和 0.8V 至 22V 输出电压。

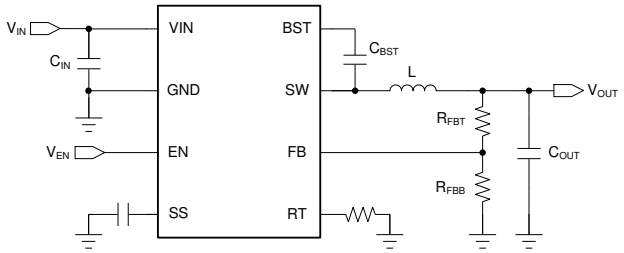
该器件采用定频峰值电流控制模式，可实现快速瞬态响应以及出色的线路和负载调节。内部环路补偿经过优化，无需使用外部补偿元件。

TPS62932、TPS62933 和 TPS62933P 在脉冲频率调制模式下运行，可实现高轻负载效率。TPS62933F 在强制连续电流调制模式下运行，可在所有负载条件下保持较低的输出纹波。TPS62933O 在 Out-of-Audio 模式下运行，可避免可闻噪声。

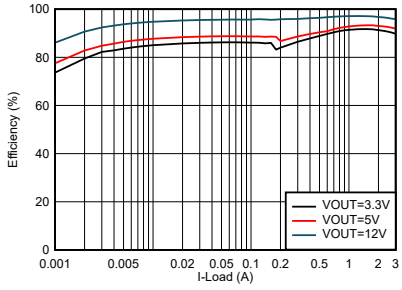
器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS6293x	SOT583 (8)	1.60mm × 2.10mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图



TPS62933 效率（V_{IN} = 24V，f_{SW} = 500kHz）

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (July 2022) to Revision D (August 2022)	Page
• 添加了 TPS62933O	1
• 更改了 TPS6293x 的 WEBENCH® Power Designer 链接	1

Changes from Revision B (February 2022) to Revision C (July 2022)	Page
• 添加了 TPS62933F	1
• 添加了 TPS62933P	1

5 说明（续）

该 ULQ（超低静态）特性有利于延长电池寿命。在 200kHz 至 2.2MHz 范围内，可以通过配置 RT 引脚来设置开关频率，从而优化系统效率、解决方案尺寸和带宽。TPS62932、TPS62933 和 TPS62933F 的软启动时间可通过 SS 引脚上的外部电容器进行调节。TPS62932、TPS62933、TPS62933P 和 TPS62933O 具有展频频谱，有助于降低 EMI 噪声。

TPS6293x 采用 0.5mm 引脚间距的小型 SOT583 (1.6mm × 2.1mm) 封装，并且具有经过优化的引脚排列，可简化 PCB 布局并提供良好的 EMI 性能。

6 Device Comparison Table

Part Number	Output Current	PFM or FCCM or OOA	SS or PG Pin
TPS62932	2 A	PFM	SS
TPS62933	3 A	PFM	SS
TPS62933F	3 A	FCCM	SS
TPS62933P	3 A	PFM	PG
TPS62933O	3 A	OOA	PG

7 Pin Configuration and Functions

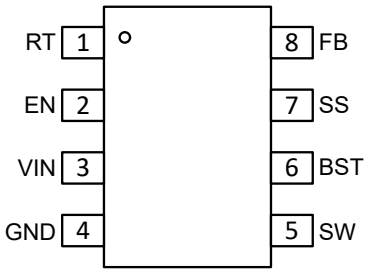


图 7-1. TPS62932, TPS62933, and TPS62933F 8-Pin SOT583 DRL Package (Top View)

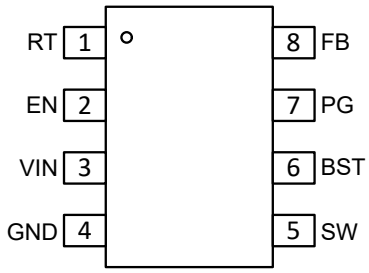


图 7-2. TPS62933P and TPS62933O 8-Pin SOT583 DRL Package (Top View)

表 7-1. Pin Functions

Pin		Type(1)	Description
Name	NO.		
RT	1	A	Frequency programming input. Float for 500 kHz, tie to GND for 1.2 MHz, or connect to an RT timing resistor. See 节 9.3.5 for details.
EN	2	A	Enable input to the converter. Driving EN high or leaving this pin floating enables the converter. An external resistor divider can be used to implement an adjustable V_{IN} UVLO function.
VIN	3	P	Supply input pin to internal LDO and high-side FET. Input bypass capacitors must be directly connected to this pin and GND.
GND	4	G	Ground pin. Connected to the source of the low-side FET as well as the ground pin for the controller circuit. Connect to system ground and the ground side of C_{IN} and C_{OUT}. The path to C_{IN} must be as short as possible.
SW	5	P	Switching output of the convertor. Internally connected to the source of the high-side FET and drain of the low-side FET. Connect to the power inductor.
BST	6	P	Bootstrap capacitor connection for high-side FET driver. Connect a high-quality, 100-nF ceramic capacitor from this pin to the SW pin.

表 7-1. Pin Functions (continued)

Pin		Type(1)	Description
Name	NO.		
SS/PG	7	A	TPS62932, TPS62933, and TPS62933F soft-start control pin. An external capacitor connected to this pin sets the internal voltage reference rising time. See 节 9.3.7 for details. A minimum 6.8-nF ceramic capacitor must be connected at this pin, which sets the minimum soft-start time to approximately 1 ms. Do not float.
		A	TPS62933P and TPS62933O open-drain power good indicator, which is asserted low if output voltage is out of PG threshold, overvoltage, or if the device is under thermal shutdown, EN shutdown, or during soft start.
FB	8	A	Output feedback input. Connect FB to the tap of an external resistor divider from the output to GND to set output voltage.

(1) A = Analog, P = Power, G = Ground

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C , unless otherwise noted(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	32	V
	EN	–0.3	6	
	FB	–0.3	6	
Output voltage	SW, DC	–0.3	32	
	SW, transient < 10 ns	–3	33	
	BST	–0.3	SW + 6	
	BST – SW	–0.3	6	
	SS/PG	–0.3	6	
	RT	–0.3	6	
T_J	Operating junction temperature(2)	–40	150	°C
T_{stg}	Storage temperature	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Operating at junction temperatures greater than 150°C, although possible, degrades the lifetime of the device.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted(1)

			MIN	NOM	MAX	UNIT
Input voltage	V_{IN}		3.8		30	V
	EN		–0.1		5.5	
	FB		–0.1		5.5	
	PG		–0.1		5.5	
Output voltage	V_{OUT}		0.8		22	
	SW, DC		–0.1		30	
	SW, transient < 10 ns		–3		32	
	BST		–0.1		SW + 5.5	
	BST-SW		–0.1		5.5	
Ouput current	I_{OUT}	TPS62933, TPS62933x	0		3	A
		TPS62932	0		2	
Temperature	Operating junction temperature, T_J		–40		150	°C

(1) The *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For compliant specifications, see the *Electrical Characteristics*.

8.4 Thermal Information

THERMAL METRIC(1)		TPS6293x		UNIT
		DRL (SOT583), 8 PINS		
		JEDEC(2)	EVM(3)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	N/A	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.1	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.3	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.6	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.2	N/A	°C/W
$R_{\theta JA\_EVM}$	Junction-to-ambient thermal resistance on official EVM board	N/A	60.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were simulated on a standard JEDEC board. They do not represent the performance obtained in an actual application.
(3) The real $R_{\theta JA}$ is tested on TI EVM (2 layer, 2-ounce copper thickness).

8.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +150°C, V_{IN} = 3.8 V to 30 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		3.8		30	V
I_Q	Nonswitching quiescent current	EN = 5 V, V_{FB} = 0.85 V, TPS62932, TPS62933, and TPS62933P		12		µA
		EN = 5 V, V_{FB} = 1 V, TPS62933F		125		
		EN = 5 V, V_{FB} = 1 V, TPS62933O		45		
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V		2		µA
V_{IN_UVLO}	Input undervoltage lockout thresholds	Rising threshold	3.4	3.6	3.8	V
		Falling threshold	3.1	3.3	3.5	V
		Hysteresis		300		mV
ENABLE (EN PIN)						
V_{EN_RISE}	Enable threshold	Rising enable threshold		1.21	1.28	V
V_{EN_FALL}	Disable threshold	Falling disable threshold	1.1	1.17		V
I_p	EN pullup current	V_{EN} = 1.0 V		0.7		µA
I_h	EN pullup hysteresis current	V_{EN} = 1.5 V		1.4		µA
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	FB voltage	T_J = 25°C	792	800	808	mV
		T_J = 0°C to 85°C	788	800	812	mV
		T_J = –40°C to 150°C	784	800	816	mV
I_{FB}	Input leakage current	V_{FB} = 0.8 V			0.15	µA
INTEGRATED POWER MOSFETS						
R_{DSON_HS}	High-side MOSFET on-resistance	T_J = 25°C, V_{BST} – SW = 5 V		76		mΩ
R_{DSON_LS}	Low-side MOSFET on-resistance	T_J = 25°C		32		mΩ
CURRENT LIMIT						
I_{HS_LIMIT}	High-side MOSFET current limit	TPS62933 and TPS62933x	4.2	5	5.8	A
		TPS62932	2.8	3.4	4	

8.5 Electrical Characteristics (continued)

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +150°C, V_{IN} = 3.8 V to 30 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{LS_LIMIT}	Low-side MOSFET current limit	TPS62933 and TPS62933x	2.9	3.8	4.5	A
		TPS62932	2	2.5	3	
I_{LS_NOC}	Reverse current limit	TPS62933F	1.2	2.4	3.6	A
I_{PEAK_MIN}	Minimum peak inductor current	TPS62933, TPS62933P, and TPS62933O		0.75		A
		TPS62932		0.53		
SOFT START (SS PIN)						
I_{SS}	Soft-start charge current	TPS62932, TPS62933, and TPS62933F	4.5	5.5	6.5	µA
T_{SS}	Fixed internal soft-start time	TPS62933P and TPS62933O		2		ms
POWER GOOD (PG PIN)						
V_{PGTH}	PG threshold, V_{FB} percentage	V_{FB} falling, PG high to low		85%		
		V_{FB} rising, PG low to high		90%		
		V_{FB} falling, PG low to high		110%		
		V_{FB} rising, PG high to low		115%		
T_{PG_R}	PG delay time	PG from low to high		70		µs
T_{PG_F}	PG delay time	PG from high to low		18		µs
$V_{IN\_PG\_VALID}$	Minimum V_{IN} for valid PG output	Measured when PG < 0.5 V with 100-kΩ pullup to external 5 V		2	2.5	V
V_{PG_OL}	PG output low-level voltage	I_{PG} = 0.5 mA			0.3	V
I_{PG_LK}	PG leakage current when open drain is high	V_{PG} = 5.5 V	–1		1	µA
OSCILLATOR FREQUENCY (RT PIN)						
f_{SW}	Switching center frequency	RT = floating	450	500	550	kHz
		RT = GND	1000	1200	1350	
		RT = 71.5 kΩ		310		
		RT = 9.09 kΩ		2100		
f_{SW_min}	Minimum switching frequency	TPS62933O		30		kHz
t_{ON_MIN} (1)	Minimum ON pulse width			70		ns
t_{OFF_MIN} (1)	Minimum OFF pulse width			140		ns
t_{ON_MAX} (1)	Maximum ON pulse width			7		µs
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP detect (L→H)	112%	115%	118%	
		Hysteresis		5%		
V_{UVP}	Output UVP threshold	UVP detect (H→L)		65%		
t_{hiccup_ON}	UV hiccup ON time before entering hiccup mode after soft start ends			256		µs
t_{hiccup_OFF}	UV hiccup OFF time before restart			10.5 × t_{SS}		s
THERMAL SHUTDOWN						
T_{SHDN} (1)	Thermal shutdown threshold	Shutdown temperature		165		°C
T_{HYS} (1)		Hysteresis		30		°C
SPREAD SPECTRUM FREQUENCY						
f_m	Modulation frequency			f_{SW} / 128		kHz

8.5 Electrical Characteristics (continued)

The electrical ratings specified in this section apply to all specifications in this document, unless otherwise noted. These specifications are interpreted as conditions that do not degrade the device parametric or functional specifications for the life of the product containing it. T_J = –40°C to +150°C, V_{IN} = 3.8 V to 30 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{spread}	Internal spread oscillator frequency			±6%		

(1) Not production tested, specified by design.

8.6 Typical Characteristics

T_J = –40°C to 150°C, V_{IN} = 12 V, unless otherwise noted.

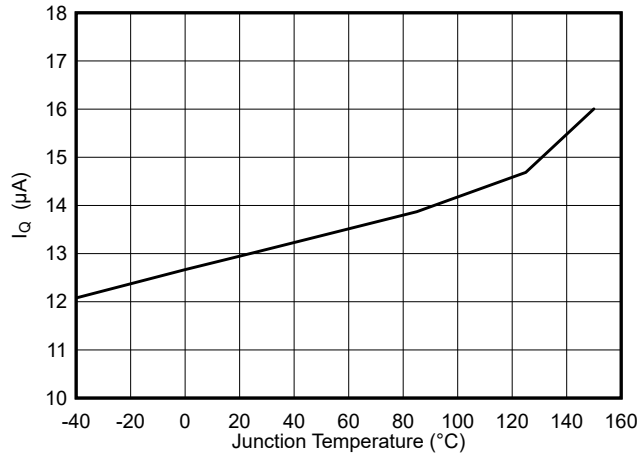


图 8-1. TPS62933 Quiescent Current vs Junction Temperature

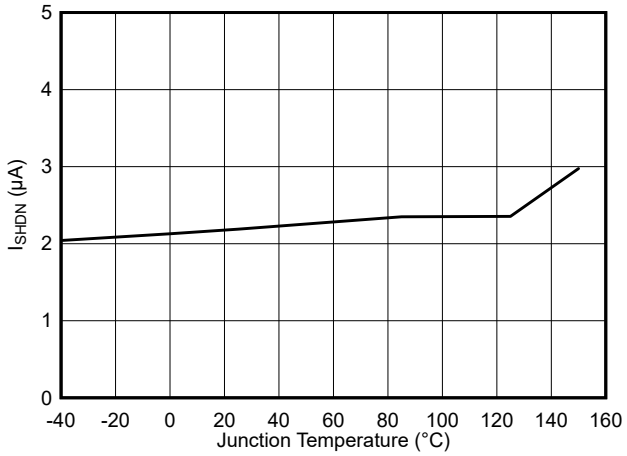


图 8-2. Shutdown Current vs Junction Temperature

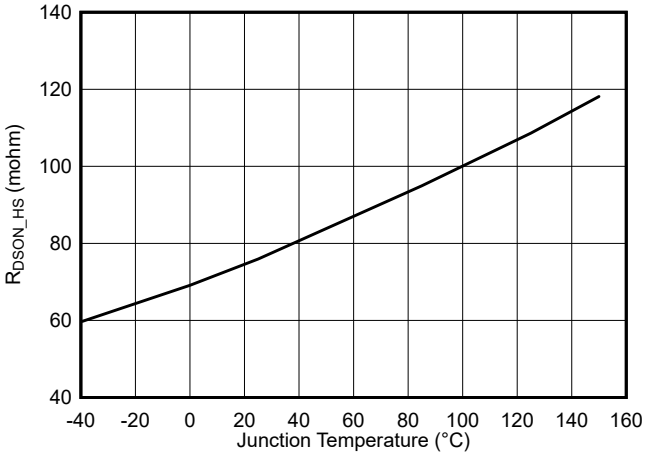


图 8-3. High-Side R_{DSON} vs Junction Temperature

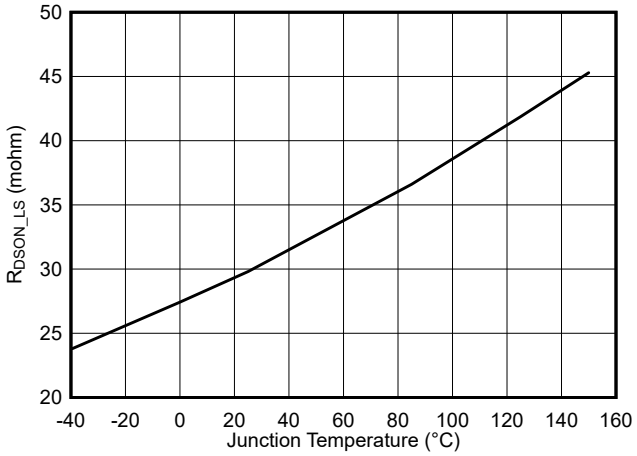


图 8-4. Low-Side R_{DSON} vs Junction Temperature

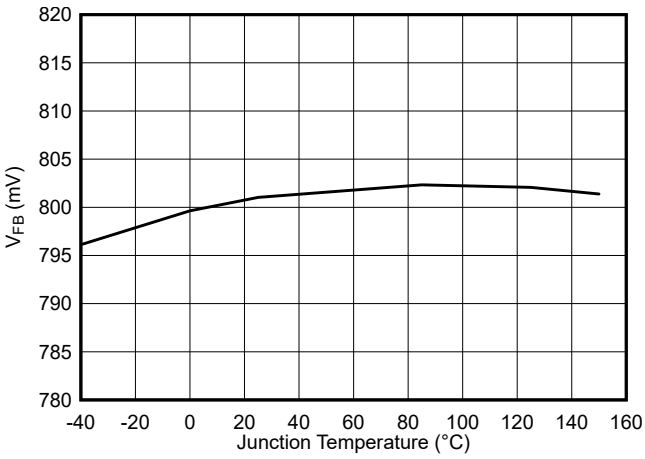


图 8-5. Feedback Voltage vs Junction Temperature

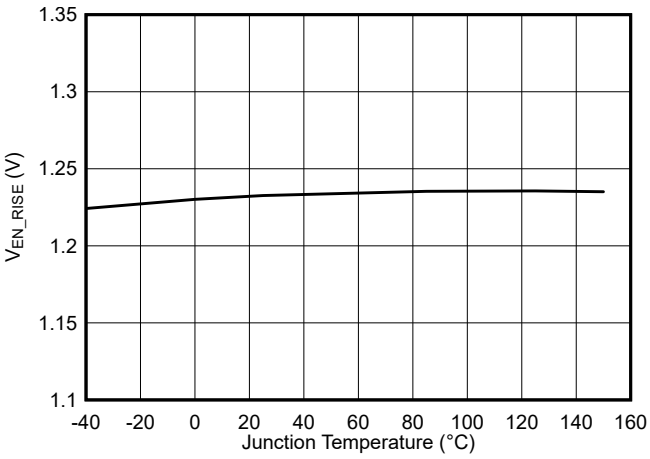


图 8-6. Enable Threshold vs Junction Temperature

8.6 Typical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 12 V, unless otherwise noted.

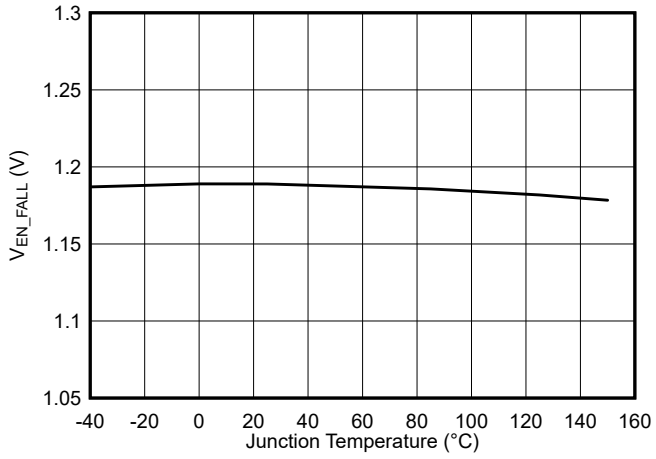


图 8-7. Disable Threshold vs Junction Temperature

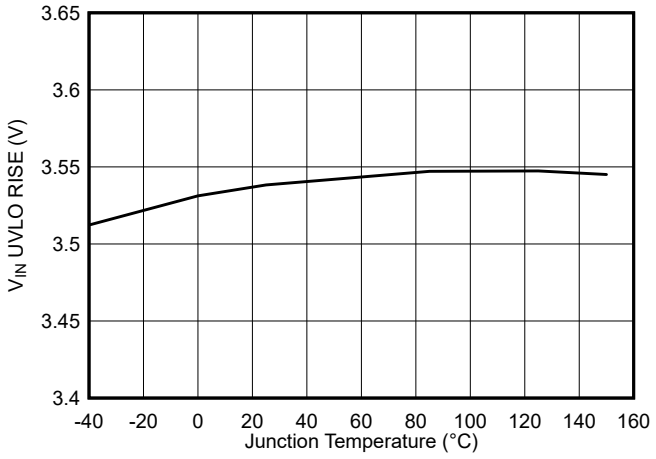


图 8-8. V_{IN} UVLO Rising Threshold vs Junction Temperature

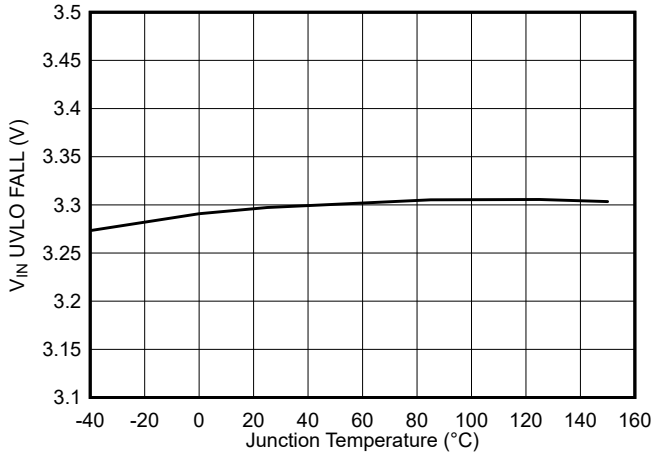


图 8-9. V_{IN} UVLO Falling Threshold vs Junction Temperature

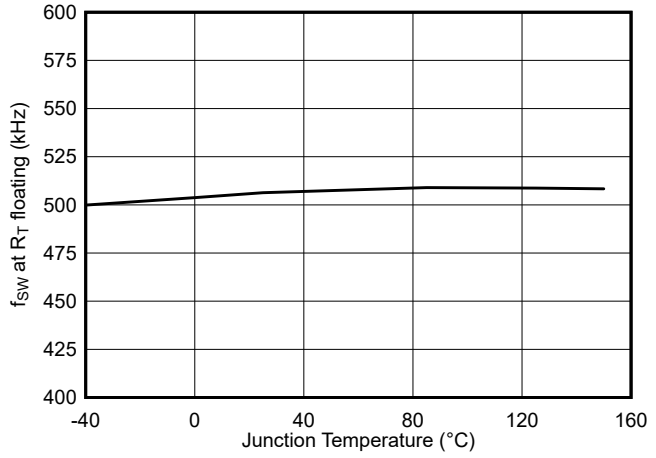


图 8-10. Switching Frequency (RT Floating) vs Junction Temperature

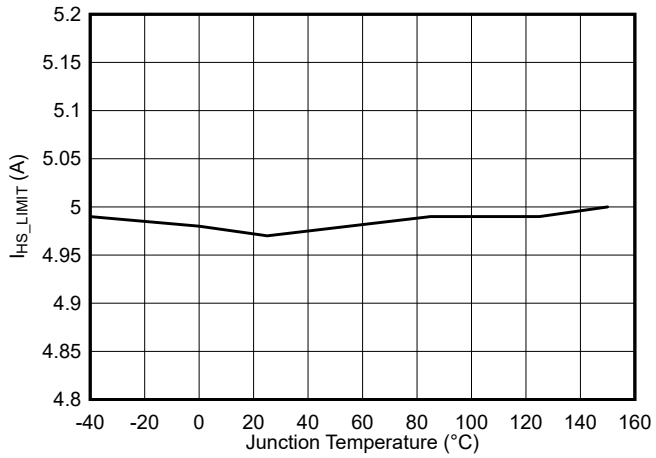


图 8-11. TPS62933 High-Side Current Limit vs Junction Temperature

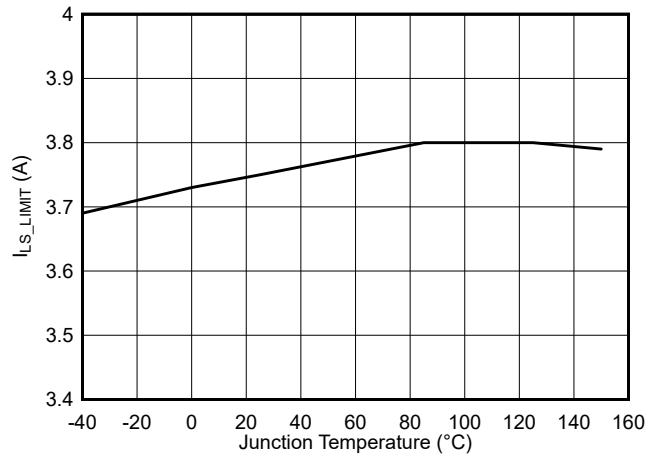


图 8-12. TPS62933 Low-Side Current Limit vs Junction Temperature

8.6 Typical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 12 V, unless otherwise noted.

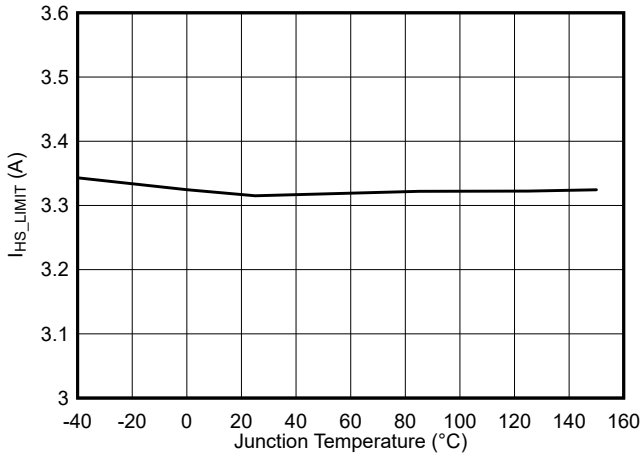


图 8-13. TPS62932 High-Side Current Limit vs Junction Temperature

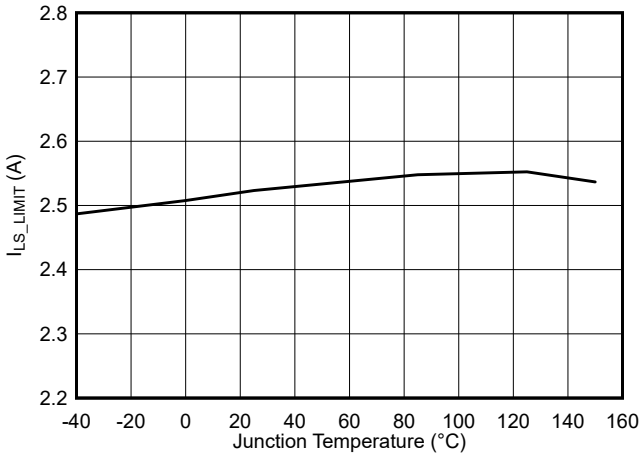


图 8-14. TPS62932 Low-Side Current Limit vs Junction Temperature

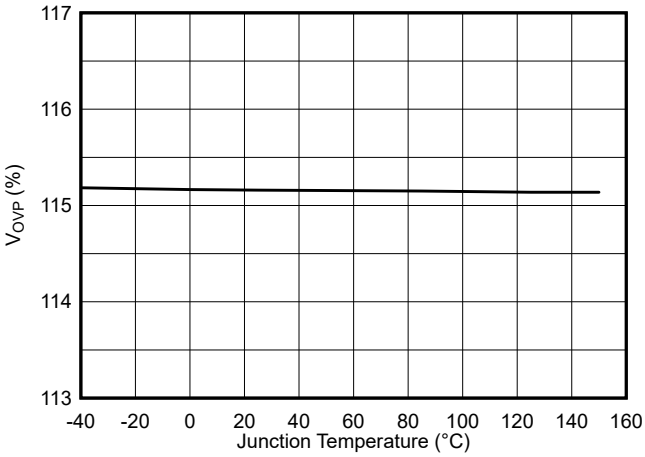


图 8-15. OVP Threshold vs Junction Temperature

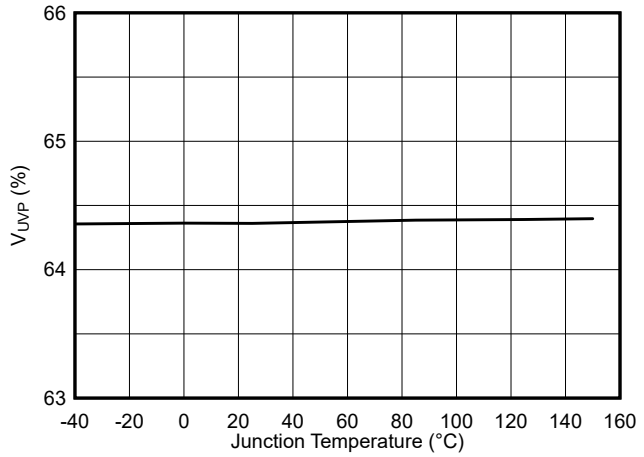


图 8-16. UVP Threshold vs Junction Temperature

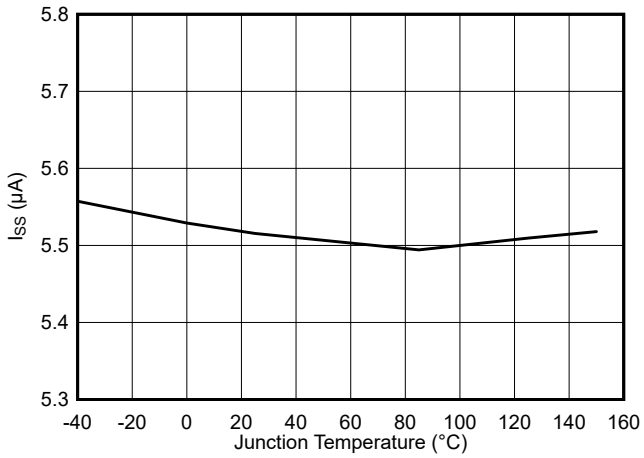


图 8-17. Soft-Start Charge Current vs Junction Temperature

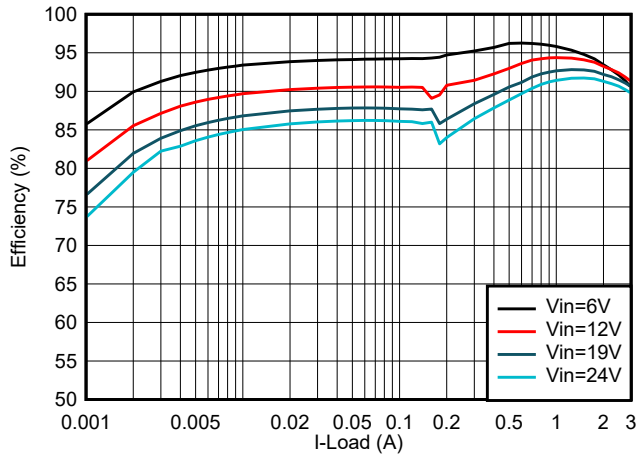


图 8-18. TPS62933 Efficiency, V_{OUT} = 3.3 V, f_{SW} = 500 kHz, L = 4.7 µH

8.6 Typical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 12 V, unless otherwise noted.

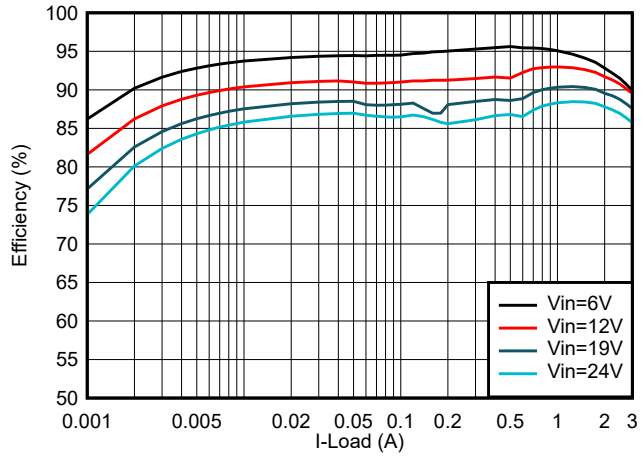


图 8-19. TPS62933 Efficiency, V_{OUT} = 3.3 V, f_{SW} = 1200 kHz, L = 2.2 µH

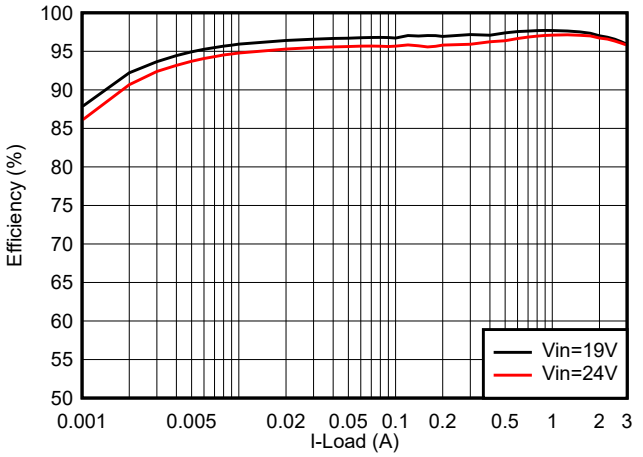


图 8-20. TPS62933 Efficiency, V_{OUT} = 12 V, f_{SW} = 500 kHz, L = 12 µH

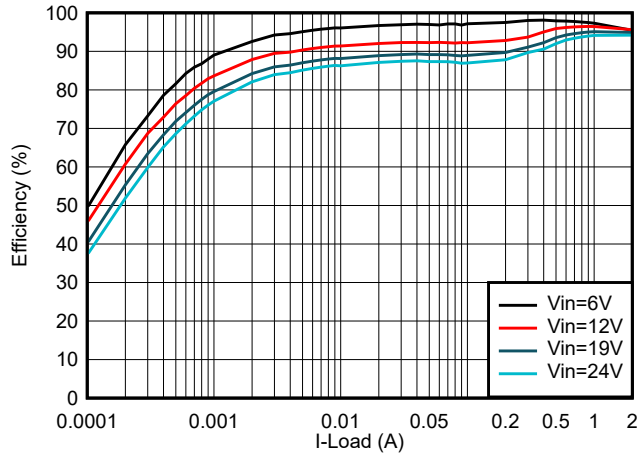


图 8-21. TPS62932 Efficiency, V_{OUT} = 5 V, f_{SW} = 500 kHz, L = 10 µH

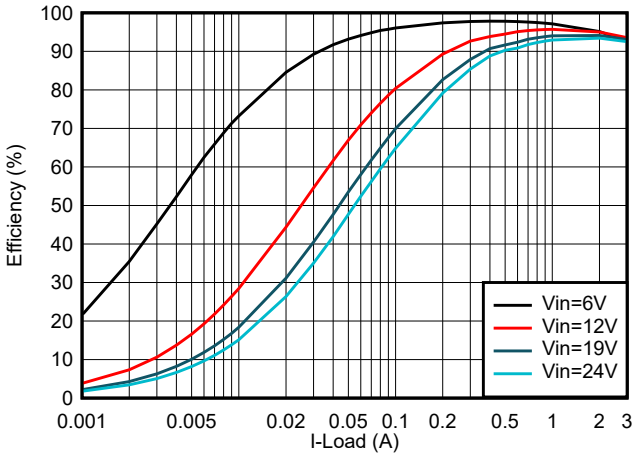


图 8-22. TPS62933F Efficiency, V_{OUT} = 5 V, f_{SW} = 500 kHz, L = 6.8 µH

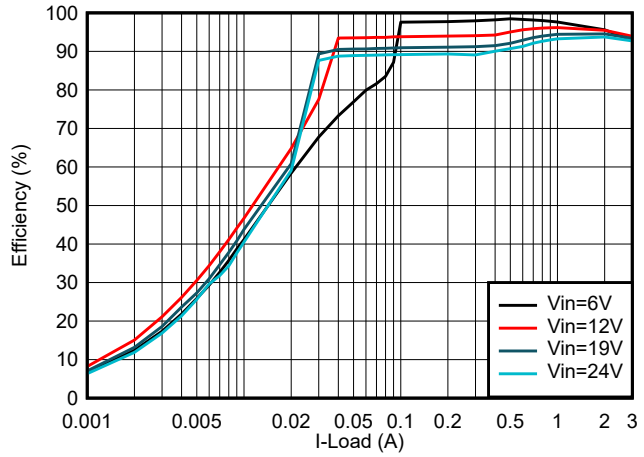


图 8-23. TPS62933O Efficiency, V_{OUT} = 5 V, f_{SW} = 500 kHz, L = 6.8 µH

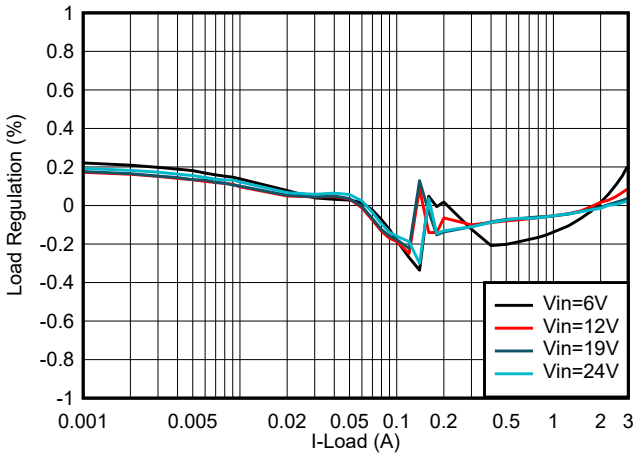


图 8-24. TPS62933 Load Regulation, V_{OUT} = 3.3 V, f_{SW} = 500 kHz

8.6 Typical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 12 V, unless otherwise noted.

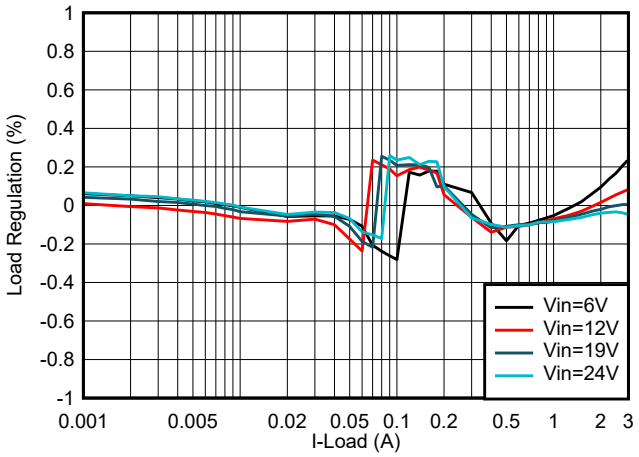


图 8-25. TPS62933 Load Regulation, V_{OUT} = 3.3 V, f_{SW} = 1200 kHz

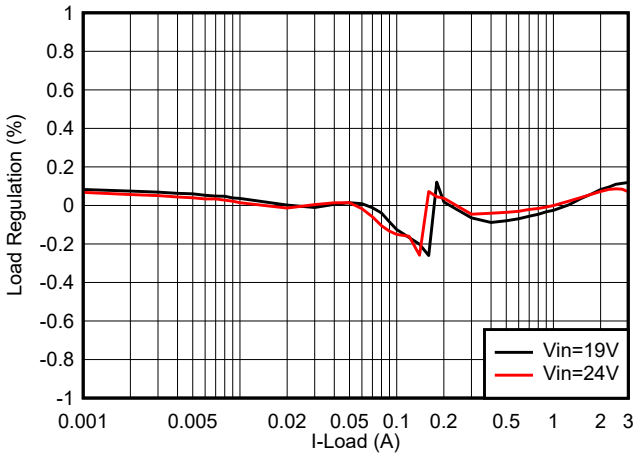


图 8-26. TPS62933 Load Regulation, V_{OUT} = 12 V, f_{SW} = 500 kHz

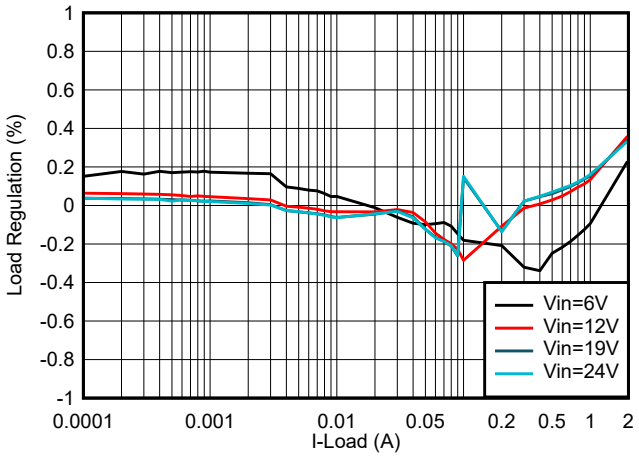


图 8-27. TPS62932 Load Regulation, V_{OUT} = 5 V, f_{SW} = 500 kHz

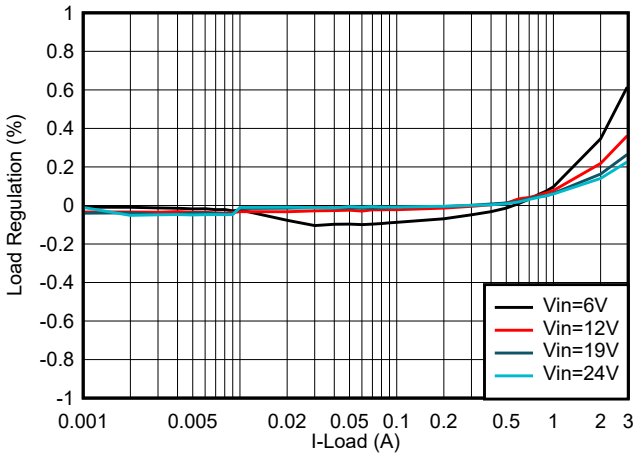


图 8-28. TPS62933F Load Regulation, V_{OUT} = 5 V, f_{SW} = 500 kHz

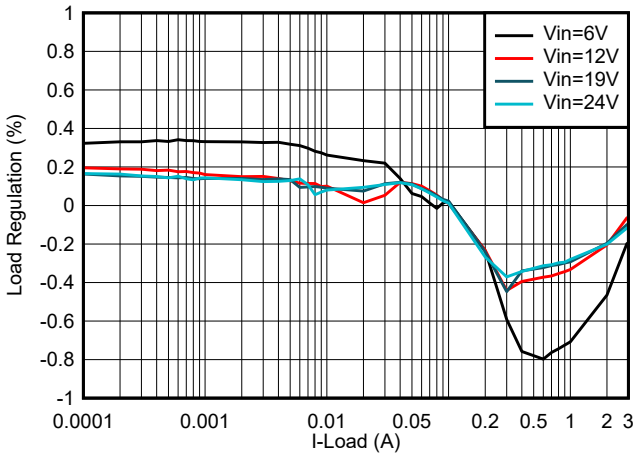


图 8-29. TPS62933O Load Regulation, V_{OUT} = 5 V, f_{SW} = 500 kHz

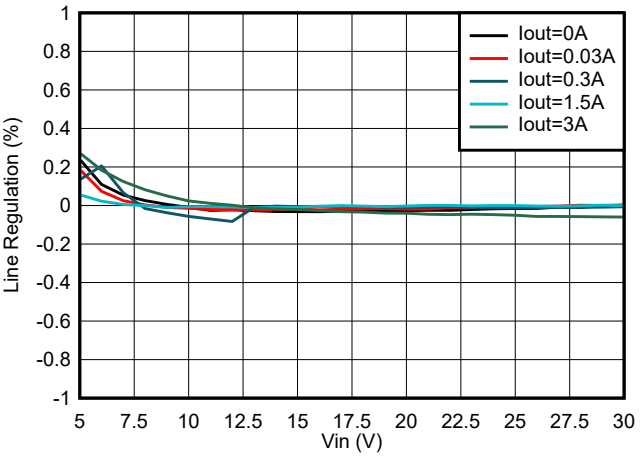


图 8-30. TPS62933 Line Regulation, V_{OUT} = 3.3 V, f_{SW} = 500 kHz

8.6 Typical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 12 V, unless otherwise noted.

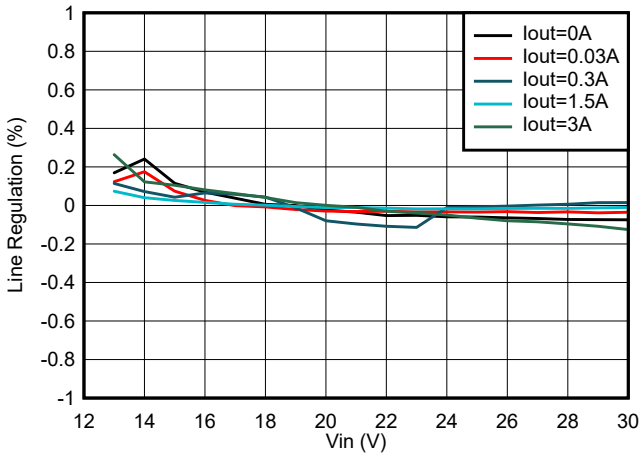


图 8-31. TPS62933 Line Regulation, V_{OUT} = 12 V, f_{SW} = 500 kHz

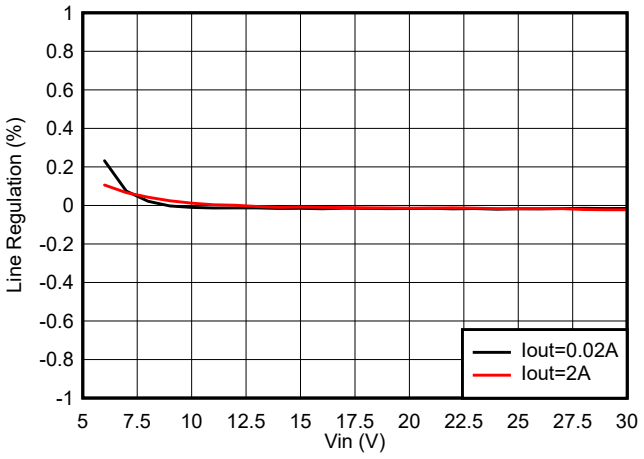


图 8-32. TPS62932 Line Regulation, V_{OUT} = 5 V, f_{SW} = 500 kHz

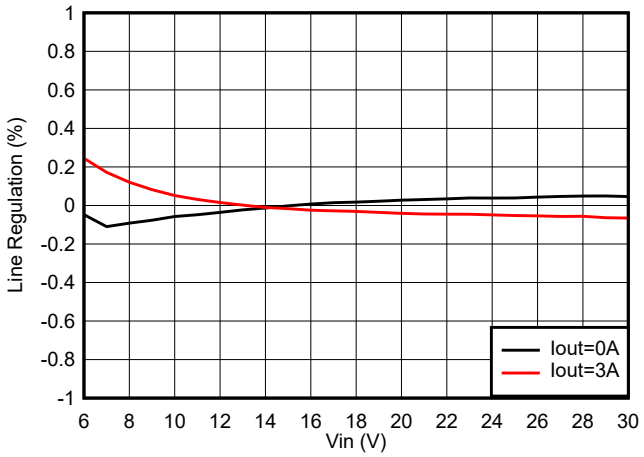


图 8-33. TPS62933F Line Regulation, V_{OUT} = 5 V, f_{SW} = 500 kHz

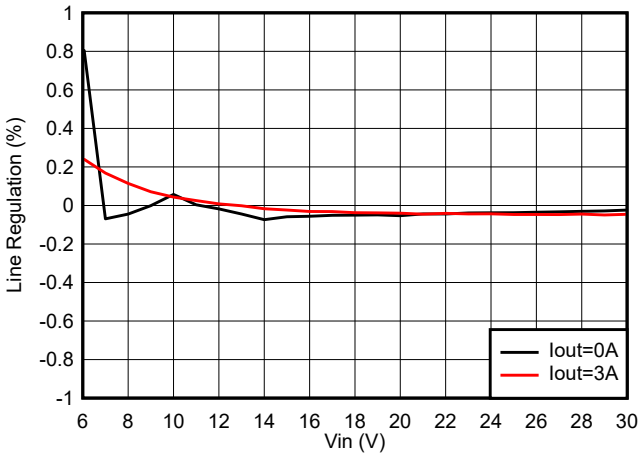


图 8-34. TPS62933O Line Regulation, V_{OUT} = 5 V, f_{SW} = 500 kHz

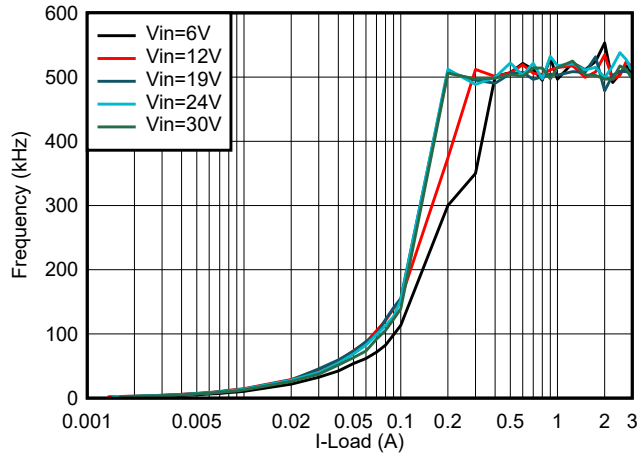


图 8-35. TPS62933 Switching Frequency vs Load Current, V_{OUT} = 3.3 V, f_{SW} = 500 kHz (RT Floating)

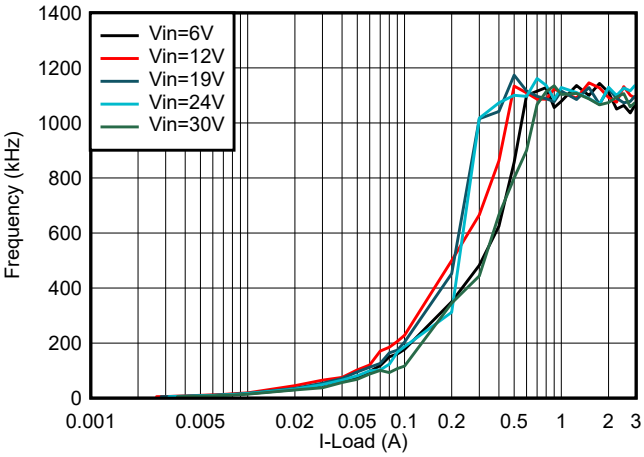


图 8-36. TPS62933 Switching Frequency vs Load Current, V_{OUT} = 3.3 V, f_{SW} = 1200 kHz (RT to GND)

8.6 Typical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 12 V, unless otherwise noted.

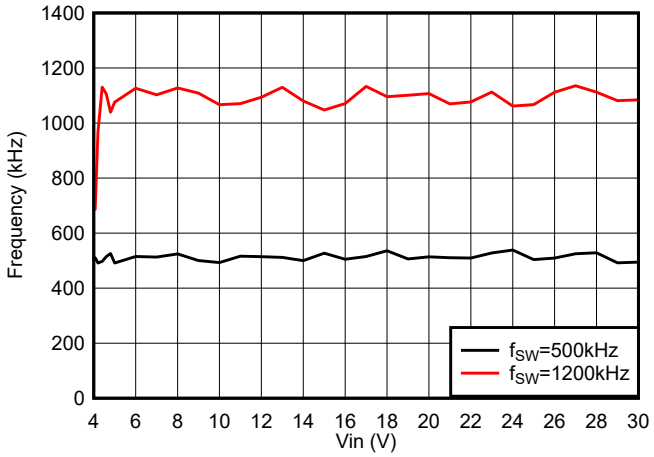


图 8-37. TPS62933 Switching Frequency vs V_{IN}, V_{OUT} = 3.3 V, I_{OUT} = 3 A

9 Detailed Description

9.1 Overview

The TPS62932 and TPS62933x are a 30-V, 2-A and 3-A, synchronous buck (step-down) converters with two integrated n-channel MOSFETs. They employ fixed-frequency peak current control mode for fast transient response and good line and load regulation. With the optimized internal loop compensation, the devices eliminate the external compensation components over a wide range of output voltage and switching frequency.

The integrated 76-mΩ and 32-mΩ MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 2 A (TPS62932) or 3 A (TPS62933 and TPS62933x). The feedback reference voltage is designed at 0.8 V. The output voltage can be stepped down from 0.8 V to 22 V. The devices are ideally suited for systems powered from 5-V, 12-V, 19-V, and 24-V power-bus rails.

The TPS6293x has been designed for safe monotonic start-up into prebiased loads. The default start-up is at V_{IN} equal to 3.8 V. After the device is enabled, the output rises smoothly from 0 V to its regulated voltage. The TPS6293x has low operating current when not switching under no load, especially the TPS62932, TPS62933, and TPS62933P whose operating current is 12 μA (typical). When the TPS6293x is disabled, the supply current is approximately 2 μA (typical). These features are extremely beneficial for long battery life time in low-power operation.

Pulse frequency modulation (PFM) mode allows the TPS62932, TPS62933, and TPS62933P to maximize the light-load efficiency. Continuous current mode allows the TPS62933F to have low output ripple in all load conditions. The TPS62933O operates in out of audio mode which can avoid the audible noise.

The EN pin has an internal pullup current that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the EN pin can be floating for the device to operate with the internal pullup current.

The switching frequency can be set by the configuration of the RT pin in the range of 200 kHz to 2.2 MHz, which allows for efficiency and solution size optimization when selecting the output filter components. The TPS62932, TPS62933, TPS62933P, and TPS62933O also have a frequency spread spectrum feature, which helps with lowering down EMI noise.

A small value capacitor or resistor divider is connected to the SS pin of the TPS62932, TPS62933, and TPS62933F for soft-start time setting or voltage tracking. The TPS62933P and TPS62933O indicate power good through PG pin.

The devices have the on-time extension function with a maximum on time of 7 μs (typical). During low dropout operation, the high-side MOSFET can turn on up to 7 μs, then the high-side MOSFET turns off and the low-side MOSFET turns on with a minimum off time of 140 ns (typical). The devices support the maximum 98% duty cycle.

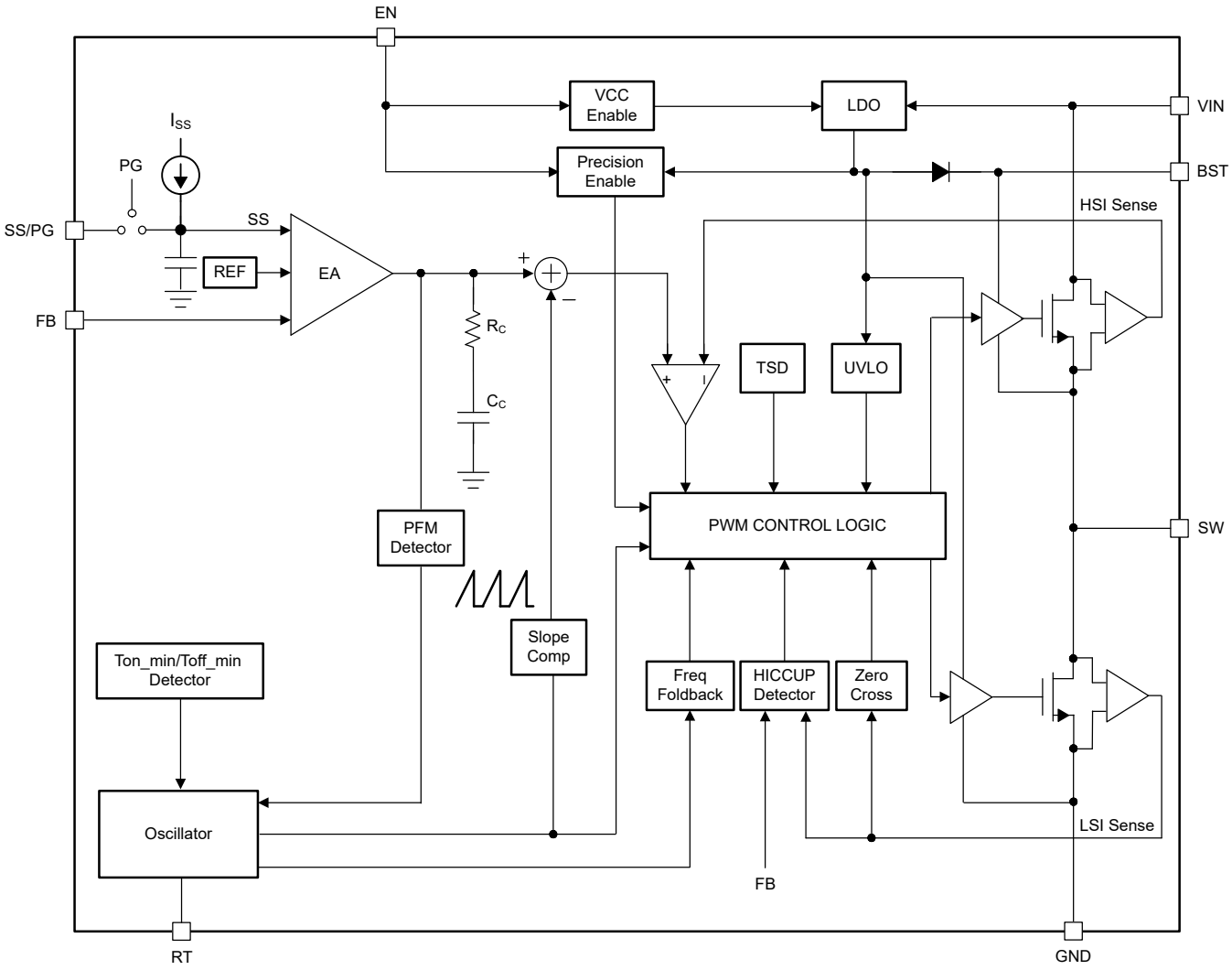
The devices reduce the external component count by integrating the bootstrap circuit. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BST and SW pins. A UVLO circuit monitors the bootstrap capacitor voltage, V_{BST-SW}. When it falls below a preset threshold of 2.5 V (typical), the SW pin is pulled low to recharge the bootstrap capacitor.

Cycle-by-cycle current limiting on the high-side MOSFET protects the device in overload situations and is enhanced by a low-side sourcing current limit, which prevents current runaway. The TPS6293x provides output undervoltage protection (UVP) when the regulated output voltage is lower than 65% of the nominal voltage due to overcurrent being triggered, approximately 256-μs (typical) deglitch time later, both the high-side and low-side MOSFET turn off, the device steps into hiccup mode.

The devices minimize excessive output overvoltage transient by taking advantage of the overvoltage comparator. When the regulated output voltage is greater than 115% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 110%.

Thermal shutdown disables the devices when the die temperature, T_J, exceeds 165°C and enables the devices again after T_J decreases below the hysteresis amount of 30°C.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Fixed Frequency Peak Current Mode

The following operation description of the TPS6293x refers to the functional block diagram and to the waveforms in 图 9-1. The TPS6293x is a synchronous buck converter with integrated high-side (HS) and low-side (LS) MOSFETs (synchronous rectifier). The TPS6293x supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch on time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current, i_L, increases with linear slope (V_{IN} – V_{OUT}) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot – through dead time. Inductor current discharges through the low-side switch with a slope of – V_{OUT} / L. The control parameter of a buck converter is defined as Duty Cycle D = t_{ON} / t_{SW}, where t_{ON} is the high-side switch on time and t_{SW} is the switching period. The converter control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

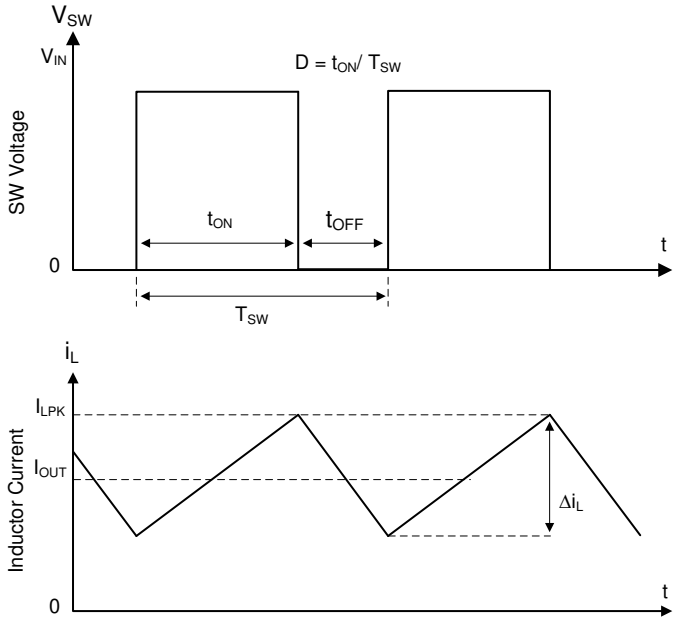


图 9-1. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The TPS6293x employs the fixed-frequency peak current mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the HS switch and compared to the peak current threshold to control the on time of the HS switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors.

9.3.2 Pulse Frequency Modulation

The TPS62932, TPS62933, and TPS62933P are designed to operate in pulse frequency modulation (PFM) mode at light load currents to boost light load efficiency.

When the load current is lower than half of the peak-to-peak inductor current in CCM, the devices operate in discontinuous conduction mode (DCM). In DCM operation, the low-side switch is turned off when the inductor current drops to I_{LS_ZC} to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced CCM operation at light load.

At even lighter current load, pulse frequency modulation (PFM) mode is activated to maintain high-efficiency operation. When either the minimum high-side switch on time, t_{ON_MIN}, or the minimum peak inductor current I_{PEAK_MIN} is reached, the switching frequency decreases to maintain regulation. In PFM mode, the switching

frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions. Since the integrated current comparator catches the peak inductor current only, the average load current entering PFM mode varies with the applications and external output LC filters.

In PFM mode, the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the feedback voltage catches V_{REF}. The periodicity of these bursts is adjusted to regulate the output, while zero current crossing detection turns off the low-side MOSFET to maximize efficiency. This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency.

9.3.3 Voltage Reference

The internal reference voltage, V_{REF}, is designed at 0.8 V (typical). The negative feedback system of converter produces a precise ±2% feedback voltage, V_{FB}, over full temperature by scaling the output of a temperature-stable internal band-gap circuit.

9.3.4 Output Voltage Setting

A precision 0.8-V reference voltage, V_{REF}, is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from the output voltage to the FB pin. TI recommends using 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the bottom-side resistor, R_{FBB}, for the desired divider current and use 方程式 1 to calculate the top-side resistor, R_{FBT}. Lower R_{FBB} increases the divider current and reduces efficiency at very light load. Larger R_{FBB} makes the FB voltage more susceptible to noise, so larger R_{FBB} values require a more carefully designed feedback path on the PCB. Setting R_{FBB} = 10 kΩ and R_{FBT} in the range of 10 kΩ to 300 kΩ is recommended for most applications.

The tolerance and temperature variation of the resistor dividers affect the output voltage regulation.

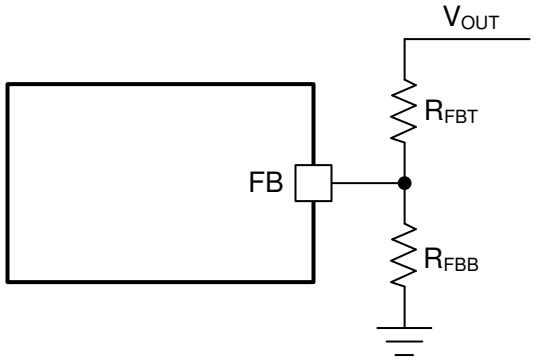


图 9-2. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (1)$$

where

- V_{REF} is the 0.8 V (the internal reference voltage).
- R_{FBB} is 10 kΩ (recommended).

9.3.5 Switching Frequency Selection

The switching frequency is set by the condition of the RT input. The condition of this input is detected when the device is first enabled. Once the converter is running, the switching frequency selection is fixed and cannot be changed until the next power-on cycle or EN toggle. 表 9-1 shows the selection programming. In adjustable frequency mode, the switching frequency can be set between 200 kHz and 2200 kHz by proper selection of RT resistor. See 方程式 2.

$$f_{SW}(kHz) = 17293 \times RT(k\Omega)^{-0.942} \quad (2)$$

where

- RT is the value of RT timing resistor in kΩ.
- f_{SW} is the switching frequency in kHz.

表 9-1. RT Pin Resistor Settings

RT Pin	Resistance	Switching Frequency
Floating	> 280 kΩ	500 kHz
GND	< 1 kΩ	1200 kHz
RT to GND	8.9 kΩ to 111 kΩ	200 kHz to 2200 kHz

图 9-3 indicates the required resistor value for RT to set a desired switching frequency.

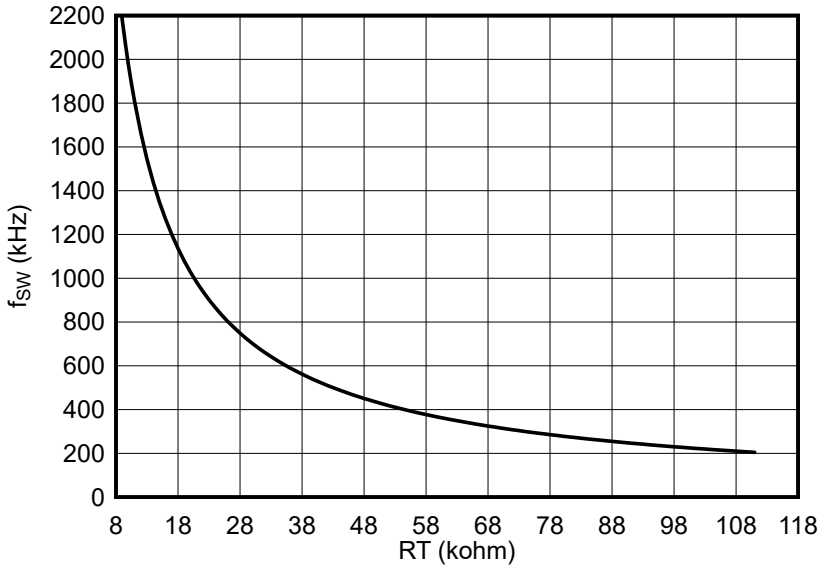


图 9-3. Switching Frequency vs R_T

There are four cases where the switching frequency does not conform to the condition set by the RT pin:

- Light load operation (PFM mode)
- Low dropout operation
- Minimum on-time operation
- Current limit tripped

Under all of these cases, the switching frequency folds back, meaning it is less than that programmed by the RT pin. During these conditions, the output voltage remains in regulation, except for current limit operation.

9.3.6 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage exceeds the enable threshold voltage, V_{EN_RISE}, the TPS6293x begins operation. If the EN pin voltage is pulled below the disable threshold voltage, V_{EN_FALL}, the converter stops switching and enters shutdown mode.

The EN pin has an internal pullup current source, which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use an open-drain or open-collector or GPIO output logic to interface with the pin.

The TPS6293x implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN_UVLO} threshold. The internal V_{IN_UVLO} threshold has a

hysteresis of typical 300 mV. If an application requires a higher UVLO threshold on the VIN pin, the EN pin can be configured as shown in 图 9-4. When using the external UVLO function, setting the hysteresis at a value greater than 500 mV is recommended.

The EN pin has a small pullup current, I_p, which sets the default state of the EN pin to enable when no external components are connected. The pullup hysteresis current, I_h, is used to control the hysteresis voltage for the UVLO function when the EN pin voltage crosses the enable threshold. Use 方程式 3 and 方程式 4 to calculate the values of R1 and R2 for a specified UVLO threshold. Once R1 and R2 are settled down, V_{EN} can be calculated by 方程式 5, which must be lower than 5.5 V with the maximum V_{IN}.

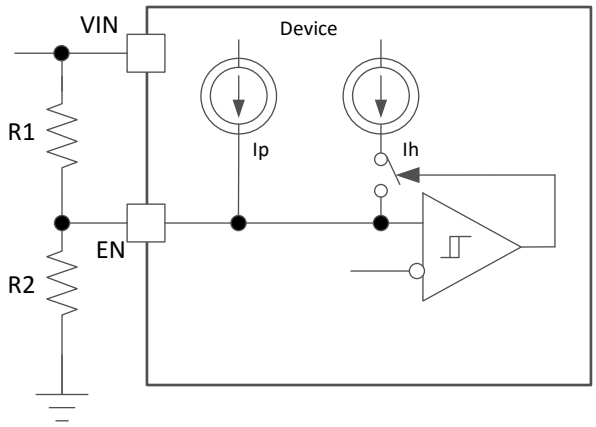


图 9-4. Adjustable V_{IN} Undervoltage Lockout

$$R_1 = \frac{V_{START} \times \frac{V_{EN\_FALL}}{V_{EN\_RISE}} - V_{STOP}}{I_p \times \left(1 - \frac{V_{EN\_FALL}}{V_{EN\_RISE}}\right) + I_h} \quad (3)$$

$$R_2 = \frac{R_1 \times V_{EN\_FALL}}{V_{STOP} - V_{EN\_FALL} + R_1 \times \left(I_p + I_h\right)} \quad (4)$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 \times R_2 \times \left(I_p + I_h\right)}{R_1 + R_2} \quad (5)$$

where

- I_p is 0.7 µA.
- I_h is 1.4 µA.
- V_{EN_FALL} is 1.17 V.
- V_{EN_RISE} is 1.21 V.
- V_{START} is the input voltage enabling the device.
- V_{STOP} is the input voltage disabling the device.

9.3.7 External Soft Start and Prebiased Soft Start

The SS pin of TPS62932, TPS62933, and TPS62933F are used to minimize inrush current when driving capacitive load. The devices use the lower voltage of the internal voltage reference, V_{REF}, or the SS pin voltage as the reference voltage and regulates the output accordingly. A capacitor on the SS pin to ground implements a soft-start time. The device has an internal pullup current source that charges the external soft-start capacitor. Use 方程式 6 to calculate the soft-start time (t_{SS}, 0% to 100%) and soft-start capacitor (C_{SS}).

$$t_{SS} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (6)$$

where

- V_{REF} is 0.8 V (the internal reference voltage).
- I_{SS} is 5.5 µA (typical), the internal pullup current.

If the output capacitor is prebiased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage, V_{FB}. This scheme makes sure that the converters ramp up smoothly into regulation point.

A resistor divider connected to the SS pin can implement voltage tracking of the other power rail.

9.3.8 Power Good

The TPS62933P and TPS62933O have a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage below 5.5 V. TI recommends a pullup resistor of 10 kΩ – 100 kΩ. The device can sink approximately 4 mA of current and maintain its specified logic low level. After the FB pin voltage is between 90% and 110% of the internal reference voltage (V_{REF}) and after a deglitch time of 70 µs, the PG turns to high impedance status. The PG pin is pulled low after a deglitch time of 18 µs when FB pin voltage is lower than 85% of the internal reference voltage or greater than 115% of the internal reference voltage, or in events of thermal shutdown, EN shutdown, or UVLO conditions. VIN must remain present for the PG pin to stay low.

表 9-2. PG Status

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN = High)	V_{FB} does not trigger V_{PGTH}	√	
	V_{FB} triggers V_{PGTH}		√
Shutdown (EN = Low)			√
UVLO	2.5 V < V_{IN} < V_{UVLO}		√
Thermal shutdown	T_J > T_{SD}		√
Power supply removal	V_{IN} < 2.5 V	√	

9.3.9 Minimum On Time, Minimum Off Time, and Frequency Foldback

Minimum on time (t_{ON_MIN}) is the smallest duration of time that the high-side switch can be on. t_{ON_MIN} is typically 70 ns in the TPS6293x. Minimum off time (t_{OFF_MIN}) is the smallest duration that the high-side switch can be off. t_{OFF_MIN} is typically 140 ns. In CCM operation, t_{ON_MIN}, and t_{OFF_MIN}, limit the voltage conversion range without switching frequency foldback.

The minimum duty cycle without frequency foldback allowed is:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \quad (7)$$

The maximum duty cycle without frequency foldback allowed is:

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \quad (8)$$

Given a required output voltage, the maximum V_{IN} without frequency foldback is:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \quad (9)$$

The minimum V_{IN} without frequency foldback is:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \quad (10)$$

In TPS6293x, a frequency foldback scheme is employed once t_{ON_MIN} or t_{OFF_MIN} is triggered, which can extend the maximum duty cycle or lower the minimum duty cycle.

The on time decreases while V_{IN} voltage increases. Once the on time decreases to t_{ON_MIN}, the switching frequency starts to decrease while V_{IN} continues to go up, which lowers the duty cycle further to keep V_{OUT} in regulation according to 方程式 7.

The frequency foldback scheme also works once larger duty cycle is needed under low V_{IN} condition. The frequency decreases once the device hits its t_{OFF_MIN}, which extends the maximum duty cycle according to 方程式 8. A wide range of frequency foldback allows the TPS6293x output voltage to stay in regulation with a much lower supply voltage V_{IN}, which allows a lower effective dropout.

With frequency foldback, V_{IN_MAX} is raised, and V_{IN_MIN} is lowered by decreased f_{SW}.

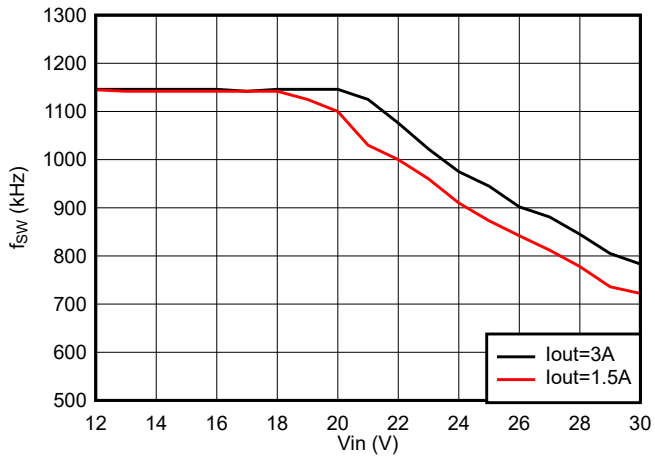


图 9-5. Frequency Foldback at t_{ON_MIN}, V_{OUT} = 1.8 V, f_{SW} = 1200 kHz

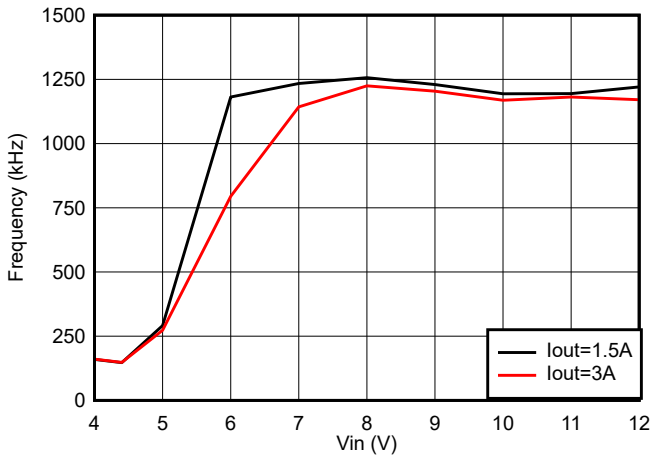


图 9-6. Frequency Foldback at t_{OFF_MIN}, V_{OUT} = 5 V, f_{SW} = 1200 kHz

9.3.10 Frequency Spread Spectrum

To reduce EMI, the TPS62932, TPS62933, TPS62933P, and TPS62933O introduce frequency spread spectrum. The jittering span is typically Δfc = ±6% of the switching frequency with the modulation frequency of $f_m = f_{SW} / 128$. The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a part with fixed frequency operation. 图 9-7 shows the frequency spread spectrum modulation. 图 9-8 shows the energy is spread out at the center frequency, f_c.

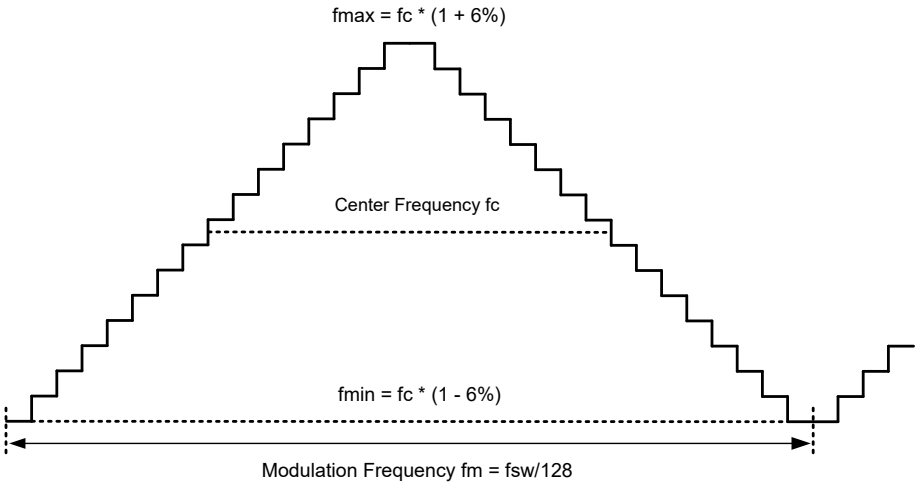


图 9-7. Frequency Spread Spectrum Diagram

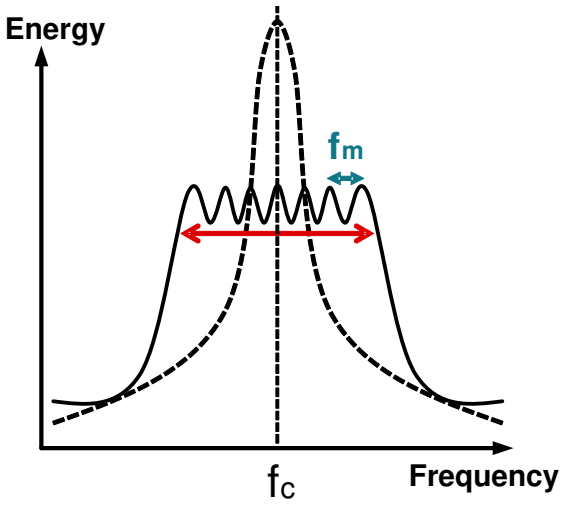


图 9-8. Energy vs Frequency

9.3.11 Overvoltage Protection

The device incorporates an output overvoltage protection (OVP) circuit to minimize output voltage overshoot. The OVP feature minimizes the overshoot by comparing the FB pin voltage to the OVP threshold. If the FB pin voltage is greater than the OVP threshold of 115%, the high-side MOSFET is turned off, which prevents current from flowing to the output and minimizes output overshoot. When the FB pin voltage drops lower than the OVP threshold minus hysteresis, the high-side MOSFET is allowed to turn on at the next clock cycle. This function is non-latch operation.

9.3.12 Overcurrent and Undervoltage Protection

The TPS6293x incorporates both peak and valley inductor current limits to provide protection to the device from overloads and short circuits and limit the maximum output current. Valley current limit prevents inductor current run-away during short circuits on the output, while both peak and valley limits work together to limit the maximum output current of the converter. Hiccup mode is also incorporated for sustained short circuits.

The high-side switch current is sensed when it is turned on after a set blanking time (t_{ON_MIN}), the peak current of high-side switch is limited by the peak current threshold, I_{HS_LIMIT}. The current going through low-side switch is also sensed and monitored. When the low-side switch turns on, the inductor current begins to ramp down.

As the device is overloaded, a point is reached where the valley of the inductor current cannot reach below I_{LS_LIMIT} before the next clock cycle, then the low-side switch is kept on until the inductor current ramps below

the valley current threshold, I_{LS_LIMIT}, then the low-side switch is turned off and the high-side switch is turned on after a dead time. When this occurs, the valley current limit control skips that cycle, causing the switching frequency to drop. Further overload causes the switching frequency to continue to drop, but the output voltage remains in regulation. As the overload is increased, both the inductor current ripple and peak current increase until the high-side current limit, I_{HS_LIMIT}, is reached. When this limit is tripped, the switch duty cycle is reduced and the output voltage falls out of regulation. This represents the maximum output current from the converter and is given approximately by 方程式 11. The output voltage and switching frequency continue to drop as the device moves deeper into overload while the output current remains at approximately I_{OMAX}. There is another situation, if the inductor ripple current is large, the high-side current limit can be tripped before the low-side limit is reached. In this case, 方程式 12 gives the approximate maximum output current.

$$I_{OMAX} \approx \frac{I_{HS\_LIMIT} + I_{LS\_LIMIT}}{2} \tag{11}$$

$$I_{OMAX} \approx I_{HS\_LIMIT} - \frac{(V_{IN} - V_{OUT})}{2 \times L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \tag{12}$$

Furthermore, if a severe overload or short circuit causes the FB voltage to fall below the V_{UVP} threshold, 65% of the V_{REF}, and triggering current limit, and the condition occurs for more than the hiccup on time (typical 256 μs), the converter enters hiccup mode. In this mode, the device stops switching for hiccup off time, 10.5 × t_{SS}, and then goes to a normal restart with soft-start time. If the overload or short-circuit condition remains, the device runs in current limit and then shuts down again. This cycle repeats as long as the overload or short-circuit condition persists. This mode of operation reduces the temperature rise of the device during a sustained overload or short circuit condition on the output. Once the output short is removed, the output voltage recovers normally to the regulated value.

For FCCM version, the inductor current is allowed to go negative. When this current exceed the LS negative current limit I_{LS_NEG}, the LS switch is turned off and HS switch is turned on immediately, which is used to protect the LS switch from excessive negative current.

9.3.13 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 165°C (typical), the device goes into thermal shutdown, both the high-side and low-side power FETs are turned off. When T_J decreases below the hysteresis amount of 30°C (typical), the converter resumes normal operation, beginning with a soft start.

9.4 Device Functional Modes

9.4.1 Modes Overview

The TPS6293x moves between CCM, DCM, PFM, OOA and FCCM mode as the load changes. Depending on the load current, the TPS6293x is in one of below modes:

- Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple
- Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation
- Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load
- Out of audio (OOA) mode when switching frequency is decreased but is always above 30 kHz at very light load
- Forced continuous conduction mode (FCCM) with fixed switching frequency even at light load

9.4.2 Heavy Load Operation

The TPS6293x operates in continuous conduction mode (CCM) when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. Regulating the output voltage provides excellent line and load regulation and minimum output voltage ripple, and the maximum continuous output current of 2 A or 3 A can be supplied by the TPS6293x.

9.4.3 Light Load Operation

The TPS62932, TPS62933, and TPS62933P are designed to operate in pulse frequency modulation (PFM) mode at light load currents to boost light load efficiency.

When the load current is lower than half of the peak-to-peak inductor current in CCM, the device operates in discontinuous conduction mode (DCM), also known as diode emulation mode (DEM). In DCM operation, the LS switch is turned off when the inductor current drops to I_{LS_ZC} to improve efficiency. Both switching losses and conduction losses are reduced in DCM, compared to forced CCM operation at light load.

At even lighter current load, pulse frequency modulation (PFM) mode is activated to maintain high efficiency operation. When either the minimum on time, t_{ON_MIN}, or the minimum peak inductor current, I_{PEAK_MIN} (750 mA typical), is reached, the switching frequency decreases to maintain regulation. In PFM mode, switching frequency is decreased by the control loop to maintain output voltage regulation when load current reduces. Switching loss is further reduced in PFM operation due to less frequent switching actions. The output current for mode change depends on the input voltage, inductor value, and the programmed switching frequency. For applications where the switching frequency must be known for a given condition, the transition between PFM and CCM must be carefully tested before the design is finalized.

9.4.4 Out of Audio Operation

TPS62933O implements the out of audio (OOA) mode which is a unique control feature that keeps the switching frequency above audible frequency (20 Hz to 20 kHz) even at no load condition. When operates in OOA mode, the minimum switching frequency is clamped above 30 kHz which avoids the audible noise in the system. The loading to enter OOA mode depends on output LC filter.

9.4.5 Forced Continuous Conduction Operation

The TPS62933F is designed to operate in forced continuous conduction mode (FCCM) under light load conditions. During FCCM, the switching frequency is maintained at a constant level over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. For some audio applications, this mode can help avoid switching frequency drop into audible range that can introduce some noise.

9.4.6 Dropout Operation

The dropout performance of any buck converter is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage level approaches the output voltage, the off time of the high-side MOSFET starts to approach the minimum value. Beyond this point, the switching frequency becomes erratic and the output voltage can fall out of regulation. To avoid this problem, the TPS6293x automatically reduces the switching frequency (on-time extension function) to increase the effective duty cycle and maintain in regulation until the switching frequency reach to the lowest limit of about 140 kHz, the period is equal to t_{ON_MAX} + t_{OFF_MIN} (7.14 μS typical). In this condition, the difference voltage between V_{IN} and V_{OUT} is defined as dropout voltage. The typical overall dropout characteristics can be found as 图 9-9.

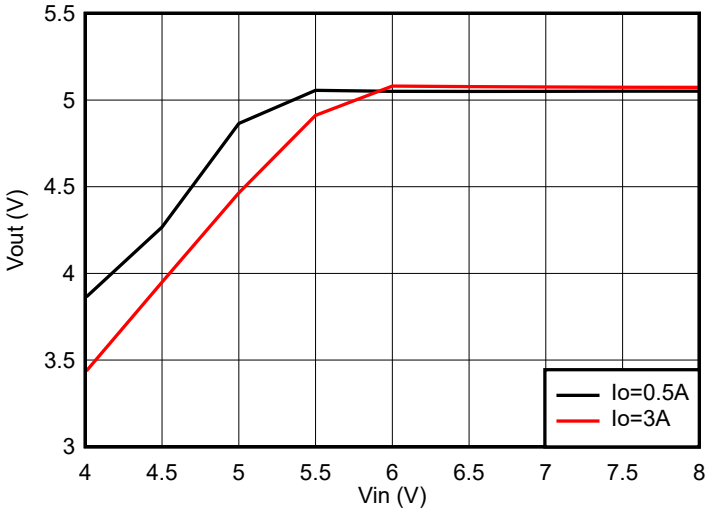


图 9-9. Overall Dropout Characteristic, V_{OUT} = 5 V

9.4.7 Minimum On-Time Operation

Every switching converter has a minimum controllable on time dictated by the inherent delays and blanking times associated with the control circuits, which imposes a minimum switch duty cycle and, therefore, a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the TPS6293x automatically reduces the switching frequency when the minimum on-time limit is reached. This way, the converter can regulate the lowest programmable output voltage at the maximum input voltage. Use 方程式 13 to find an estimate for the approximate input voltage for a given output voltage before frequency foldback occurs. The values of t_{ON_MIN} and f_{SW} can be found in 节 8.5.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON\_MIN} \times f_{SW}} \tag{13}$$

As the input voltage is increased, the switch on time (duty-cycle) reduces to regulate the output voltage. When the on time reaches the minimum on time, t_{ON_MIN}, the switching frequency drops while the on time remains fixed.

9.4.8 Shutdown Mode

The EN pin provides electrical ON and OFF control for the device. When V_{EN} is below typical 1.1 V, the TPS6293x is in shutdown mode. The device also employs VIN UVLO protection. If V_{IN} voltage is below their respective UVLO level, the converter is turned off too.

10 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

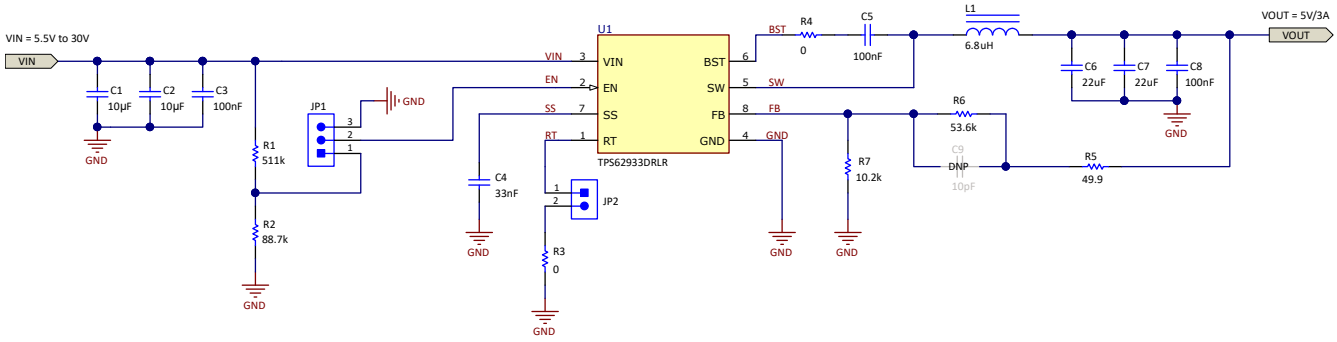
10.1 Application Information

The TPS62933 is a highly integrated, synchronous, step-down, DC-DC converter. This device is used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 3 A.

10.2 Typical Application

The application schematic of 图 10-1 was developed to meet the requirements of the device. This circuit is available as the TPS62933EVM evaluation module. The design procedure is given in this section.

图 10-1. TPS62933 5-V Output, 3-A Reference Design



10.2.1 Design Requirements

表 10-1 shows the design parameters for this application.

表 10-1. Design Parameters

Parameter		Conditions	MIN	TYP	MAX	Unit
V_{IN}	Input voltage		5.5	24	30	V
V_{OUT}	Output voltage			5		V
I_{OUT}	Output current rating			3		A
ΔV_{OUT}	Transient response	Load step from 0.5 A→2.5 A→0.5 A, 0.8-A/µS slew rate		±5% × V_{OUT}		V
$V_{IN(ripple)}$	Input ripple voltage			400		mV
$V_{OUT(ripple)}$	Output ripple voltage			30		mV
F_{SW}	Switching frequency	RT = floating		500		kHz
t_{SS}	Soft-start time	C_{SS} = 33 nF		5		mS
V_{START}	Start input voltage (Rising V_{IN})			8		V
V_{STOP}	Stop input voltage (Falling V_{IN})			7		V
T_A	Ambient temperature			25		°C

10.2.2 Detailed Design Procedure

10.2.2.1 Custom Design With WEBENCH® Tools

Create a custom design with the TPS6293x using the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Referring to the application schematic of 图 10-1, start with 10.2 kΩ for R7 and use 方程式 14 to calculate R6 = 53.6 kΩ. To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the converter is more susceptible to noise and voltage errors from the FB input leakage current are noticeable.

$$R_6 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_7 \tag{14}$$

表 10-2 shows the recommended components value for common output voltages.

10.2.2.3 Choosing Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Higher switching frequency allows the use of smaller inductors and output capacitors, and hence, a more compact design. However, lower switching frequency implies reduced switching losses and usually results in higher system efficiency, so the 500-kHz switching frequency was chosen for this example, remove the jumper on JP2 and leave RT pin floating.

Please note the switching frequency is also limited by the following as mentioned in 节 9.3.9:

- Minimum on time of the integrated power switch
- Input voltage
- Output voltage
- Frequency shift limitation

10.2.2.4 Soft-Start Capacitor Selection

The large C_{SS} can reduce inrush current when driving large capacitive load. 33 nF is chosen for C4, which sets the soft-start time, t_{SS}, to approximately 5 ms.

In addition, the SS pin cannot be floated, so a minimum 6.8-nF capacitor must be connected at this pin.

10.2.2.5 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BST to SW pins for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor C5 must have a 16-V or higher voltage rating.

In addition, adding one BST resistor R4 to reduce the spike voltage on the SW node, TI recommends the resistance smaller than 10 Ω be used between BST to the bootstrap capacitor.

10.2.2.6 Undervoltage Lockout Setpoint

The undervoltage lockout (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between VIN and the EN pin and R2 is connected between EN and GND. The UVLO has two thresholds: one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply turns on and starts switching when the input voltage increases above 8 V (V_{START}). After the converter starts switching, it continues to do so until the input voltage falls below 7 V (V_{STOP}). 方程式 3 and 方程式 4 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified, the nearest standard resistor value for R1 is 511 kΩ and for R2 is 80.7 kΩ.

10.2.2.7 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current, Δi_L, which can be calculated by 方程式 15.

$$\Delta I_L = \frac{V_{OUT}}{V_{IN\_MAX}} \times \frac{V_{IN\_MAX} - V_{OUT}}{L \times f_{SW}} \tag{15}$$

Usually, define K coefficient represents the amount of inductor ripple current relative to the maximum output current of the device, a reasonable value of K is 20% to 60%. Experience shows that the best value of K is 40%. Since the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L. Use 方程式 16 to calculate the minimum value of the output inductor.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \times K \times I_{OUT\_MAX}} \times \frac{V_{OUT}}{V_{IN}} \tag{16}$$

where

- K is the ripple ratio of the inductor current (ΔI_L / I_{OUT_MAX}).

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. Too low of an inductance can generate too large of an inductor current ripple such that overcurrent protection at the full load can be falsely triggered. The device also generates more inductor core loss since the current ripple is larger. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors.

After inductance L is determined, the maximum inductor peak current and RMS current can be calculated by 方程式 17 and 方程式 18.

$$I_{L\_PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \tag{17}$$

$$I_{L\_RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}} \tag{18}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{HS_LIMIT} (see 节 8.5). This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LS_LIMIT}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly, this can lead to component damage, so do not allow the inductor to saturate. In any case, the inductor saturation current must not be less than the maximum peak inductor current at full load.

For this design example, choose the following values:

- K = 0.4
- V_{IN_MAX} = 30 V
- f_{SW} = 500 kHz
- I_{OUT_MAX} = 3 A

The inductor value is calculated to be 6.94 μH. Choose the nearest standard value of 6.8 μH, which gives a new K value of 0.408. The maximum I_{HS_LIMIT} is 5.8 A, the calculated peak current is 3.61 A, and the calculated RMS current is 3.02 A. The chosen inductor is a Würth Elektronik, 74439346068, 6.8 μH, which has a saturation current rating of 10 A and a RMS current rating of 6.5 A.

The maximum inductance is limited by the minimum current ripple required for the peak current mode control to perform correctly. To avoid subharmonic oscillation, as a rule-of-thumb, the minimum inductor ripple current must be no less than approximately 10% of the device maximum rated current (3 A) under nominal conditions.

10.2.2.8 Output Capacitor Selection

The device is designed to be used with a wide variety of LC filters, so it is generally desired to use as little output capacitance as possible to keep cost and size down. Choose the output capacitance, C_{OUT}, with care since it directly affects the following specifications:

- Steady state output voltage ripple
- Loop stability
- Output voltage overshoot and undershoot during load current transient

The output voltage ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR = K \times I_{OUT} \times ESR \tag{19}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}} = \frac{K \times I_{OUT}}{8 \times f_{SW} \times C_{OUT}} \tag{20}$$

where

- K is the ripple ratio of the inductor current (ΔI_L / I_{OUT_MAX}).

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks.

Output capacitance is usually limited by the load transient requirements rather than the output voltage ripple if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a large load step happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the converter usually needs eight or more clock cycles to regulate the inductor current equal to the new load level. The output capacitance must be large enough to supply the current difference for about eight clock cycles to maintain the output voltage within the specified range. 方程式 21 shows the minimum output capacitance needed for specified V_{OUT} overshoot and undershoot.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT} \times K} \times \left[(1-D) \times (1+K) + \frac{K^2}{12} (2-D) \right] \tag{21}$$

where

- D is V_{OUT} / V_{IN}, duty cycle of steady state.
- ΔV_{OUT} is the output voltage change.

- ΔI_{OUT} is the output current change.

For this design example, the target output ripple is 30 mV. Presuppose $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 30 mV and choose K = 0.4. 方程式 19 yields ESR no larger than 25 mΩ and 方程式 20 yields C_{OUT} no smaller than 10 µF. For the target overshoot and undershoot limitation of this design, $\Delta V_{OUT\_SHOOT} < 5\% \times V_{OUT}$ = 250 mV for an output current step of ΔI_{OUT} = 1.5 A. C_{OUT} is calculated to be no smaller than 25 µF by 方程式 21. In summary, the most stringent criterion for the output capacitor is 25 µF. Considering the ceramic capacitor has DC bias de-rating, it can be achieved with a bank of 2 × 22-µF, 35-V, ceramic capacitor C3216X5R1V226M160AC in the 1206 case size.

More output capacitors can be used to improve the load transient response. Ceramic capacitors can easily meet the minimum ESR requirements. In some cases, an aluminum electrolytic capacitor can be placed in parallel with the ceramics to build up the required value of capacitance. When using a mixture of aluminum and ceramic capacitors, use the minimum recommended value of ceramics and add aluminum electrolytic capacitors as needed.

The recommendations given in 表 10-2 provide typical and minimum values of output capacitance for the given conditions. These values are the effective figures. If the minimum values are to be used, the design must be tested over all of the expected application conditions, including input voltage, output current, and ambient temperature. This testing must include both bode plot and load transient assessments. The maximum value of total output capacitance can be referred to C_{OUT} selection and C_{FF} selection in the *TPS62933 Thermal Performance with SOT583 Package Application Report*. Large values of output capacitance can adversely affect the start-up behavior of the converter as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

In practice, the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can help reduce spikes on the output caused by inductor and board parasitics.

表 10-2 shows the recommended LC combination.

表 10-2. Recommended LC Combination for TPS62933

V_{OUT}(V)	f_{SW} (kHz)	R_{TOP}(kΩ)	R_{DOWN}(kΩ)	Typical Inductor L (µH)	Typical Effective C_{OUT} (µF)	Minimum Effective C_{OUT} (µF)
3.3	500	31.3	10.0	4.7	40	15
	1200			2.2	30	10
5	500	52.5	10.0	6.8	20	10
	1200			3.3	20	10
12	500	140.0	10.0	12	15	10

10.2.2.9 Input Capacitor Selection

The TPS6293x device requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The typical recommended value for the decoupling capacitor is 10 µF, and an additional 0.1-µF capacitor from the VIN pin to ground is recommended to provide high frequency filtering.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. X5R and X7R ceramic dielectrics are recommended because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The capacitor must also be selected with the DC bias taken into account. The effective capacitance value decreases as the DC bias increases.

The capacitor voltage rating needs to be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple. The input ripple current can be calculated using 方程式 22.

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{V_{IN\_MIN} - V_{OUT}}{V_{IN\_MIN}}} \quad (22)$$

For this example design, two TDK CGA5L1X7R1H106K160AC (10-μF, 50-V, 1206, X7R) capacitors have been selected. The effective capacitance under input voltage of 24 V for each one is 3.45 μF. The input capacitance value determines the input ripple voltage of the converter. The input voltage ripple can be calculated using 方程式 23. Using the design example values, I_{OUT_MAX} = 3 A, C_{IN_EFF} = 2 × 3.45 = 6.9 μF, and f_{SW} = 500 kHz, yields an input voltage ripple of 222 mV and a RMS input ripple current of 1.22 A.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX} \times 0.25}{C_{IN} \times f_{SW}} + (I_{OUT\_MAX} \times R_{ESR\_MAX}) \quad (23)$$

where

- R_{ESR_MAX} is the maximum series resistance of the input capacitor, which is approximately 1.5 mΩ of two capacitors in paralleled.

10.2.2.10 Feedforward Capacitor C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT} in combination with the parasitic capacitance at the FB pin can create a small signal pole that interferes with the loop stability. A C_{FF} helps mitigate this effect. Use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor.

The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor Application Report* is helpful when experimenting with a feedforward capacitor.

For this example design, a 10-pF capacitor C9 can be mounted to boost load transient performance.

10.2.2.11 Maximum Ambient Temperature

As with any power conversion device, the TPS6293x dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, $R_{\theta JA}$, of the device
- PCB combination

The maximum internal die temperature must be limited to 150°C. This establishes a limit on the maximum device power dissipation and, therefore, the load current. 方程式 24 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. Note that these curves include the power loss in the inductor. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics Application Report*, the value of $R_{\theta JA}$ given in the *Thermal Information* table is not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application. The data given for $R_{\theta JC(bott)}$ and Ψ_{JT} can be useful when determining thermal performance. See the *Semiconductor and IC Package Thermal Metrics Application Report* for more information and the resources given at the end of this section.

$$I_{OUT\_MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{1-\eta} \times \frac{1}{V_{OUT}} \quad (24)$$

where

- η is efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature and flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

10.2.3 Application Curves

V_{IN} = 24 V, V_{OUT} = 5 V, L_1= 6.8 µH, C_{OUT} = 44 µF, T_A = 25°C (unless otherwise noted)

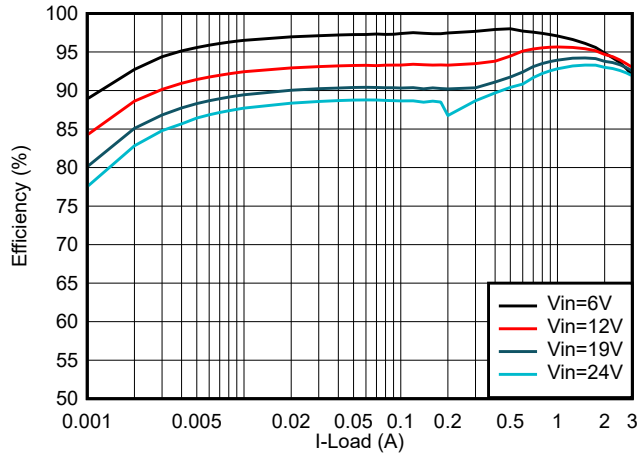


图 10-2. Efficiency

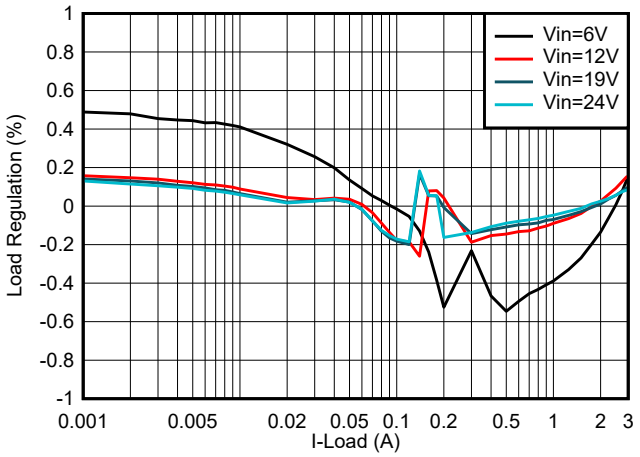


图 10-3. Load Regulation

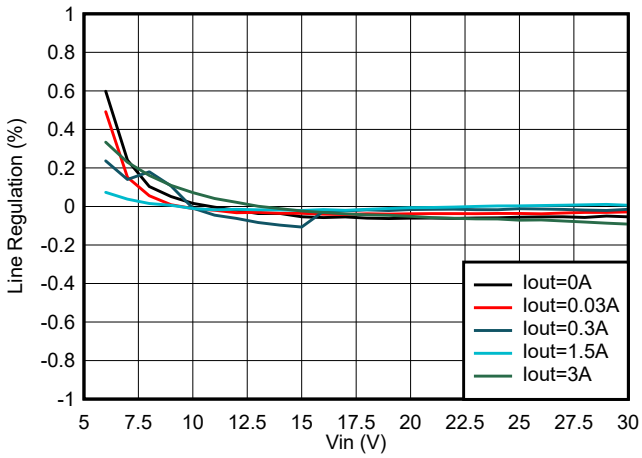


图 10-4. Line Regulation

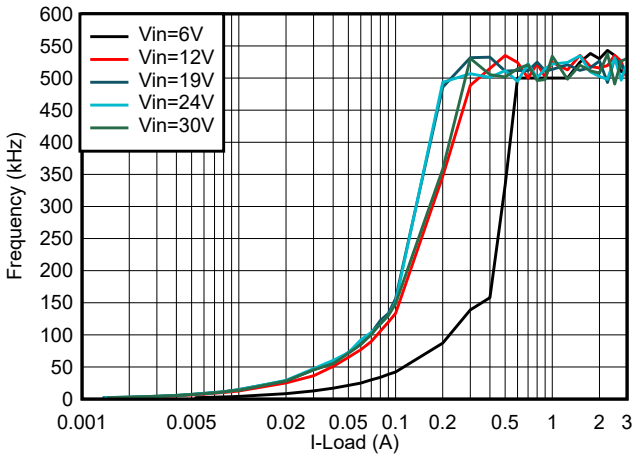


图 10-5. Switching Frequency vs Load Current

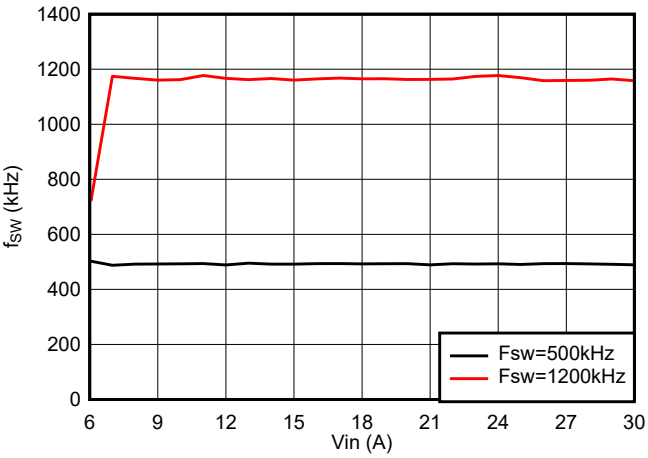


图 10-6. Switching Frequency vs V_{IN}, V_{OUT} = 5 V

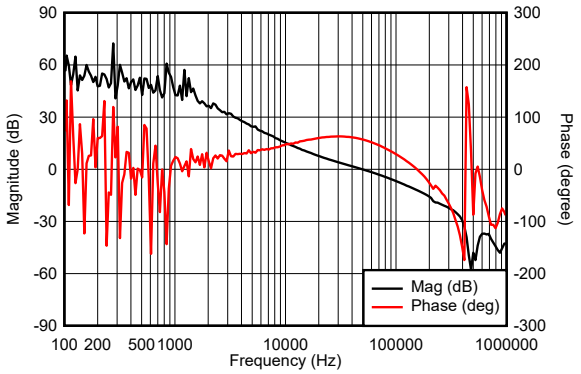


图 10-7. Loop Frequency Response, I_{OUT} = 3 A, BW = 49.4 kHz, PM = 57°, GM = – 12 dB

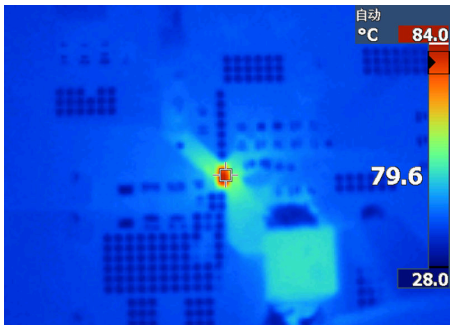


图 10-8. Case Temperature, V_{IN} = 24 V, I_{OUT} = 3 A, f_{SW} = 500 kHz

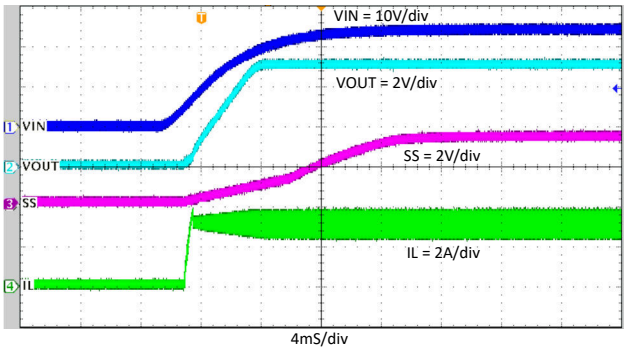


图 10-9. Start-Up Relative to V_{IN}, I_{OUT} = 3 A

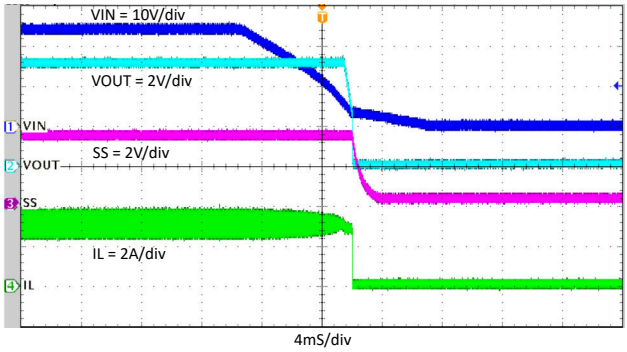


图 10-10. Shutdown Relative to V_{IN}, I_{OUT} = 3 A

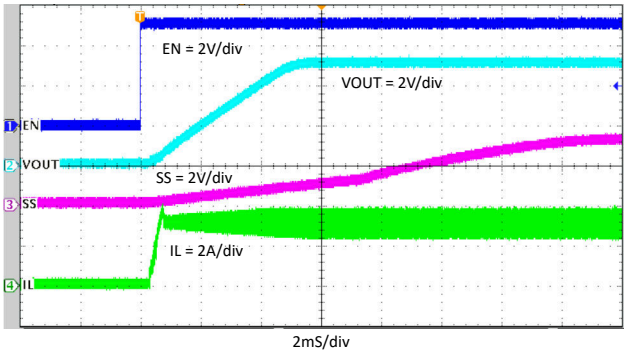


图 10-11. Start-Up Through EN, I_{OUT} = 3 A

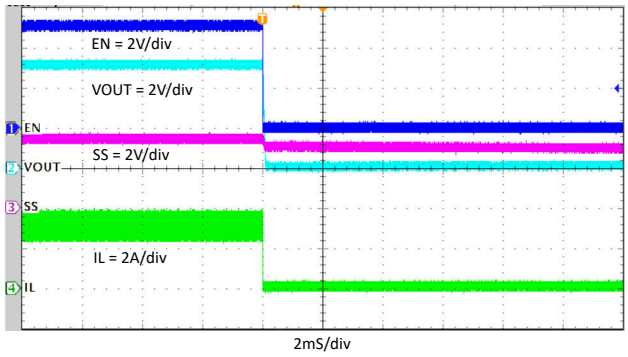


图 10-12. Shutdown Through EN, I_{OUT} = 3 A

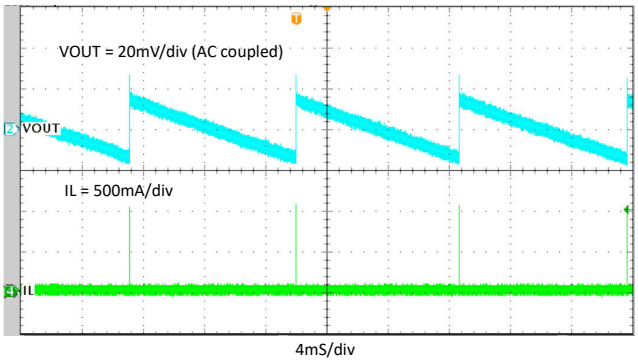


图 10-13. Steady State, I_{OUT} = 0 A

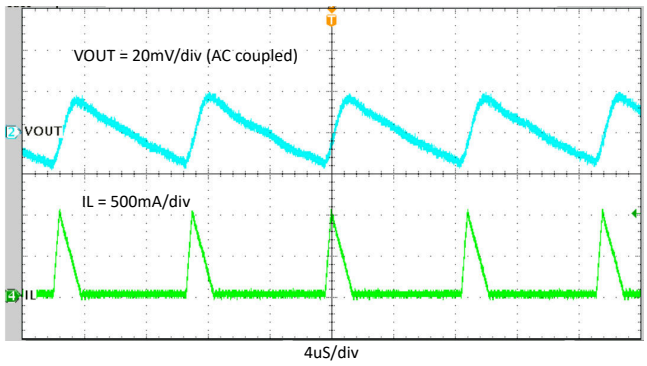


图 10-14. Steady State, I_{OUT} = 0.1 A

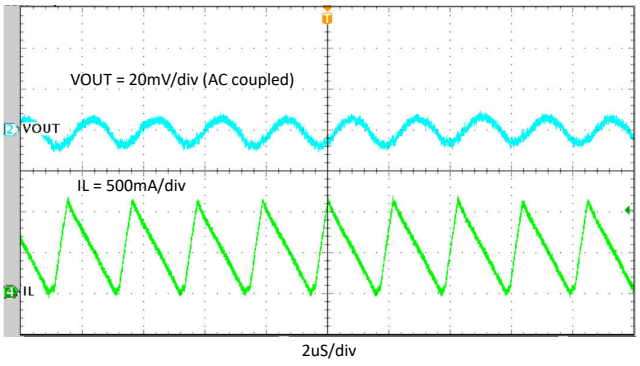


图 10-15. Steady State, I_{OUT} = 0.5 A

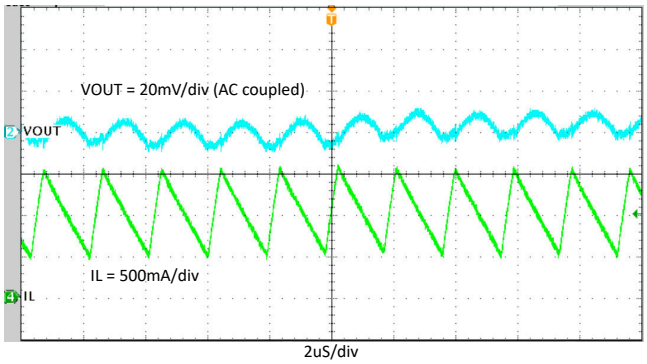


图 10-16. Steady State, I_{OUT} = 1 A

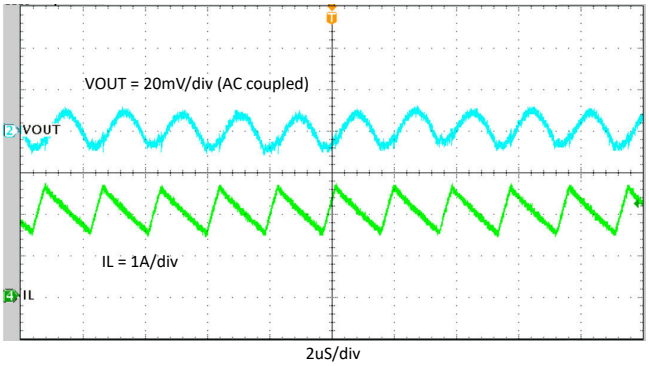


图 10-17. Steady State, I_{OUT} = 2 A

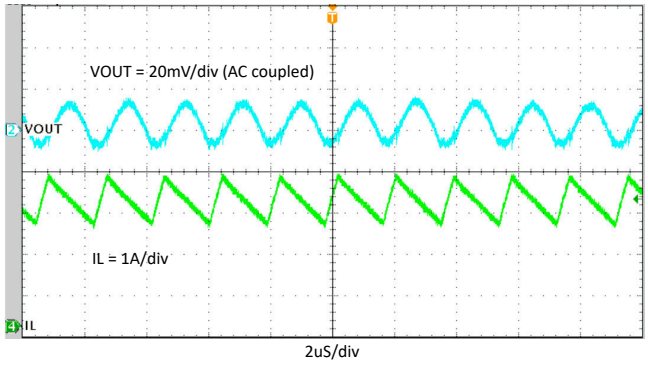


图 10-18. Steady State, I_{OUT} = 3 A

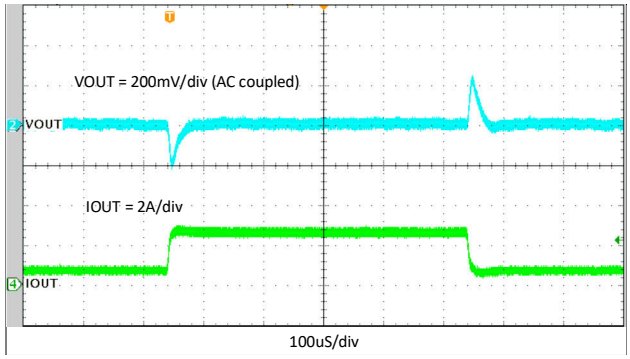


图 10-19. Load Transient Response, 0.5 to 2.5 A, Slew Rate = 0.8 A/ µ S

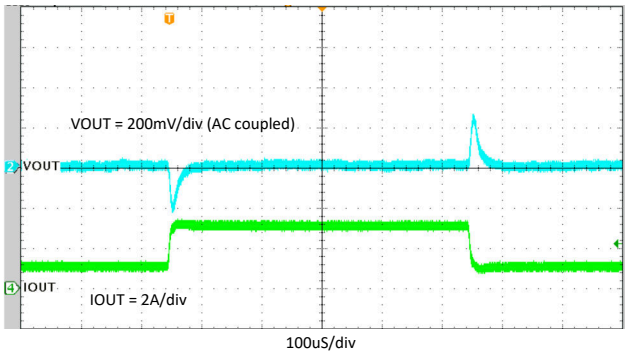


图 10-20. Load Transient Response, 1 to 3 A, Slew Rate = 0.8 A/ µ S

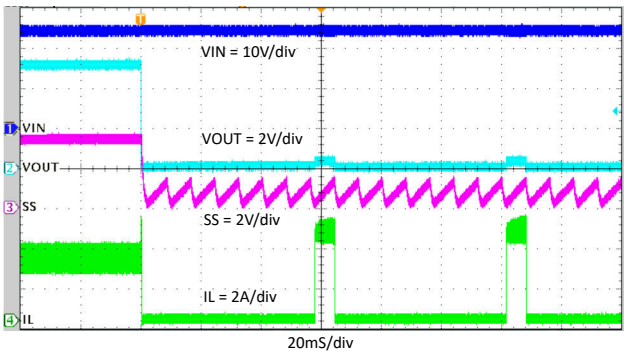


图 10-21. V_{OUT} Hard Short Protection

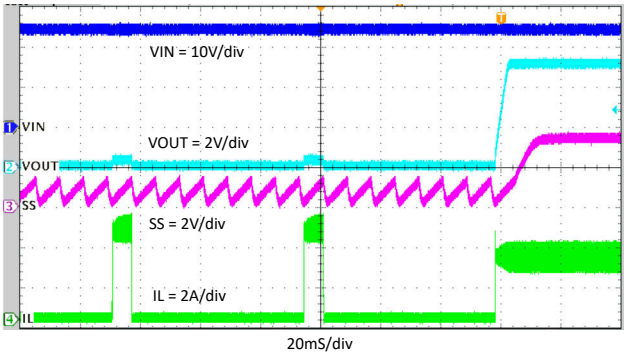


图 10-22. V_{OUT} Hard Short Recovery

10.3 What to Do and What Not to Do

- Do not exceed the *Absolute Maximum Ratings.*
- Do not exceed the *Recommended Operating Conditions.*
- Do not exceed the *ESD Ratings.*
- Do not allow the SS pin floating.
- Do not allow the output voltage to exceed the input voltage, nor go below ground.
- Do not use the value of $R_{\theta JA}$ given in the *Thermal Information* table to design your application. See 节 10.2.2.11.
- Follow all the guidelines and suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success.
- Use a 100-nF capacitor connected directly to the VIN and GND pins of the device. See 节 10.2.2.9 for details.

11 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 3.8 V and 30 V. This input supply must be well regulated and compatible with the limits found in the specifications of this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded converter. The average input current can be estimated with 方程式 25.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{25}$$

where

- η is efficiency.

If the converter is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the converter. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an under-damped resonant circuit, resulting in overvoltage transients at the input to the converter. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip can cause the converter to momentarily shutdown and reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the converter and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

TI recommends that the input supply must not be allowed to fall below the output voltage by more than 0.3 V. Under such conditions, the output capacitors discharges through the body diode of the high-side power MOSFET. The resulting current can cause unpredictable behavior, and in extreme cases, possible device damage. If the application allows for this possibility, then use a Schottky diode from VIN to VOUT to provide a path around the converter for this current.

In some cases, a transient voltage suppressor (TVS) is used on the input of converters. One class of this device has a snap-back characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the converter, the output capacitors discharges through the device, as mentioned above.

Sometimes, for other system considerations, an input filter is used in front of the converter, which can lead to instability as well as some of the effects mentioned above, unless it is designed carefully. The *AN-2162 Simple Success with Conducted EMI from DCDC Converters User's Guide* provides helpful suggestions when designing an input filter for any switching converter.

12 Layout

12.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of a good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, the EMI performance of the converter is dependent on the PCB layout to a great extent. In a buck converter, the most critical PCB feature is the loop formed by the input capacitors and power ground, as shown in 图 12-1. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance.

TI recommends a 2-layer board with 2-oz copper thickness of top and bottom layer, and proper layout provides low current conduction impedance, proper shielding, and lower thermal resistance. 图 12-2 and 图 12-3 show the recommended layouts for the critical components of the TPS62933.

- Place the inductor, input and output capacitors, and the IC on the same layer.
- Place the input and output capacitors as close as possible to the IC. The VIN and GND traces must be as wide as possible and provide sufficient vias on them to minimize trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- Place a 0.1-µF ceramic decoupling capacitor or capacitors as close as possible to VIN and GND pins, which is key to EMI reduction.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Place a BST capacitor and resistor close to the BST pin and SW node. A > 10-mil width trace is recommended to reduce the parasitic inductance.
- Place the feedback divider as close as possible to the FB pin. A > 10-mil width trace is recommended for heat dissipation. Connect a separate V_{OUT} trace to the upper feedback resistor. Place the voltage feedback loop away from the high-voltage switching trace. The voltage feedback loop preferably has ground shield.
- Place the SS capacitor and RT resistor close to the IC and routed with minimal lengths of trace. A > 10-mil width trace is recommended for heat dissipation.

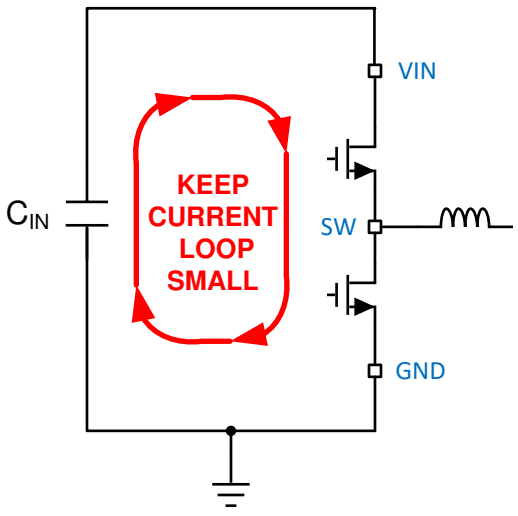


图 12-1. Current Loop With Fast Edges

12.2 Layout Example

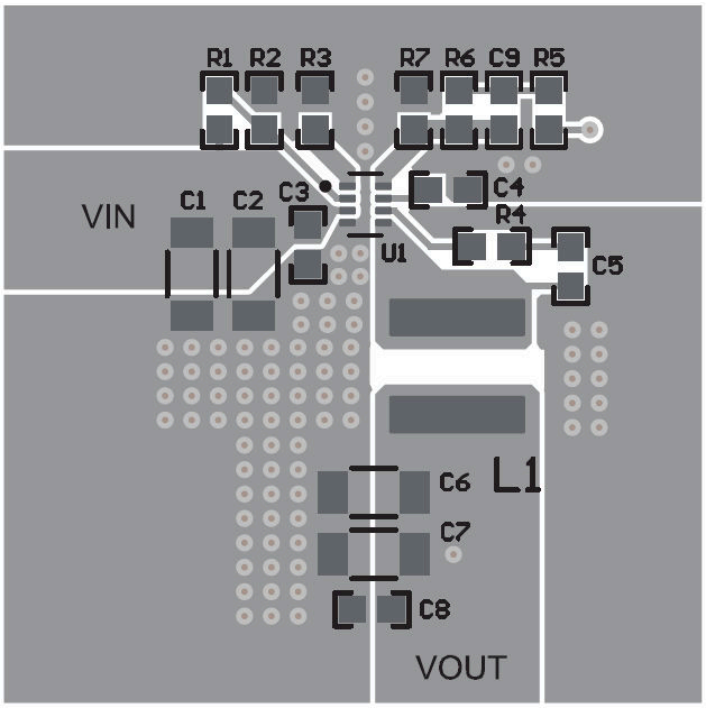


图 12-2. TPS62933 Top Layout Example

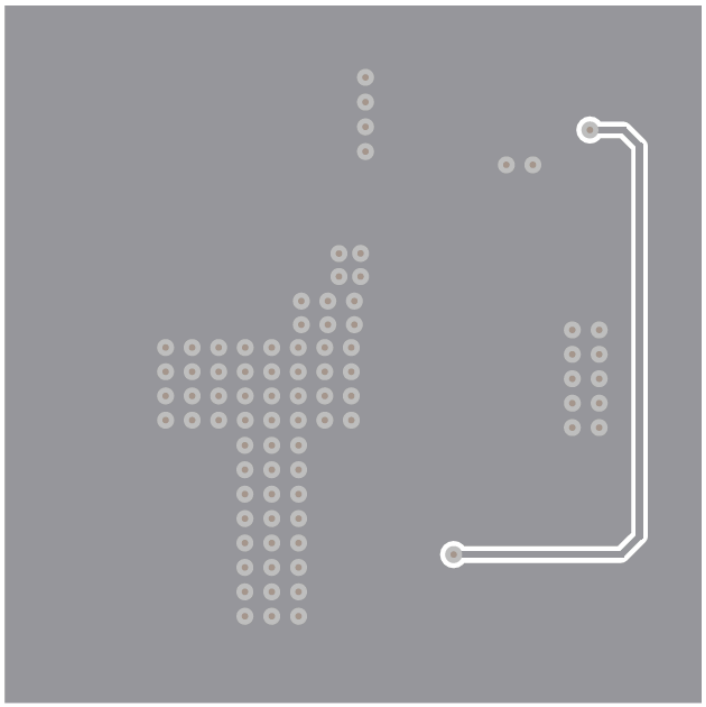


图 12-3. TPS62933 Bottom Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

13.1.2 Development Support

13.1.2.1 Custom Design With WEBENCH® Tools

Create a custom design with the TPS6293x using the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

13.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

13.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

13.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62932DRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 150	2932	Samples
TPS62933DRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 150	2933	Samples
TPS62933FDRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 150	933F	Samples
TPS62933ODRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 150	933O	Samples
TPS62933PDRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 150	933P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

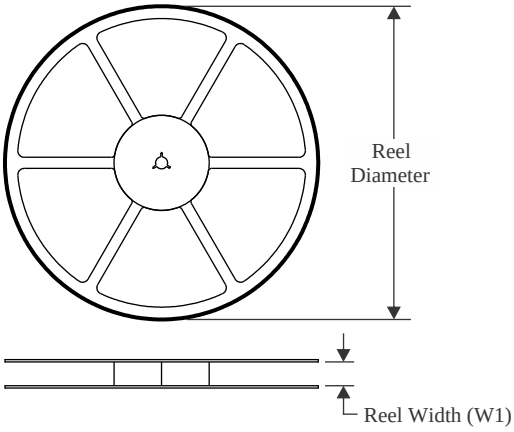
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

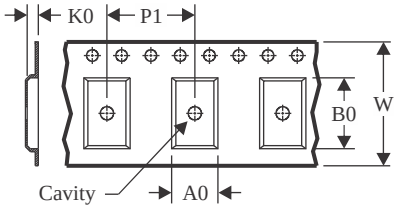
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

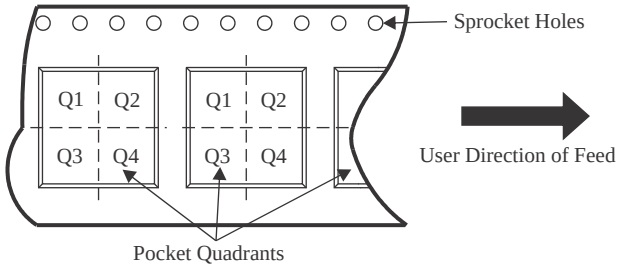


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

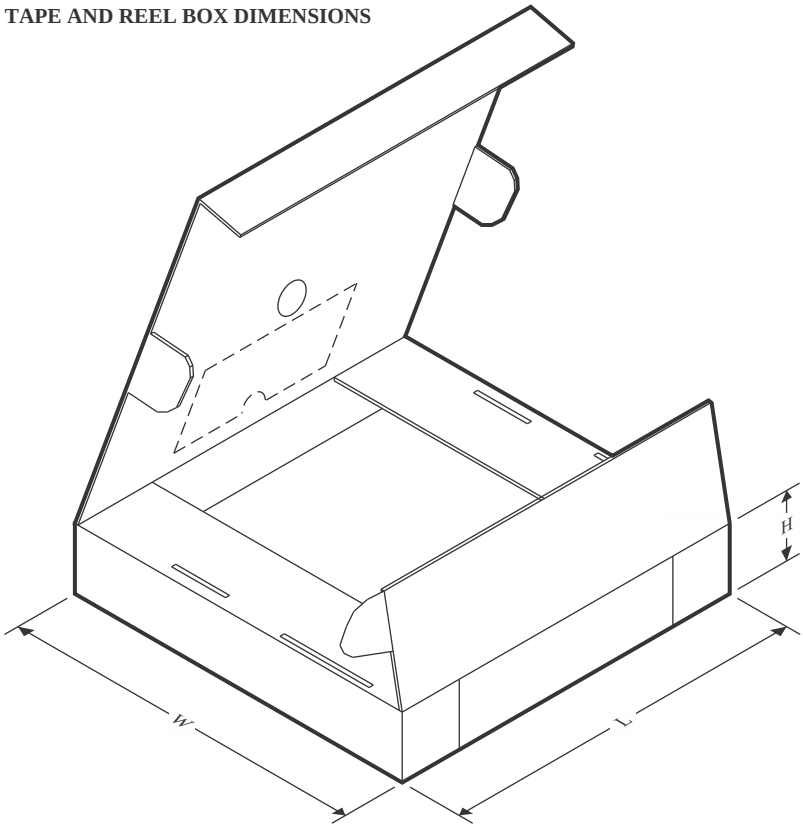
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62932DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS62933DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS62933FDRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS62933ODRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3
TPS62933PDRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

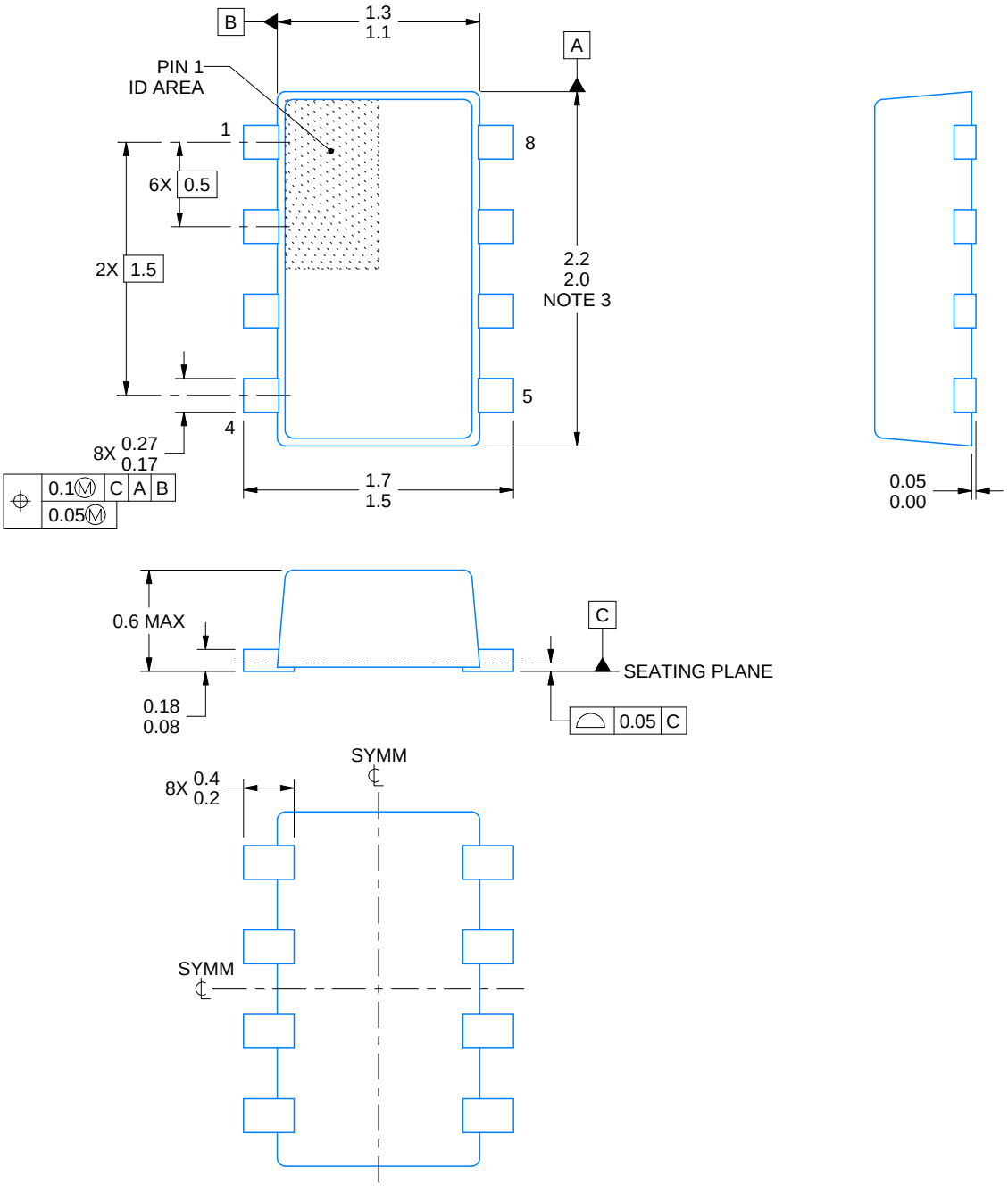
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62932DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS62933DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS62933FDRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS62933ODRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0
TPS62933PDRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



4224486/E 12/2021

NOTES:

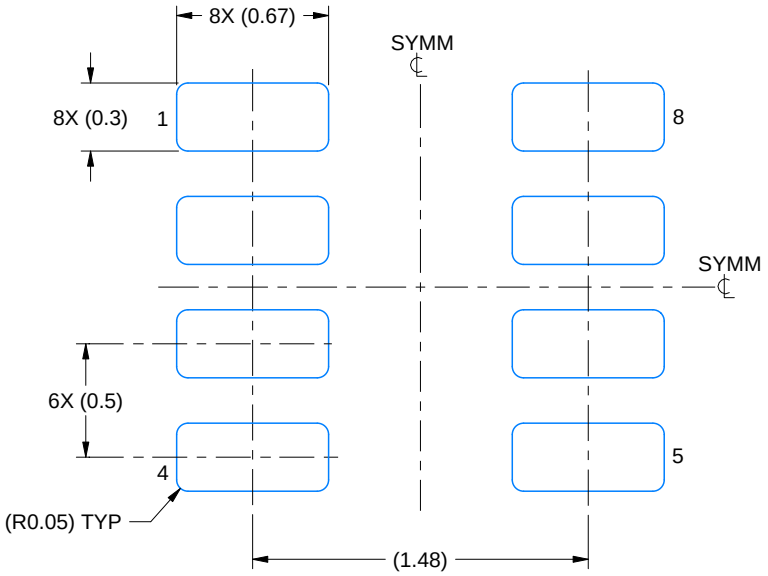
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

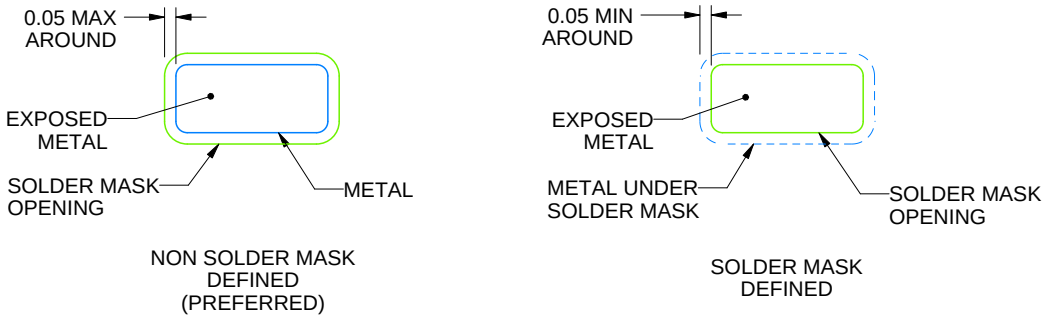
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

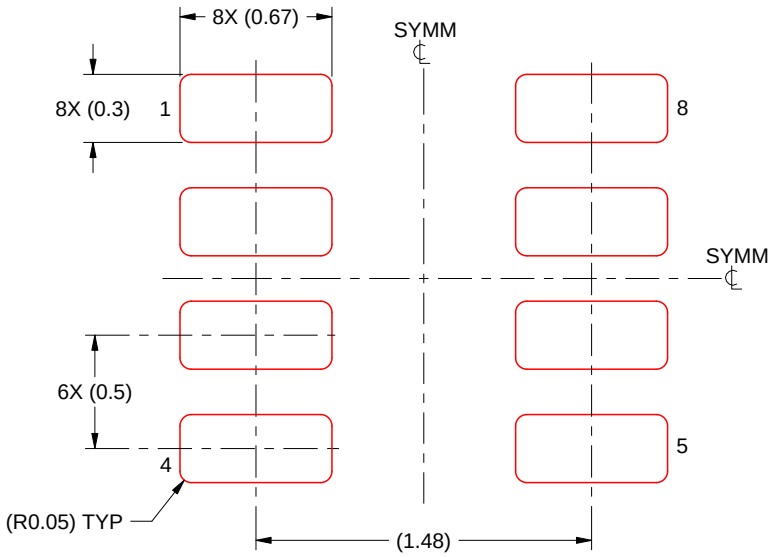


SOLDERMASK DETAILS

4224486/E 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4224486/E 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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