TEXAS INSTRUMENTS
TPSI3052-Q1
ZHCSMH9 – APRIL 2022

TPSI3052-Q1 具有集成 15-V 栅极电源的汽车类增强型隔离式开关驱动器

1 特性

- 无需隔离式次级电源
- 驱动外部功率晶体管或 SCR
- 5-kV_{RMS} reinforced isolation
- 具有 1.5/3A 峰值拉电流和灌电流的 15-V 栅极驱动
- 适用于外部辅助电路的最高 50 mW 电源
- 支持交流或直流开关
- 支持双线或三线模式
- 七电平功率传输，电阻可选
- 提供功能安全
  - 有助于进行功能安全系统设计的文档
- -40°C 至 125°C 汽车类环境温度范围，符合 AEC-Q100 标准
- 安全相关认证
  - 计划：符合 DIN V VDE 0884-11:2017-01 标准的 7071V_{PK} 增强型隔离
  - 计划：符合 UL 1577 标准且长达 1 分钟的 5kV_{RMS} 隔离

2 应用

- 固态继电器 (SSR)
- 电池管理系统
- 车载充电器
- 混合动力、电动和动力总成系统
- 楼宇自动化
- 工厂自动化和控制

3 说明

TPSI3052-Q1 是一款完全集成的隔离式开关驱动器，与外部电源开关结合使用时，可构成完整的隔离式固态继电器 (SSR)。当标称栅极驱动电压为 15 V、峰值拉电流和灌电流为 1.5/3.0A 时，可以选择多种外部电源开关来满足各种应用需求。TPSI3052-Q1 可通过初级侧电源自行产生次级偏置电源，因此无需隔离式次级电源偏置。而且，TPSI3052-Q1 可以有选择性地向外部配套电路供电，以满足不同的应用需求。

TPSI3052-Q1 根据所需的输入引脚数量，支持两种工作模式。在双线模式（通常用于驱动机械继电器）中，控制开关仅需两个引脚，并支持 6.5V 至 48V 的宽工作电压范围。在三线模式中，由外部提供 3V 至 5.5V 的初级侧电源，并通过独立的使能引脚控制开关。TPSI3052S-Q1 具有可实现开关控制的一次性启用功能，且仅在三线模式下可用。此功能对于驱动 SCR 非常有用，通常只需要一个电流脉冲即可触发。

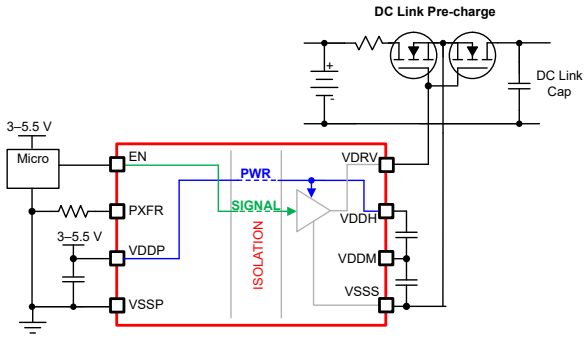
次级侧可为驱动多种电源开关提供 15 V 的浮动稳压电源轨，无需次级偏置电源。具体用途包括为直流应用驱动单个电源开关，或为交流应用驱动两个背靠背电源开关，以及各种类型的 SCR。TPSI3052-Q1 集成式隔离保护功能非常稳健，与传统机械继电器和光耦合器相比，其可靠性更高、功耗更低，且温度范围更宽。

使用从 PXFR 引脚到 VSSP 的外部电阻器在七个功率等级设置中选择一个，以调节 TPSI3052-Q1 的功率传输。此操作可根据应用需求权衡功率损耗与次级侧功耗。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPSI3052-Q1	SOIC 8 引脚 (DWZ)	7.50mm × 5.85mm
TPSI3052S-Q1	SOIC 8 引脚 (DWZ)	7.50mm × 5.85mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



TPSI3052-Q1 简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
April 2022	*	Initial Release

5 Pin Configuration and Functions

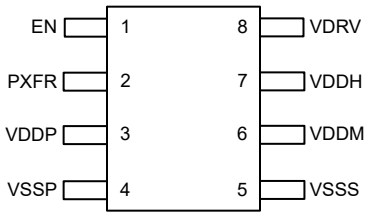

图 5-1. TPSI3052-Q1, TPSI3052S-Q1 8-Pin SOIC Top View

表 5-1. Pin Functions

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	EN	I	—	Active high driver enable
2	PXFR	I	—	Power transfer can be adjusted by selecting one of seven power level settings using an external resistor from the PXFR pin to VSSP. In three-wire mode, a given resistor setting sets the duty cycle of the power converter (see 表 8-1) and hence the amount of power transferred. In two-wire mode, a given resistor setting adjusts the current limit of the EN pin (see 表 8-2) and hence the amount of power transferred.
3	VDDP	—	P	Power supply for primary side
4	VSSP	—	GND	Ground supply for primary side
5	VSSS	—	GND	Ground supply for secondary side
6	VDDM	—	P	Generated mid supply
7	VDDH	—	P	Generated high supply
8	VDRV	O	—	Active high driver output

(1) P = power, GND = ground, NC = no connect

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER(1)		MIN	MAX	UNIT
Primary Side Supply(2)	VDDP	–0.3	6	V
Primary Side Supply(2)	EN	–0.3	60	V
Primary Side Supply(2)	PXFR	–0.3	60	V
Secondary Side Supply(3)	VDRV	–0.3	18	V
Secondary Side Supply(3)	VDDH	–0.3	18	V
Secondary Side Supply(3)	VDDM	–0.3	6	V
Secondary Side Supply(3)	VDDH-VDDM	–0.3	12	V
Junction temperature, T_J	Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to VSSP.
(3) All voltage values are with respect to VSSS.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C2a	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDDP	Primary side supply voltage(1)	3.0		5.5	V
EN	Enable in two-wire mode(1)	0		48.0	V
	Enable in three-wire mode(1)	0		5.5	V
PXFR	Power transfer control(1)	0		5.5	V
C_{IN}	Decoupling capacitance on VDDP and VSSP, two-wire mode(3)	220		500	nF
	Decoupling capacitance on VDDP and VSSP, three-wire mode(3)	0.22		20	µF
C_{DIV1} (2)	Decoupling capacitance across VDDH and VDDM(3)	0.004		15	µF
C_{DIV2} (2)	Decoupling capacitances across VDDM and VSSS(3)	0.012		40	µF
T_A	Ambient operating temperature	–40		125	°C

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	– 40		150	°C

(1) All voltage values are with respect to VSSP.
(2) C_{DIV1} and C_{DIV2} should be of same type and tolerance. C_{DIV2} capacitance value should be at least three times the capacitance value of C_{DIV1} i.e. $C_{DIV2} \geqslant 3 \times C_{DIV1}$.
(3) All capacitance values are absolute. Derating should be applied where necessary.

6.4 Thermal Information

THERMAL METRIC(1) (2)		DEVICE DWZ(SOIC) 8 PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	89.3	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	45.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44.4	°C/W

(1) Estimate only.
(2) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation, VDDP.	V_{VDDP} = 5 V, R_{PXFR} = 20 kΩ, three-wire mode, C_{VDRV} = 100 pF, C_{DIV1} = 33 nF, C_{DIV2} = 100 nF f_{EN} = 1-kHz square wave, V_{EN} = 5 V peak to peak.			250	mW
		R_{PXFR} = 20 kΩ, two-wire mode, C_{VDRV} = 100 pF, C_{DIV1} = 33 nF, C_{DIV2} = 100 nF f_{EN} = 1-kHz square wave, V_{EN} = 48 V peak to peak.k.			350	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
CREEPAGE AND TRACKING				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	⩾ 8.5	mm
CPG	External Creepage(1)	Shortest terminal-to-terminal distance across the package surface	⩾ 8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ⩽ 600 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 1000 V_{RMS}	I-III	
DIN V VDE 0884-11:2017-01, IEC 60747-17:2020				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V_{PK}

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6.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test.	1000	V_{RMS}
		DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$; t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$; t = 1 s (100% production).	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(2)	$V_{TEST} = 1.6 \times V_{IOSM} = 12000\ V_{PK}$ (qualification).	7500	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After input-output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM} = 1697\ V_{PK}$, t_m = 10 s.	⩽ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM} = 2262\ V_{PK}$, t_m = 10 s.	⩽ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM} = 2651\ V_{PK}$, t_m = 1 s.	⩽ 5	
C_{IO}	Barrier capacitance, input to output(4)	V_{IO} = 0.4 × sin (2 π ft), f = 1 MHz	3	pF
R_{IO}	Insulation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	> 10^{13}	Ω
		V_{IO} = 500 V, 100°C ⩽ T_A ⩽ 125°C	> 10^{12}	
		V_{IO} = 500 V at T_S =150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL
Plan to certify according to DIN V VDE 0884-11:2017-01	Plan to certify under UL 1577 Component Recognition Program
Reinforced insulation; Maximum transient isolation voltage, 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1414 V_{PK}; Maximum surge isolation voltage, 7500 V_{PK}	Single protection, 5000 V_{RMS}
Certificate planned	Certificate planned

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6.8 Safety Limiting Values

PARAMETER(1) (2)		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 89.3°C/W, V_{VDDP} = 5.5 V, T_J = 150°C, T_A = 25°C, three-wire mode.			254	mA
		$R_{\theta JA}$ = 89.3°C/W, V_{EN} = 24 V, T_J = 150°C, T_A = 25°C, two-wire mode.			58	
		$R_{\theta JA}$ = 89.3°C/W, V_{EN} = 48 V, T_J = 150°C, T_A = 25°C, two-wire mode.			29	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 89.3°C/W, T_J = 150°C, T_A = 25°C.			1.4	W
T_S	Maximum safety temperature				150	°C

(1) Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

(2) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

6.9 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25℃. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_{DRV} = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON						
$V_{VDDP\_UV\_R}$	VDDP under-voltage threshold rising	VDDP rising	2.50	2.70	2.90	V
$V_{VDDP\_UV\_F}$	VDDP under-voltage threshold falling	VDDP falling	2.35	2.55	2.75	V
$V_{VDDP\_UV\_HYS}$	VDDP under-voltage threshold hysterisis			150		mV
TSD	Temperature shutdown			173		℃
TSDH	Temperature shutdown hysteresis			32		℃
R_{DSON_VDRV}	Driver on resistance in low state.	Force V_{VDDH} = 15 V, sink I_{VDRV} = 50 mA.			2.5	Ω
	Driver on resistance in high state.	Force V_{VDDH} = 15 V, source I_{VDRV} = 50 mA.			5.2	Ω
$V_{VDDH\_UV\_R}$	VDDH under-voltage threshold rising	VDDH rising.	12.5	13	13.4	V
$V_{VDDH\_UV\_F}$	VDDH under-voltage threshold falling. TPSI3052-Q1 only.	VDDH falling.	11.1	11.4	11.9	V
	VDDH under-voltage threshold falling. TPSI3052S-Q1 only. One-shot enable only available in three-wire mode.	VDDH falling.	11.8	12.1	12.6	V

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6.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25℃. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_{DRV} = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDDH\_UV\_HYS}$	VDDH under-voltage threshold hysterisis. TPSI3052-Q1 only. One-shot enable only available in three-wire mode.			1.5		V
	VDDH under-voltage threshold hysterisis. TPSI3052S-Q1 only.			0.8		V
CMTI	Common-mode transient immunity	$\|V_{CM}\|$ = 1000 V			50	V/ns
TWO-WIRE MODE						
V_{IH_EN}	Minimum voltage on EN to be detected as a valid logic high.		6.5			V
V_{IL_EN}	Maximum voltage on EN to be detected as a valid logic low.				2.0	V
I_{EN_START}	Enable current at startup	EN = 0 V → 6.5 V		27		mA
I_{EN}	Enable current steady state	EN = 6.5 V, R_{PXFR} = 7.32 kΩ, R_{PXFR} ⩾100 kΩ or R_{PXFR} ⩽1 kΩ, V_{VDDH} in steady state.		1.9		mA
		EN = 6.5 V, R_{PXFR} = 20 kΩ, V_{VDDH} in steady state.		6.7		mA
V_{VDDP_H}	VDDP positive hysteretic control threshold	EN = 6.5 V, V_{VDDH} in steady state, measure positive peak VDDP level.		4.5		V
V_{VDDH}	VDDH output voltage	EN = 6.5 V, V_{VDDH} in steady state.	13.9	15	16.2	V
V_{VDRV_H}	VDRV output voltage driven high	EN = 6.5 V, V_{VDDH} in steady state, no DC loading.	13.9	15	16.2	V
V_{VDRV_L}	VDRV output voltage driven low	EN = 6.5 V, V_{VDDH} in steady state, sink 10 mA load.	0		0.1	V
I_{VDRV_PEAK}	VDRV peak output current during rise	EN = 0 V → 6.5 V, measure peak current.		1.5		A
	VDRV peak output current during fall	EN = 6.5 V → 0 V, measure peak current.		3		A
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	EN = 6.5 V, steady state. R_{PXFR} = 7.32 kΩ, R_{PXFR} ⩾ 100 kΩ or R_{PXFR} ⩽ 1 kΩ, C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, source 0.275 mA from VDDM, measure VDDM voltage.	4.7		5.5	V
	Average VDDM voltage when sourcing external current.	EN = 6.5 V, steady state. R_{PXFR} = 20 kΩ, C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, source 1.4 mA from VDDM, measure VDDM voltage.	4.7		5.5	V
THREE-WIRE MODE						
V_{IH_EN}	Minimum voltage on EN to be detected as a valid logic high. $V_{IH(min)}$ = 0.7 x V_{VDDP}	V_{VDDP} = 3 V	2.1			V
		V_{VDDP} = 5.5 V	3.85			V

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6.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25℃. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_{DRV} = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL_EN}	Maximum voltage on EN to be detected as a valid logic low.	V_{VDDP} = 3 V			0.9	V
		V_{VDDP} = 5.5 V			1.65	V
$V_{IT\_HYS(EN)}$	Input threshold voltage hysteresis on EN.	V_{VDDP} = 3 V		0.33		V
		V_{VDDP} = 5.5 V		0.5		V
I_{VDDP_START}	VDDP current at startup	EN = 0 V, V_{VDDP} = 0 V → 3.3 V, Measure average current while power conversion is active.		32		mA
I_{VDDP}	VDDP average current in steady state	EN = 3.3 V, V_{VDDP} = 3.3 V, R_{PXFR} = 7.32 kΩ, R_{PXFR} ⩾ 100 kΩ or R_{PXFR} ⩽ 1 kΩ, V_{VDDH} in steady state, measure I_{VDDP}.		4.5		mA
		EN = 3.3 V, V_{VDDP} = 3.3 V, R_{PXFR} = 20 kΩ, V_{VDDH} in steady state, measure I_{VDDP}.		33		
V_{VDDH}	VDDH output voltage	V_{VDDP} = 3.0 V, EN = 3.0 V, V_{VDDH} in steady state.	13.9	15	16.2	V
V_{VDRV_H}	VDRV output voltage driven high	V_{VDDP} = 3.0 V, EN = 3.0 V, V_{VDDH} in steady state, no DC loading.	13.9	15	16.2	V
V_{VDRV_L}	VDRV output voltage driven low	V_{VDDP} = 3.0 V, EN = 0 V, V_{VDDH} in steady state, VDRV sinking 10 mA.	0		0.1	V
I_{VDRV_PEAK}	VDRV peak output current during rise	V_{VDDP} = 3.3 V, EN = 0 V → 3.3 V, V_{VDDH} in steady state, measure peak current.		1.5		A
	VDRV peak output current during fall	V_{VDDP} = 3.3 V, EN =3.3 V → 0 V, V_{VDDH} in steady state, measure peak current.		3		A
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 3.3 V, EN = 0.0 V, steady state. R_{PXFR} = 7.32 kΩ, C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, Source 0.35 mA from VDDM measure V_{VDDM}.	4.7		5.5	V
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 5.0 V, EN = 0.0 V, steady state. R_{PXFR} = 7.32 kΩ, C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, Source 0.50 mA from VDDM measure V_{VDDM}.	4.7		5.5	V

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6.9 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25℃. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_{DRV} = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 3.3 V, EN = 0.0 V, steady state. R_{PXFR} = 20 kΩ C_{DIV1} = 75 nF, C_{DIV2} = 220 nF, Source 3.0 mA from VDDM measure V_{VDDM}.	4.7		5.5	V
V_{VDDM_IAUX}	Average VDDM voltage when sourcing external current.	V_{VDDP} = 5.0 V, EN = 0.0 V, steady state. R_{PXFR} = 20 kΩ C_{DIV1} = 75 nF C_{DIV2} = 220 nF Source 5.0 mA from VDDM measure V_{VDDM}.	4.7		5.5	V

6.10 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25℃. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_L = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TWO-WIRE MODE						
t_{LO_EN}	Low time of EN.		5			µs
$t_{LH\_VDDP\_H}$	Propagation delay time from EN rising to V_{VDDP_H}.	EN = 0 V → 6.5 V.		37		µs
t_{LH_VDDH}	Propagation delay time from EN rising to VDDH at 50% level.	EN = 0 V → 6.5 V, V_{VDDH} = 7.5 V.		175		µs
t_{HL_VDDH}	Propagation delay time from EN falling to VDDH at 50% level.	EN = 6.5 V → 0 V, V_{VDDH} = 7.5 V.		650		µs
t_{LH_VDRV}	Propagation delay time from EN rising to VDRV at 90% level.	EN = 0 V → 6.5 V, V_{VDRV} = 13.5 V.		450		µs
t_{HL_VDRV}	Propagation delay time from EN falling to VDRV at 10% level.	EN = 6.5 V → 0 V, V_{VDRV} = 1.5 V.		2.5	3.0	µs
t_{R_VDRV}	VDRV rise time from EN rising to VDRV from 15% to 85% level.	EN = 0 V → 6.5 V, V_{VDRV} = 2.25 V to 12.75 V.		5		ns
t_{F_VDRV}	VDRV fall time from EN falling to VDRV from 85% to 15% level.	EN = 6.5 V → 0 V, V_{VDRV} = 12.75 V to 2.25 V.		5		ns
THREE-WIRE MODE						
t_{LO_EN}	Low time of EN.	V_{VDDP} = 3.3 V, V_{VDDH} = steady state.	5			µs
t_{HI_EN}	High time of EN.	V_{VDDP} = 3.3 V, V_{VDDH} = steady state.	5			µs
t_{HI_VDRV}	High time of VDRV in one-shot enable mode. TPSI3052S-Q1 only. One-shot enable only available in three-wire mode.	V_{VDDP} = 3.3 V, steady state.		2.5		µs
t_{LH_VDDH}	Propagation delay time from VDDP rising to VDDH at 50% level.	EN = 0 V, V_{VDDP} = 0 V → 3.3 V at 1 V/µs, V_{VDDH} = 7.5 V.		60		µs

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6.10 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted). Typicals at T_A = 25℃. C_{IN} = 220 nF, C_{DIV1} = 5.1 nF, C_{DIV2} = 15 nF, C_L = 100 pF, R_{PXFR} = 7.32 kΩ ±1%

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{HL_VDDH}	Propagation delay time from VDDP falling to VDDH at 50% level	EN = 0 V, V_{VDDP} = 3.3 V → 0 V at -1 V/µs, V_{VDDH} = 7.5 V.		650		µs
t_{LH_VDRV}	Propagation delay time from EN rising to VDRV at 90% level	V_{VDDP} = 3.3 V, V_{VDDH} steady state, EN = 0 V → 3.3 V, V_{VDRV} = 13.5 V.		3	4	µs
t_{HL_VDRV}	Propagation delay time from EN falling to VDRV at 10% level	V_{VDDP} = 3.3 V, V_{VDDH} steady state, EN = 3.3 V → 0 V, V_{VDRV} = 1.5 V.		2.5	3.0	µs
$t_{HL\_VDRV\_PD}$	Propagation delay time from VDDP falling to VDRV at 10% level. Timeout mechanism due to loss of power on primary supply.	EN = 3.3 V, V_{VDDP} = 3.3 V → 0 V at -1 V/µs, V_{VDRV} = 1.5 V.		300		µs
t_{R_VDRV}	VDRV rise time from EN rising to VDRV from 15% to 85% level	V_{VDDP} = 3.3 V, V_{VDDH} steady state, EN = 0 V → 3.3 V, V_{VDRV} = 2.25 V to 12.75 V.		5		ns
t_{F_VDRV}	VDRV fall time from EN falling to VDRV from 85% to 15% level	V_{VDDP} = 3.3 V, V_{VDDH} steady state, EN = 3.3 V → 0 V, V_{VDRV} = 12.75 V to 2.25 V.		5		ns

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6.11 Insulation Characteristic Curves

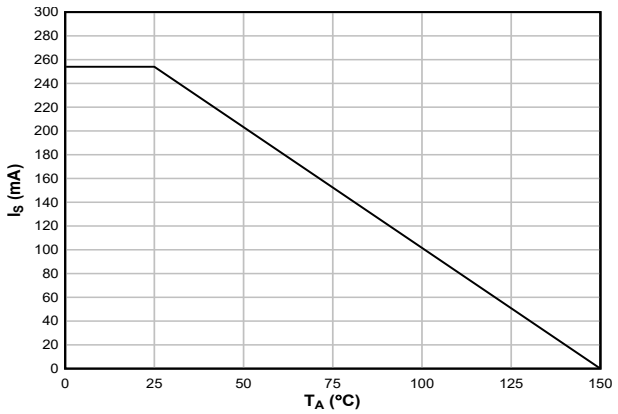

图 6-1. Thermal Derating Curve for Limiting Current per VDE and IEC, Three-Wire Mode

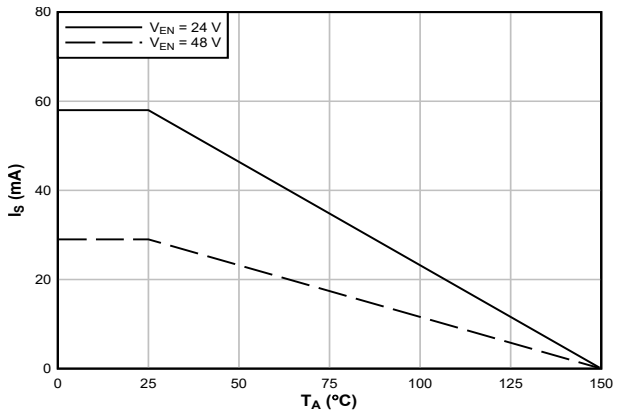

图 6-2. Thermal Derating Curve for Limiting Current per VDE and IEC, Two-Wire Mode

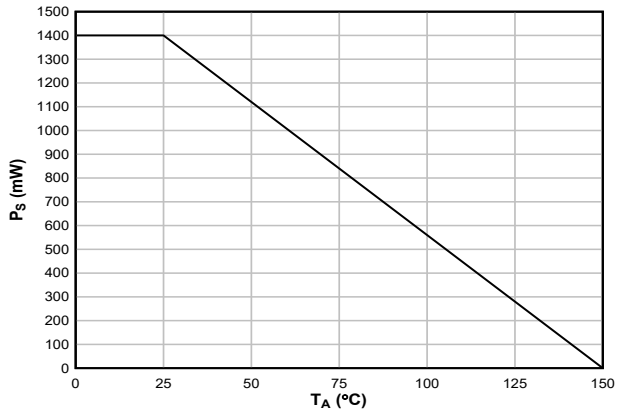

图 6-3. Thermal Derating Curve for Limiting Power per VDE and IEC

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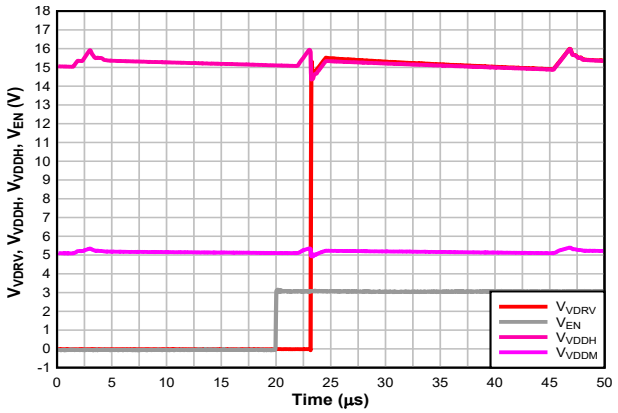
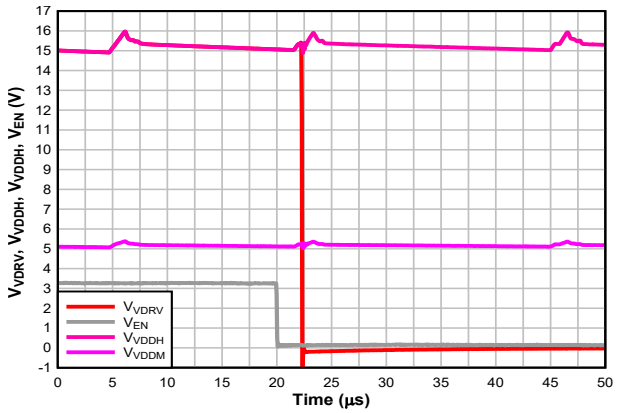
6.12 Typical Characteristics



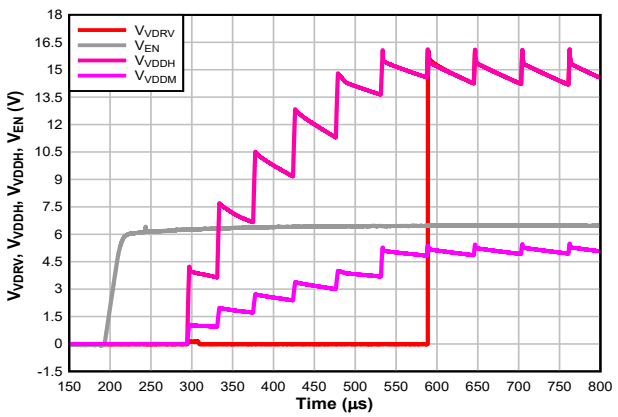
Three-wire mode VDDP = 5.0 V R_{PXFR} = 7.32 kΩ
C_{DIV1} = 5.1 nF C_{VDRV} = 100 pF T_A = 25°C
C_{DIV2} =15 nF

图 6-4. t_{LH_VDRV}, Three-Wire Mode, TPSI3052-Q1



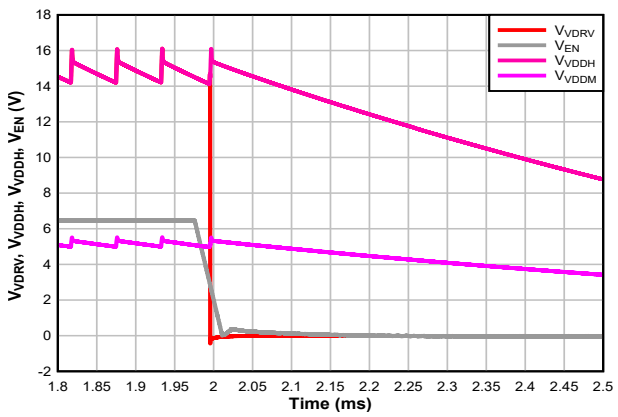
Three-wire mode VDDP = 5.0 V R_{PXFR} = 7.32 kΩ
C_{DIV1} = 5.1 nF C_{VDRV} = 100 pF T_A = 25°C
C_{DIV2} =15 nF

图 6-5. t_{HL_VDRV}, Three-Wire Mode, TPSI3052-Q1



Two-wire mode EN = 6.5 V R_{PXFR} = 7.32 kΩ
C_{DIV1} = 5.1 nF C_{VDRV} = 100 pF T_A = 25°C
C_{DIV2} =15 nF

图 6-6. t_{LH_VDRV}, Two-Wire Mode, TPSI3052-Q1



Two-wire mode EN = 6.5 V R_{PXFR} = 7.32 kΩ
C_{DIV1} = 5.1 nF C_{VDRV} = 100 pF T_A = 25°C
C_{DIV2} =15 nF

图 6-7. t_{HL_VDRV}, Two-Wire Mode, TPSI3052-Q1

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7 Parameter Measurement Information

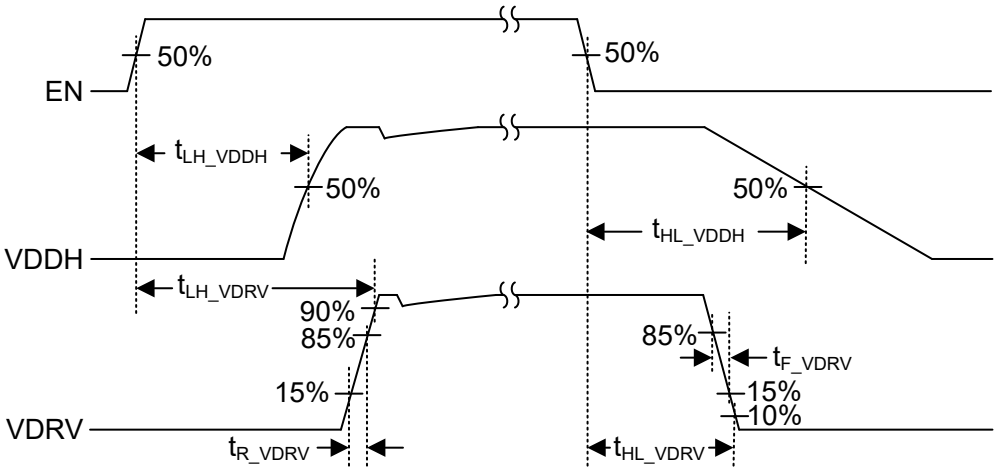

图 7-1. Two-Wire Mode Timing, Standard Enable (TPSI3052-Q1 Only)

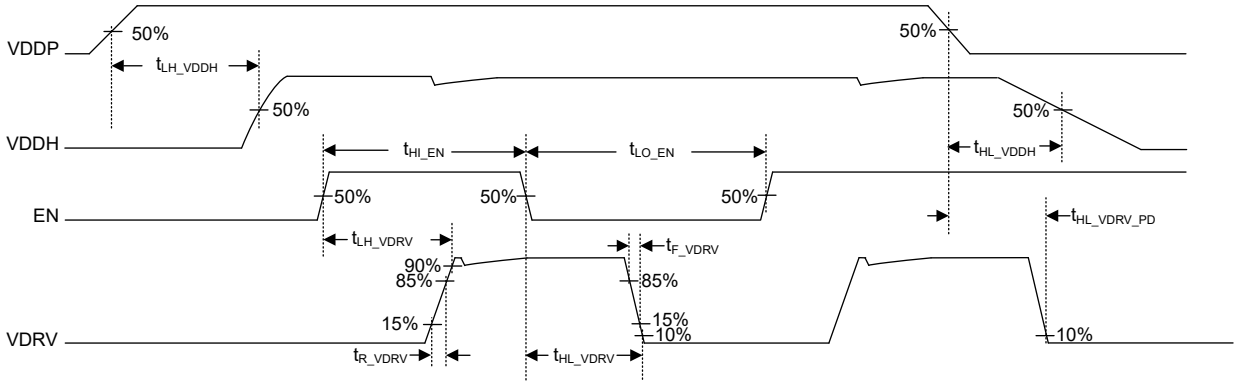

图 7-2. Three-Wire Mode Timing, Standard Enable (TPSI3052-Q1 Only)

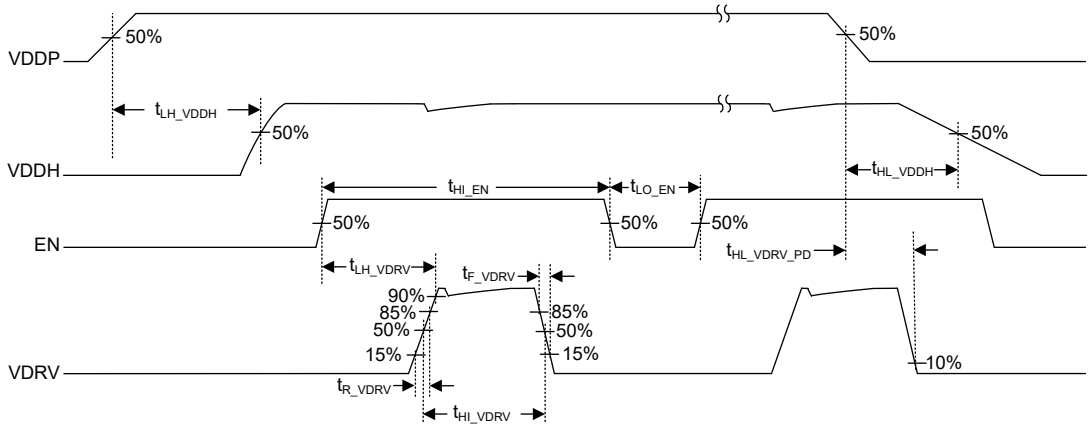

图 7-3. Three-Wire Mode Timing, One-Shot Enable (TPSI3052S-Q1 Only)

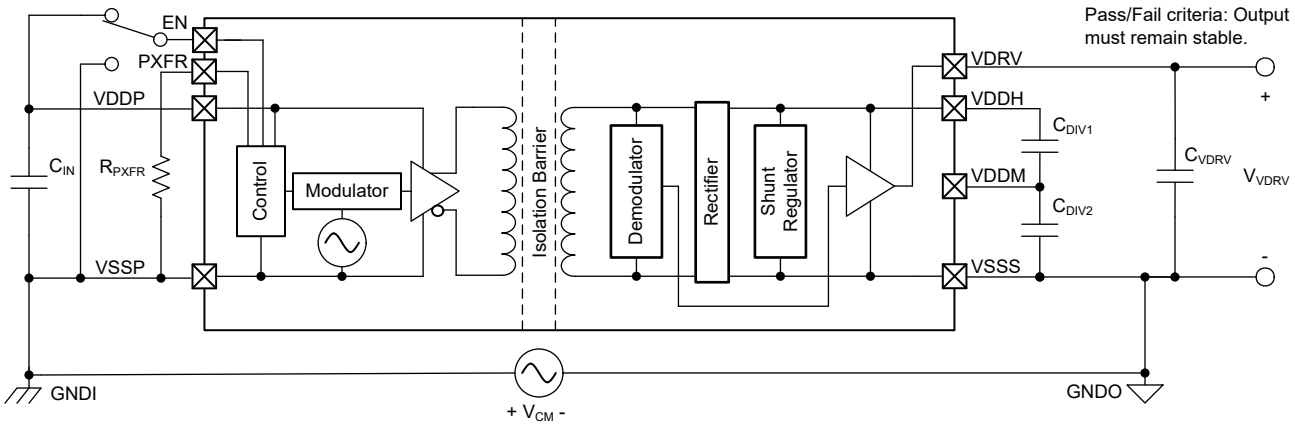

图 7-4. Common-Mode Transient Immunity Test Circuit

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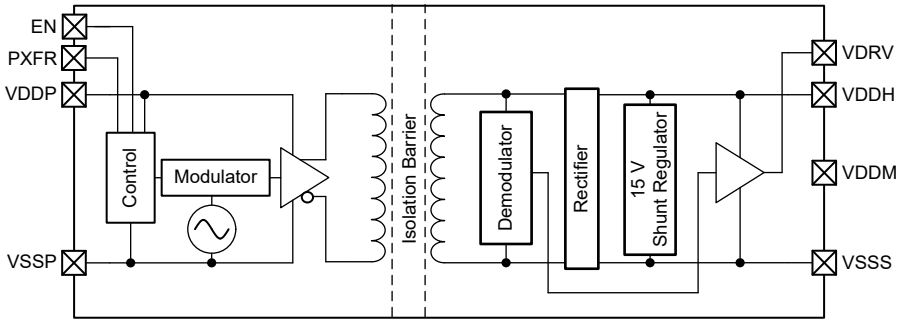
8 Detailed Description

8.1 Overview

The TPSI3052-Q1 is a fully integrated, reinforced isolated power switch driver, which when combined with an external power switch, forms a complete isolated power switch solution. With a nominal gate drive voltage of 15 V and 1.5/3.0-A peak source and sink current, a large variety of external power switches can be chosen to meet a wide range of applications. The TPSI3052-Q1 generates its own secondary supply from the power received from its primary side, so no isolated secondary bias supply is required.

The *Functional Block Diagram* shows the primary side that includes a transmitter that drives an alternating current into the primary winding of an integrated transformer at a rate determined by the setting of the PXFR pin and the logic state of the EN pin. The transmitter operates at high frequency to optimally drive the transformer to its peak efficiency. In addition, the transmitter uses spread spectrum techniques to greatly improve EMI performance, allowing many applications to achieve CISPR 25 - Class 5. During transmission, data information transfers to the secondary side alongside with the power. On the secondary side, the voltage induced on the secondary winding of the transformer is rectified, and the shunt regulator regulates the output voltage level of VDDH. Lastly, the demodulator decodes the received data information and drives VDRV high or low based on the logic state of the EN pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Transmission of the Enable State

The TPSI3052-Q1 and TPSI3052S-Q1 use a modulation scheme to transmit the switch enable state information across the isolation barrier. The transmitter modulates the EN signal with an internally generated, high frequency carrier (89-MHz typical), and differentially drives the primary winding of the isolation transformer. The receiver on the secondary side demodulates the received signal and asserts VDRV high or low based on the data received.

8.3.2 Power Transmission

The TPSI3052-Q1 and TPSI3052S-Q1 do not use a secondary side bias supply for their power. The secondary side power is obtained by the transferring of the primary side input power across the isolation transformer. The modulation scheme uses spread spectrum of the high frequency carrier (89-MHz typical) to improve EMI performance assisting applications in meeting the CISPR 25 Class 5 standards.

8.3.3 Gate Driver

The TPSI3052-Q1 and TPSI3052S-Q1 have an integrated gate driver that provides a nominal 15-V gate voltage with 1.5/3.0-A peak source and sink current sufficient for driving many power transistors or Silicon-Controlled Rectifiers (SCR). When driving external power transistors, TI recommends bypass capacitors (C_{DIV2} = 3 * C_{DIV1}) from VDDH to VDDM and VDDM to VSSS of 20 times the equivalent gate capacitance.

8.3.4 Modes Overview

The TPSI3052-Q1 and TPSI3052S-Q1 have two modes of operation: two-wire mode and three-wire mode.

In two-wire mode, the power on the primary side is provided directly by the EN pin. Setting EN high causes power transfer to the secondary side. As power transfers, the secondary rails, VDDM and VDDH, begin to rise. After sufficient power is available on the secondary side, VDRV is asserted high. Setting EN low causes VDRV to assert low and stop the power transfer to the secondary side.

In three-wire mode, the power on the primary side is provided by a dedicated, low output impedance supply connected to VDDP. In this case, power transfer is independent from the enable state. If VDDP power is present, power is transferred from the primary side to the secondary side regardless of the EN state. In steady state conditions, when sufficient power is available on the secondary side, setting EN high causes VDRV to assert high. Setting EN low causes VDRV to assert low.

In standard enable, available only on the TPSI3052-Q1, VDRV follows the state of the EN pin and is used in most load switch applications. In one-shot enable mode, available only on the TPSI3052S-Q1 in three-wire mode, when a rising transition occurs on EN, VDRV is asserted high momentarily and then automatically asserted low, forming a one-shot pulse on VDRV. This event is useful for driving SCR devices that require only one burst of power to trigger. To re-trigger VDRV, EN must first transition low, followed by another rising transition.

8.3.5 Three-Wire Mode

Three-wire mode is used for applications that require higher levels of power transfer or the shortest propagation delay TPSI3052-Q1 can offer. VDDP is supplied independently from the EN pin by a low output impedance external supply that can deliver the required power. In this mode, power from the primary side to the secondary side always occurs regardless of the state of the EN pin. Setting the EN pin logic high or low asserts or de-asserts VDRV, thereby enabling or disabling the external switch, respectively. 图 8-1 shows the basic setup required for three-wire mode operation which requires EN, VDDP, and VSSP signals. EN can be driven up to 5.5 V which is normally driven from the circuitry residing on the same rail as VDDP. In this example, the TPSI3052-Q1 is being used to drive back-to-back MOSFETs in a common-source configuration. C_{IN} provides the required decoupling capacitance for the VDDP supply rail of the device. C_{DIV1} and C_{DIV2} provide the required decoupling capacitances of the VDDH and VDDM supply rails that provide the peak current to drive the external MOSFETs.

图 8-2 and 图 8-3 show the basic operation from startup to steady state conditions. 图 8-2 shows operation using standard enable of the TPSI3052-Q1. After power up, the TPSI3052-Q1 begins to transfer power from VDDP to the secondary side for a fixed time period (25-μs typical) at a duty cycle rate determined by R_{PXFR}, which begins to charge up the VDDH (and VDDM) secondary side rails. Power transfer continues as long as VDDP is present. The time required to fully charge VDDH depends on several factors including the values of VDDP, C_{DIV1}, C_{DIV2}, R_{PXFR}, and the overall power transfer efficiency. When the application drives the EN pin to a logic high, the TPSI3052-Q1 signals information from the primary side to the secondary side to assert VDRV and drive it high. Similarly, setting EN pin to a logic low causes VDRV to be driven low. 图 8-3 shows operation using one-shot enable of the TPSI3052S-Q1. The start-up behavior is identical. In one-shot enable, when the application drives the EN pin to a logic high, VDRV is asserted high (t_{HI_VDRV}), then is automatically asserted low by the TPSI3052S-Q1. To assert VDRV high again, the EN pin must transition low first, followed by a transition high.

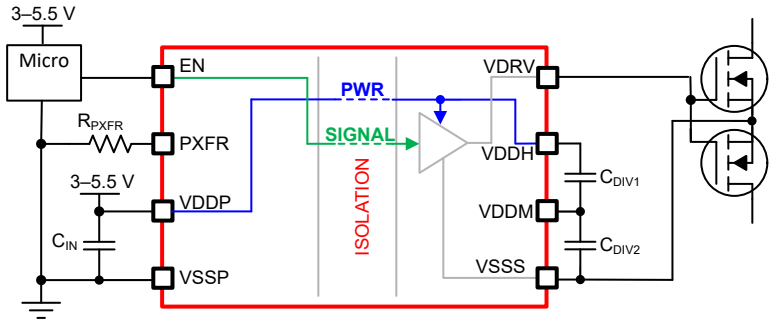


图 8-1. Three-Wire Mode Simplified Schematic

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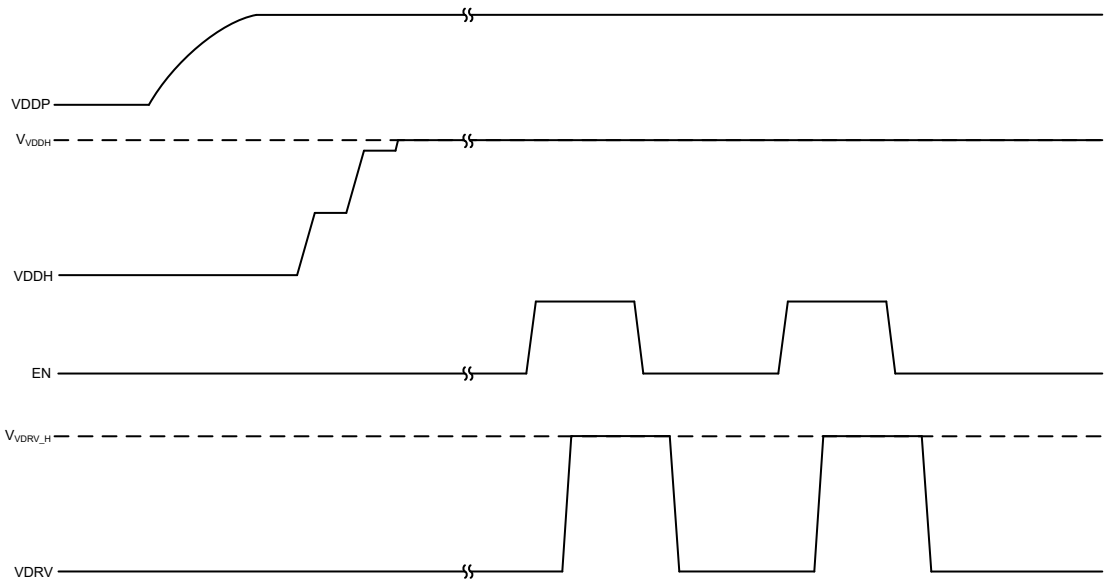

图 8-2. Three-Wire Mode with TPSI3052-Q1 (Standard Enable)

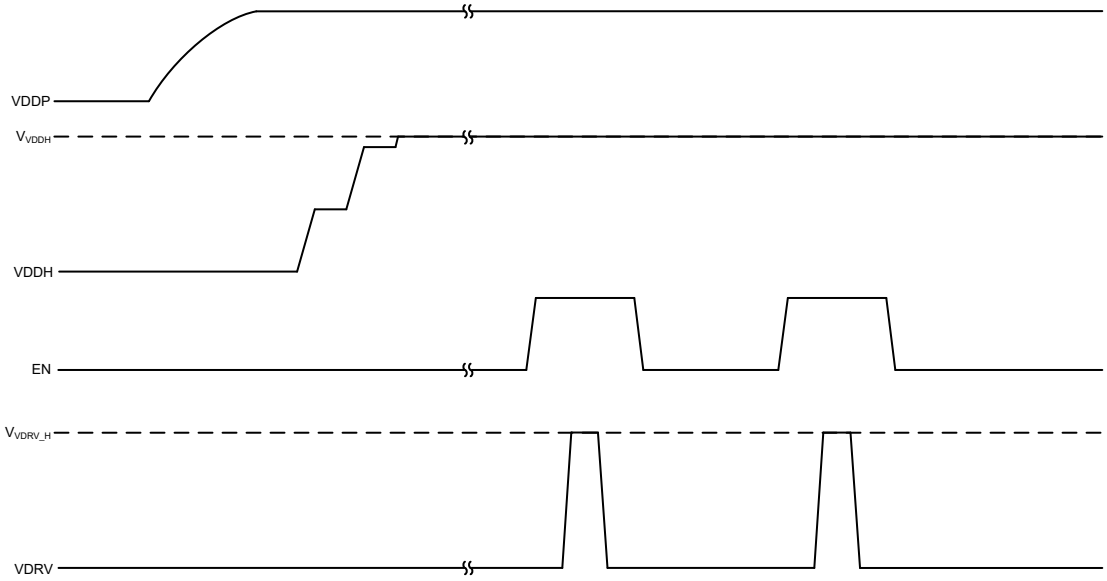

图 8-3. Three-Wire Mode with TPSI3052S-Q1 (One-shot Enable)

To reduce average power, the TPSI3052-Q1 transfers power from the primary side to the secondary side in a burst fashion. The period of the burst is fixed while the burst on time is programmable by selecting one of seven appropriate resistor values, R_{PXFR}, from the PXFR to VSSP pins, thereby changing the duty cycle of the power converter. This action provides flexibility in the application, allowing tradeoffs in power consumed versus power delivered. Higher power converter settings increase the burst on time which, in turn, increases average power consumed from the VDDP supply and increases the amount of power transferred to the secondary side VDDH and VDDM supplies. Similarly, lower power converter settings decrease the burst on time which, in turn, decreases average power consumed from the VDDP supply and decreases the amount of power transferred to the secondary side.

表 8-1 summarizes the three-wire mode power transfer selection.

表 8-1. Three-Wire Mode Power Transfer Selection

R_{PXFR} (1) (2)	Power Converter Duty Cycle (Three-Wire Mode, Nominal)	Description
7.32 kΩ	13.3%	The device supports seven, fixed power transfer settings, by selection of a corresponding R_{PXFR} value . Selecting a given power transfer setting adjusts the duty cycle of the power converter and hence the amount of power transferred. Higher power transfer settings leads to an increased duty cycle of the power converter leading to increased power transfer and consumption. During power up, the power transfer setting is determined and remains fixed at that setting until VDDP power cycles.
9.09 kΩ	26.7%	
11 kΩ	40.0%	
12.7 kΩ	53.3%	
14.7 kΩ	66.7%	
16.5 kΩ	80.0%	
20 kΩ	93.3%	

(1) Standard resistor (EIA E96), 1% tolerance, nominal value.
(2) $R_{PXFR} \geq 100$ kΩ or $R_{PXFR} \leq 1$ kΩ sets the duty cycle of the power converter to 13.3%.

8.3.6 Two-Wire Mode

图 8-4 shows the basic setup required for two-wire mode operation, which requires the EN signal and VSSP ground signal. EN can be driven up to 48 V. No current limiting resistor is required on EN because the TPSI3052-Q1 limits the input current based on the values set by the R_{PXFR} resistor (see 表 8-2). In this example, the TPSI3052-Q1 is being used to drive back-to-back MOSFETs in a common-source configuration. C_{IN} provides the required decoupling capacitance for the VDDP supply rail of the device. C_{DIV1} and C_{DIV2} provide the required decoupling capacitance of the VDDH and VDDM supply rails that provide the peak current to drive the external MOSFETs.

图 8-5 shows the typical operation in two-wire mode configured for standard enable. The application drives EN to a logic high and the TPSI3052-Q1 begins its power-up sequence. During power up, the current provided by the EN pin, I_{EN}, begins to charge up the external capacitance, C_{IN}, and the voltage on VDDP begins to rise until it reaches V_{VDDP_H}. After VDDP reaches V_{VDDP_H}, the TPSI3052-Q1 transfers stored energy on C_{IN} to the secondary side for a fixed time (3.3-μs typical) which begins to charge up the VDDH (and VDDM) secondary side rails thereby discharging the voltage on VDDP. This cycle repeats until the VDDH (and VDDM) secondary side rails are fully charged. The time required to fully charge VDDH depends on several factors including the values of C_{IN}, C_{DIV1}, C_{DIV2}, R_{PXFR}, and the overall power transfer efficiency. After VDDH is fully charged, VDRV is asserted high and remains high while the EN pin remains at a logic high. When the application drives the EN pin to a logic low, the charge on VDDP begins to discharge. Prior to VDDP reaching its UVLO falling threshold, TPSI3052-Q1 signals information from the primary side to the secondary side to de-assert VDRV and drive it low. Because power is no longer being transferred, all rails begin to fully discharge.

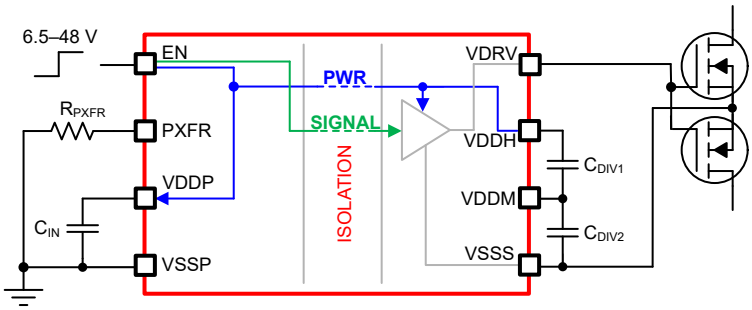

图 8-4. Two-Wire Mode Simplified Schematic

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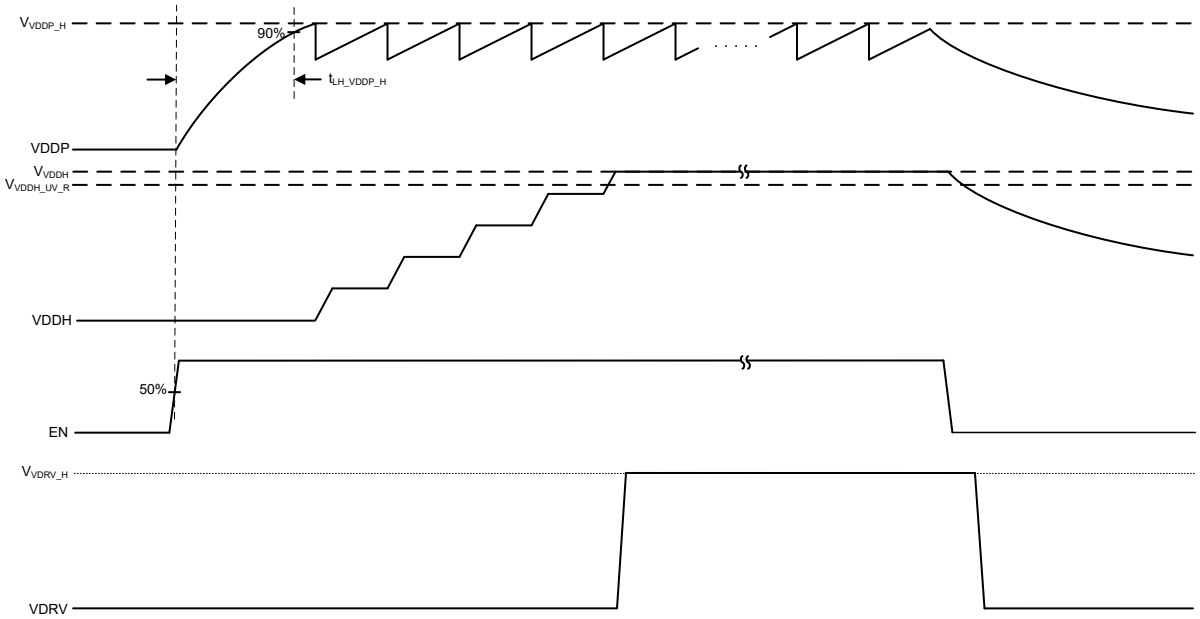

图 8-5. Two-Wire Mode with Standard Enable (TPSI3052-Q1 Only)

In two-wire mode, power is supplied directly by the EN pin. When EN is asserted high, the TPSI3052-Q1 transfers power to the secondary side for a fixed time (3.3- μ s nominal) while the time period varies. The period varies due to the hysteretic control of the power transfer that ensures the average current supplied through the EN pin is maintained. The amount of average current, and hence the amount of power transferred, is programmable by selecting one of seven appropriate resistor values, R_{PXFR}, from the PXFR to VSSP pins. Higher settings of R_{PXFR} increase I_{EN} which increases the average power consumed from the EN pin and increases the amount of power transferred to the secondary side VDDH supply. Similarly, lower settings of R_{PXFR} decrease I_{EN}, which decreases the average power consumed from the EN pin and decreases the amount of power transferred to the secondary side.

表 8-2 summarizes the two-wire mode power selection.

表 8-2. Two-Wire Mode Power Selection

R_{PXFR} (1) (2)	I_{EN} (Two-Wire Mode, Nominal)	Description
7.32 kΩ	1.9 mA	The device supports seven, fixed EN input current limit options selected by the corresponding R_{PXFR} specified value. Higher current limit selections lead to increased power transfer and consumption. During power up, the EN input current limit is determined and remains fixed at that setting until VDDP power cycles.
9.09 kΩ	2.8 mA	
11 kΩ	3.7 mA	
12.7 kΩ	4.5 mA	
14.7 kΩ	5.2 mA	
16.5 kΩ	6.0 mA	
20 kΩ	6.7 mA	

(1) Standard resistor (EIA E96), 1% tolerance, nominal value.
(2) $R_{PXFR} \geq 100$ kΩ or $R_{PXFR} \leq 1$ kΩ sets the I_{EN} to 1.9 mA.

8.3.7 VDDP and VDDH Undervoltage Lockout (UVLO)

TPSI3052-Q1 and TPSI3052S-Q1 implement an internal UVLO protection feature for both input and output power supplies, VDDP and VDDH. When either supply voltage is lower than the threshold voltage, the driver output, VDRV, is held low. VDRV only goes high when both VDDP and VDDH are out of the UVLO status. The UVLO protection blocks feature hysteresis, which helps to improve the noise immunity of the power supply. During turn-on and turn-off, the driver sources and sinks a peak transient current, which can result in voltage drop of the VDDH power supply. The internal UVLO protection block ignores the associated noise during these normal switching transients.

8.3.8 Thermal Shutdown

The device contains an integrated temperature sensor to monitor its local temperature. When the sensor reaches its threshold, it automatically ceases power transfer from the primary side to the secondary side. In addition, if power is still present on VDDP, the driver is automatically asserted low. The power transfer is disabled until the local temperature reduces enough to re-engage.

8.4 Device Functional Modes

表 8-3 summarizes the functional modes for the TPSI3052-Q1 and TPSI3052S-Q1.

表 8-3. TPSI3052-Q1, TPSI3052S-Q1 Device Functional Modes(1)

VDDP	VDDH	EN	VDRV	COMMENTS
Powered up(2)	Powered up(4)	L	L	Normal operation (TPSI3052-Q1 only): VDRV output state assumes logic state of EN logic state.
		H	H	
		L	L	Normal operation (TPSI3052S-Q1, three-wire mode only): rising edge of EN causes VDRV to be singly pulsed high. EN must be asserted low first to assert another pulse.
		L → H	L → H → L	
Powered down(3)	Powered down(5)	X	L	Disabled operation: VDRV output disabled, keep off circuitry applied.
Powered up(2)	Powered down(5)	X	L	Disabled operation: VDRV output disabled, keep off circuitry applied.
Powered down(3)	Powered up(4)	X	L	Disabled operation: when VDDP is powered down, output driver is disabled automatically after timeout, keep off circuitry applied.

(1) X: do not care.
(2) $V_{VDDP} \geqslant$ VDDP undervoltage lockout rising threshold, $V_{VDDP\_UV\_R}$.
(3) V_{VDDP} < VDDP undervoltage lockout falling threshold, $V_{VDDP\_UV\_F}$.
(4) $V_{VDDH} \geqslant$ VDDH undervoltage lockout rising threshold, $V_{VDDH\_UV\_R}$.
(5) V_{VDDH} < VDDH undervoltage lockout falling threshold, $V_{VDDH\_UV\_F}$.

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9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPSI3052-Q1 is a fully integrated, isolated switch driver with integrated bias, which when combined with an external power switch, forms a complete isolated solid state relay solution. With a nominal gate drive voltage of 15 V with 1.5/3.0-A peak source and sink current, a large variety of external power switches such as MOSFETs, IGBTs, or SCRs can be chosen to meet a wide range of applications. The TPSI3052-Q1 generates its own secondary bias supply from the power received from its primary side, so no isolated secondary supply bias is required.

The TPSI3052-Q1 supports two modes of operation based on the number of input pins required. In two-wire mode, typically found in driving mechanical relays, controlling the switch requires only two pins and supports a wide voltage range of operation of 6.5 V to 48 V. In three-wire mode, the primary supply of 3 V to 5.5 V is supplied externally, and the switch is controlled through a separate enable. Available in three-wire mode only, the TPSI3052S-Q1 features a one-shot enable for the switch control. This feature is useful for driving SCRs that typically require only one pulse of current to trigger.

The secondary side provides a regulated, floating supply rail of 15 V for driving a large variety of power switches with no need for a secondary bias supply. The TPSI3052-Q1 can support driving single power switch, dual back-to-back, parallel power switches for a variety of AC or DC applications. The TPSI3052-Q1 integrated isolation protection is extremely robust with much higher reliability, lower power consumption, and increased temperature ranges than those found using traditional mechanical relays and optocouplers.

The power dissipation of the TPSI3052-Q1 can be adjusted by an external resistor from the PXFR pin to VSSP. This feature allows for tradeoffs in power dissipation versus power provided on the secondary depending on the needs of the application.

9.2 Typical Application

The circuits in 图 9-1 and 图 9-2 show a typical application for driving silicon based MOSFETs in three-wire mode and two-wire mode, respectively.

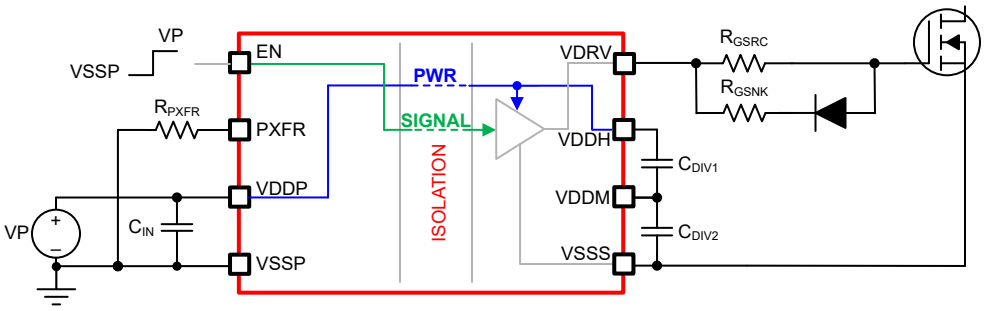

图 9-1. TPSI3052-Q1 Three-Wire Mode Driving MOSFETs

ADVANCE INFORMATION

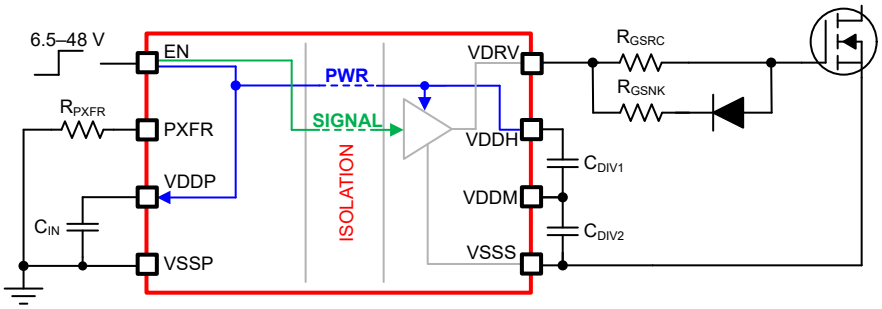

图 9-2. TPSI3052-Q1 Two-Wire Mode Driving MOSFETs

9.2.1 Design Requirements

表 9-1 lists the design requirements of the TPSI3052-Q1 gate driver.

表 9-1. TPSI3052-Q1 Design Requirements

DESIGN PARAMETERS	
Total gate capacitance	120 nC
FET turn-on time	1 µs
Propagation delay	< 4 µs
Switching frequency	10 kHz
Supply voltage (VDDP)	5 V ±5%

9.2.2 Detailed Design Procedure

9.2.2.1 Two-Wire or Three-Wire Mode Selection

The first design decision is to determine if two-wire or three-wire mode can be used in the application. For this design, note that the overall propagation delay is less than 4 µs and only three-wire mode is able to meet this requirement. In this case, two-wire mode is not applicable. Two-wire mode, due to its limited power transfer, is typically limited to very low frequency applications of less than a few kHz or when enable times are not critical.

9.2.2.2 Standard Enable, One-Shot Enable

Next, based on the application a decision must be if standard enable or one-shot enable mode is required. In this design, assume that after the switch is enabled, it is desired that the switch remain enabled until commanded to be disabled. Therefore, standard enable mode is assumed. In most applications that involve driving FETs, standard enable is appropriate. If driving SCRs or TRIACS, one-shot mode can be beneficial.

9.2.2.3 C_{DIV1}, C_{DIV2} Capacitance

The C_{DIV1} and C_{DIV2} capacitances required depends on the amount of drop that can be tolerated on the VDDH rail during switching of the external load. The charge stored on the CDIV1 and CDIV2 capacitances is used to provide the current to the load during switching. During switching, charge sharing occurs and the voltage on VDDH drops. At a minimum, TI recommends that the total capacitance formed by the series combination of C_{DIV1} and C_{DIV2} be sized to be at least 30 times the total gate capacitance to be switched. This sizing results in an approximate 0.5-V drop of the VDDH supply rail that is used to supply power to the VDRV signal. 方程式 1 and 方程式 2 can be to used to calculate the amount of capacitance required for a specified voltage drop.

C_{DIV1} and C_{DIV2} must be of the same type and tolerance.

$$C_{DIV1} = \left(\frac{n+1}{n}\right) \times \frac{Q_{LOAD}}{\Delta V},\ n \geq 3.0 \quad (1)$$

$$C_{DIV2} = n \times C_{DIV1},\ n \geq 3.0 \quad (2)$$

where

- n is a real number greater than or equal to 3.0.
- C_{DIV1} is the external capacitance from VDDH to VDDM.
- C_{DIV2} is the external capacitance from VDDM to VSSS.
- Q_{LOAD} is the total charge of the load from VDRV to VSSS.
- ΔV is the voltage drop on VDDH when switching the load.

备注

C_{DIV1} and C_{DIV2} represent absolute capacitances and components selected must be adjusted for tolerances and any derating necessary to achieve the required capacitances.

Larger values of ΔV can be used in the application, but excessive droop can cause the VDDH undervoltage lockout falling threshold ($V_{VDDH\_UVLO\_F}$) to be reached and cause VDRV to be asserted low. Note that as the series combination of C_{DIV1} and C_{DIV2} capacitances increases relative to Q_{LOAD}, the VDDH supply voltage drop decreases, but the initial charging of the VDDH supply voltage during power up increases.

For this design, assuming n = 3 and ΔV = 0.5 V, then

$$C_{DIV1} = \left(\frac{3+1}{3}\right) \times \frac{120\,nC}{0.5\,V} = 320\,nF \tag{3}$$

$$C_{DIV2} = 3 \times 320\,nF = 960\,nF \tag{4}$$

9.2.2.4 R_{PXFR} Selection

The selection of R_{PXFR} allows for a tradeoff between power consumed and power delivered, as described in the *Three-wire Mode* section. For this design, one must choose an appropriate R_{PXFR} selection that ensures enough power is transferred to support the amount of load being driven at the specified switching frequency.

During switching of the load, Q_{LOAD} of charge on VDDH is transferred to the load and VDDH supply voltage droops. After each switching cycle, this charge must be replenished before the next switching cycle occurs. This action ensures that the charge residing on VDDH does not deplete over time due to subsequent switching cycles of the load. The time it takes to recover this charge, $t_{RECOVER}$, can be estimated as follows:

$$t_{RECOVER} = \frac{1}{f_{MAX}} \cong \frac{Q_{LOAD}}{I_{OUT}} \tag{5}$$

where

- Q_{LOAD} is the load charge in Coulombs ©.
- I_{OUT} is the average current available from VDDH supply in Amperes (A).
- f_{MAX} is maximum switching frequency in Hertz (Hz).

For this design, Q_{LOAD} = 120 nC and f_{MAX} = 10 kHz are known, so I_{OUT} required can be estimated as

$$I_{OUT} \cong 120\,nC \times 10\,kHz = 1.2\,mA \tag{6}$$

I_{OUT} represents the minimum average current required to meet the design requirements. Using the TPSI3052-Q1 calculator tool, one can easily find the R_{PXFR} necessary by referring to the I_{OUT} or f_{MAX} columns directly. 表 9-2 shows the results from the tool, assuming VDDP = 4.75 V, to account for the supply tolerance specified in the design requirements. The TPSI3052-Q1 Calculator tool can be found at 表 12-1.

表 9-2. Results from the TPSI3052-Q1 Calculator Tool, Three-Wire Mode

R_{PXFR}, kΩ	Power Converter Duty Cycle, %	I_{VDDP}, mA	P_{IN}, mW	P_{OUT}, mW	I_{OUT}, mA	I_{OUT_CHG}, mA	t_{START}, µs	$t_{RECOVER}$, µs	f_{MAX}, kHz
7.32	13.3	4.13	19.3	5.6	0.37	0.37	6045	325.9	3.1
9.09	21.1	7.39	34.7	10.5	0.69	0.69	3241	173.3	5.8
11	40.0	15.29	72.3	23.0	1.52	1.52	1506	78.9	12.7

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表 9-2. Results from the TPSI3052-Q1 Calculator Tool, Three-Wire Mode (continued)

R_{PXFR}, kΩ	Power Converter Duty Cycle, %	I_{VDDP}, mA	P_{IN}, mW	P_{OUT}, mW	I_{OUT}, mA	I_{OUT_CHG}, mA	t_{START}, µs	$t_{RECOVER}$, µs	f_{MAX}, kHz
12.7	53.3	20.85	98.7	31.6	2.09	2.09	1112	57.4	17.4
14.7	66.7	26.45	125.3	40.2	2.66	2.66	885	45.1	22.2
16.5	80.0	32.00	151.7	49.4	3.27	3.27	732	36.7	27.2
20	93.3	37.56	178.1	58.0	3.84	3.84	631	31.2	32.0

表 9-3 summarizes the various output parameters of the calculator tool.

表 9-3. TPSI3052-Q1 Calculator Tool Parameter Descriptions

Parameter	Description
R_{PXFR}	External resistor setting that controls the amount of power transferred to the load by adjusting the duty cycle. Higher R_{PXFR} settings lead to increased power transfer and power consumption.
Power Converter Duty Cycle	Nominal duty cycle of the power converter. Higher R_{PXFR} settings leads to higher duty cycles of the power converter and higher power transfer.
I_{VDDP}	Average current consumed from the VDDP supply
P_{IN}	Average power consumed from the VDDP supply
P_{OUT}	Average power delivered to the VDDH supply
I_{OUT}	Average current delivered to the VDDH supply
I_{OUT_CHG}	Average current available to charge the load present on VDDH. If no auxiliary current is being supplied from VDDM, then I_{OUT_CHG} equals I_{OUT}.
t_{START}	Start-up time from VDDP rising until VDDH supply rail is fully charged. This parameter assumes VDDH and VDDM supply rails are fully discharged initially.
$t_{RECOVER}$	Represents the time for the VDDH rail to recover after switching the load present on VDRV
f_{MAX}	Maximum switching frequency possible for a given R_{PXFR} setting for the applied loading conditions

For this design example, R_{PXFR} must be configured to the 9.09-kΩ setting or higher to transfer enough power to support switching the specified load at the required 10-kHz frequency.

9.2.2.5 C_{IN} Capacitance

For two-wire mode, the recommended capacitance C_{IN} from VDDP to VSSP is 220 nF.

For this design, three-wire mode is required to meet the design requirements. For three-wire mode, increasing the amount of capacitance, C_{IN}, improves the ripple on the VDDP supply. For this design, 1 µF in parallel with 100 nF is used.

9.2.2.6 Gate Driver Output Resistor

The optional external gate driver resistors, R_{GSRC} and R_{GSNK}, along with the diode are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage switching dv/dt, high current switching di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength for sourcing and sinking
4. Reduce electromagnetic interference (EMI)

The TPSI3052-Q1 has a pullup structure with a P-channel MOSFET with a peak source current of 1.5 A. Therefore, the peak source current can be predicted with:

$$I_{O+} \cong min\left(1.5\ A,\ \frac{V_{VDDH}}{R_{DSON\_VDRV} + R_{GSRC} + R_{GFET\_INT}}\right) \quad (7)$$

where

- R_{GSRC}: external turn-on resistance.
- R_{DSON_VDRV}: TPSI3052-Q1 driver on resistance in high state. See *Electrical Characteristics*.
- V_{VDDH}: VDDH voltage. Assumed 15.1 V in this example.
- R_{GFET_INT}: external power transistor internal gate resistance, found in the power transistor data sheet. Assume 0 Ω for this example.
- I_{O+}: peak source current. The minimum value between 1.5 A, the gate driver peak source current, and the calculated value based on the gate drive loop resistance.

For this example, R_{DSON_VDRV} = 5.2 Ω, R_{GSRC} = 5.8 Ω, and R_{GFET_INT} = 0 Ω results in:

$$I_{O+} \cong min\left(1.5\ A, \frac{15.1\ V}{5.2\ \Omega + 5.8\ \Omega + 0\ \Omega}\right) = 1.37\ A \quad (8)$$

Similarly, the TPSI3052-Q1 has a pulldown structure with an N-channel MOSFET with a peak sink current of 3.0 A. Therefore, assuming R_{GFET_INT} = 0 Ω, the peak sink current can be predicted with:

$$I_{O-} \cong min\left[3.0\ A, (V_{VDDH} \times (R_{GSRC} + R_{GSNK}) - R_{GSRC} \times V_F) \times \frac{1}{R_{GSRC} \times R_{GSNK} + R_{DSON\_VDRV} \times (R_{GSRC} + R_{GSNK})}\right] \quad (9)$$

where

- R_{GSRC}: external turn-on resistance.
- R_{GSNK}: external turn-off resistance.
- R_{DSON_VDRV}: TPSI3052-Q1 driver on resistance in low state. See *Electrical Characteristics*.
- V_{VDDH}: VDDH voltage. Assumed 15.1 V in this example.
- V_F: diode forward voltage drop. Assumed 0.7 V in this example.
- I_{O-}: peak sink current. The minimum value between 3.0 A, the gate driver peak sink current, and the calculated value based on the gate drive loop resistance.

For this example, assuming R_{DSON_VDRV} = 2.5 Ω, R_{GSRC} = 5.8 Ω, R_{GSNK} = 5.0 Ω, and R_{GFET_INT} = 0 Ω, results in:

$$I_{O-} \cong min\left[3.0\ A, (15.1\ V \times (5.8\ \Omega + 5.0\ \Omega) - 5.8\Omega \times 0.7\ V) \times \frac{1}{5.8\ \Omega \times 5.0\ \Omega + 2.5\ \Omega \times (5.8\Omega + 5.0\ \Omega)}\right] = 2.84\ A \quad (10)$$

Importantly, the estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate driver loop can slow down the peak gate drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends to minimize the gate driver loop.

9.2.2.7 Start-up Time and Recovery Time

As described in the *C_{DIV1}, C_{DIV2} Capacitance* section, the start-up time of the fully discharged VDDH rail depends on the amount of capacitance present on the VDDH supply. The rate at which this capacitance is charged depends on the amount of power transferred from the primary side to the secondary side. The amount of power transferred can be adjusted by choosing R_{PXFR}. Increasing the resistor settings for R_{PXFR} transfers more power from the primary supply (VDDP) to the secondary supply (VDDH), thereby reducing the overall start-up and recovery times.

9.2.2.8 Supplying Auxiliary Current, I_{AUX} From VDDM

The TPSI3052-Q1 is capable of providing power from VDDM to support external auxiliary circuitry as shown in 图 9-3. In this case, the required transfer power must include the additional power consumed by the auxiliary circuitry on the VDDM rail. The R_{PXFR} value must be set to meet the overall power requirements.

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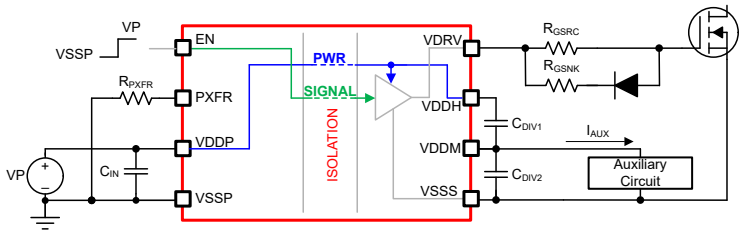

图 9-3. Supplying Auxiliary Power From VDDM

As an example, assume that the auxiliary circuitry requires an average current of 4 mA. 表 9-4 summarizes the results from the TPSI3052-Q1 calculator tool. The Calculator tool can be found at 表 12-1.

表 9-4. Results from the TPSI3052-Q1 Calculator Tool, Three-Wire Mode with I_{AUX} = 4 mA

R_{PXFR}, kΩ	Power Converter Duty Cycle, %	I_{VDDP}, mA	P_{IN}, mW	P_{OUT}, mW	I_{OUT}, mA	I_{OUT_CHG}, mA	t_{START}, µs	$t_{RECOVER}$, µs	f_{MAX}, kHz
7.32	13.3	4.13	19.3	5.6	0.37	N/A	N/A	N/A	N/A
9.09	21.1	7.39	34.7	10.5	0.69	N/A	N/A	N/A	N/A
11	40.0	15.29	72.3	23.0	1.52	0.17	12976	703.1	1.4
12.7	53.3	20.85	98.7	31.6	2.09	0.74	3039	162.3	6.2
14.7	66.7	26.45	125.3	40.2	2.66	1.31	1737	91.4	10.9
16.5	80.0	32.00	151.7	49.4	3.27	1.92	1207	62.6	16.0
20	93.3	37.56	178.1	58.0	3.84	2.49	942	48.2	20.8

Based on the results in 表 9-4, several observations can be made:

- With R_{PXFR} = 7.32 kΩ and R_{PXFR} = 9.09 kΩ, insufficient power is available to meet the application power needs .
- With R_{PXFR} = 11 kΩ, sufficient power is transferred, but f_{MAX} is lower than the 10 kHz specified in the design requirements in 表 9-1.
- With R_{PXFR} = 12.7 kΩ and higher, sufficient power is transferred to meet the specified design requirements.
- For a given R_{PXFR}, because some of the transferred power is being provided to the auxiliary circuitry, t_{START} can be significantly longer, and f_{MAX} reduced when compared to the results shown in 表 9-2 with I_{AUX} = 0 mA.

9.2.2.9 VDDM Ripple Voltage

Note that when supplying power from VDDM, that is when I_{AUX} > 0 mA, additional voltage ripple is present on the VDDM rail. For a given R_{PXFR} setting, this ripple can be reduced by applying additional capacitance from VDDM to VSSS. For this design example, the ripple on VDDM, $VDDM_{ripple}$, computed in the calculator tool is 63 mV.

It is possible to reduce the $VDDM_{ripple}$ with the addition of capacitance while still maintaining the original $VDDH_{droop}$ = 0.5V. For example, applying C_{DIV1} = 300 nF and C_{DIV2} = 1200 nF in the calculator tool, reduces $VDDM_{ripple}$ to 50 mV, while still maintaining $VDDH_{droop}$ = 0.5 V. This additional capacitance leads to increased t_{START} times.

10 Power Supply Recommendations

In three-wire mode, to help ensure a reliable supply voltage, TI recommends that the C_{IN} capacitance from VDDP to VSSP consists of a 0.1-µF bypass capacitor for high frequency decoupling in parallel with a 1 µF for low frequency decoupling.

In two-wire mode, TI recommends that the C_{IN} capacitance placed from VDDP to VSSP consists of a 220-nF capacitor connected close to the device between the VDDP and VSSP pins. The recommended absolute capacitance must be 220 nF, so if derating is required, a higher component value can be needed.

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Low-ESR and low-ESL capacitors must be connected close to the device between the VDDP and VSSP pins.

11 Layout

11.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the TPSI3052-Q1. Some key guidelines are:

- Component placement:
  - Place the driver as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDH and VDDM pins and the VDDM and VSSS pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - Connect low-ESR and low-ESL capacitors close to the device between the VDDP and VSSP pins.
  - Minimize parasitic capacitances on the R_{PXFR} pin.
- Grounding considerations:
  - Limit the high peak currents that charge and discharge the transistor gates to a minimal physical area. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. Place the gate driver as close as possible to the transistors.
  - Connect the driver VSSS to the Kelvin connection of MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, connect the VSSS pin as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. TI recommends a PCB cutout or groove to prevent contamination that can compromise the isolation performance.
- Thermal considerations:
  - Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - If the system has multiple layers, TI also recommends connecting the VDDH and VSSS pins to internal ground or power planes through multiple vias of adequate size. These vias must be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

ADVANCE INFORMATION

11.2 Layout Example

图 11-1 shows a PCB layout example with the signals and key components labeled.

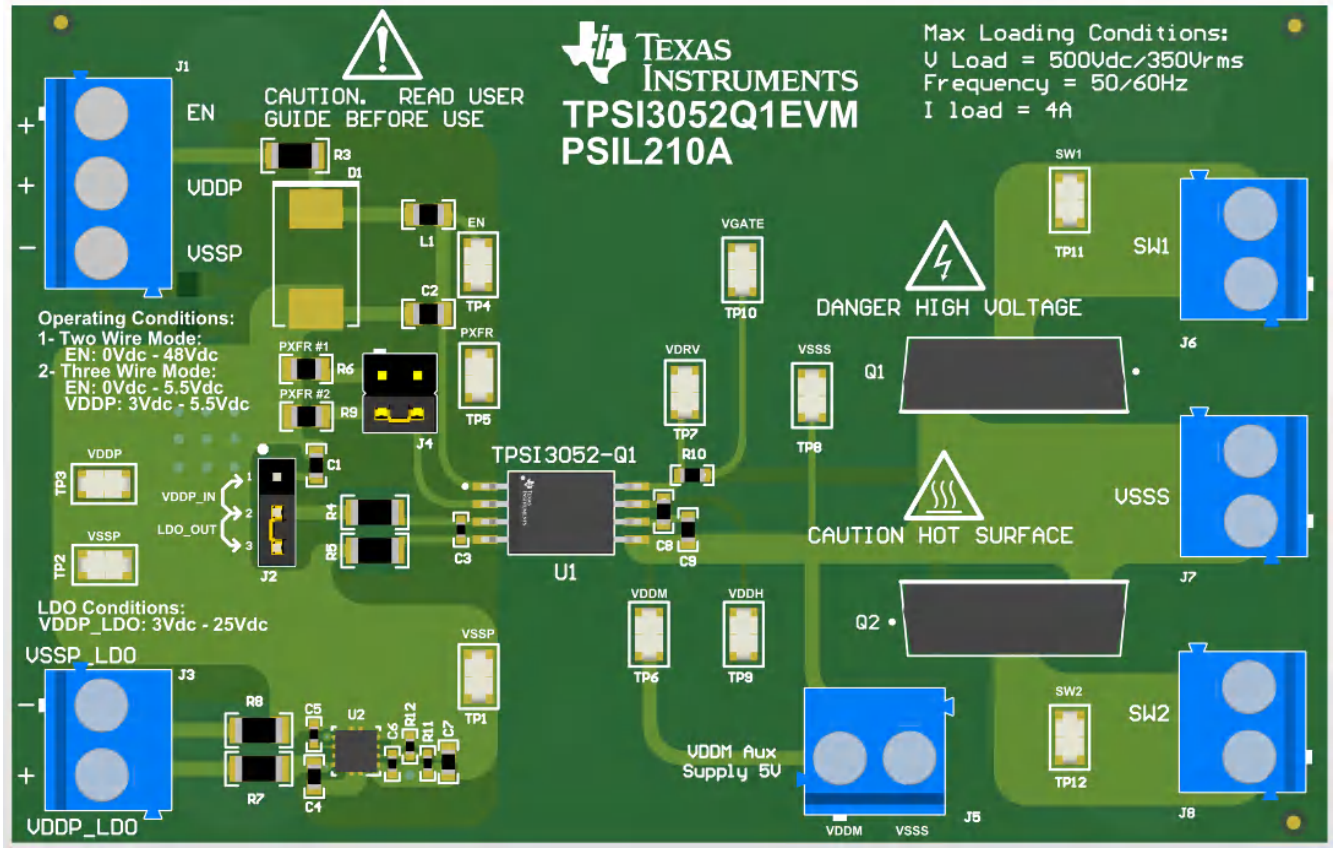


图 11-1. 3-D PCB View

图 11-2 and 图 11-3 show the top and bottom layer traces and copper.

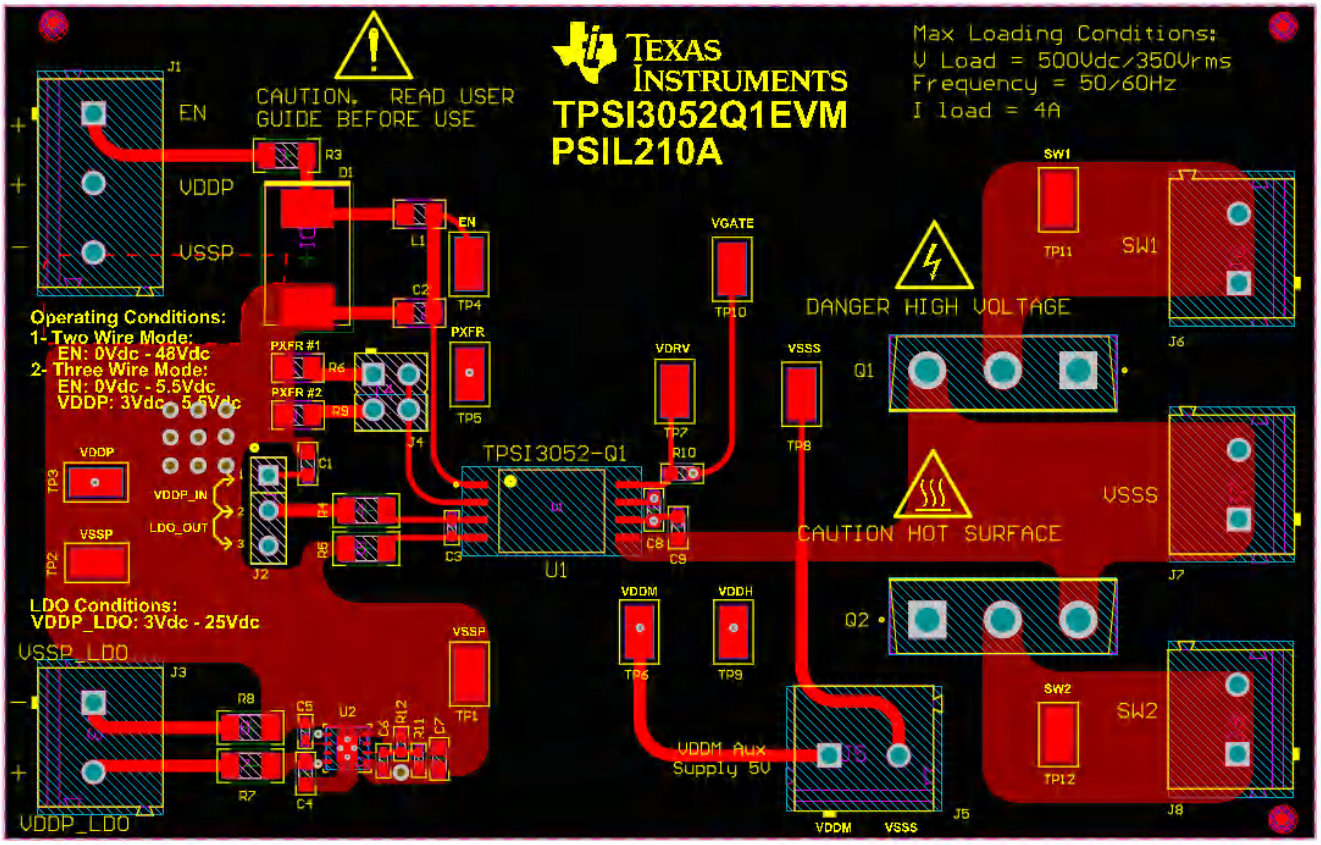


图 11-2. Top Layer

ADVANCE INFORMATION

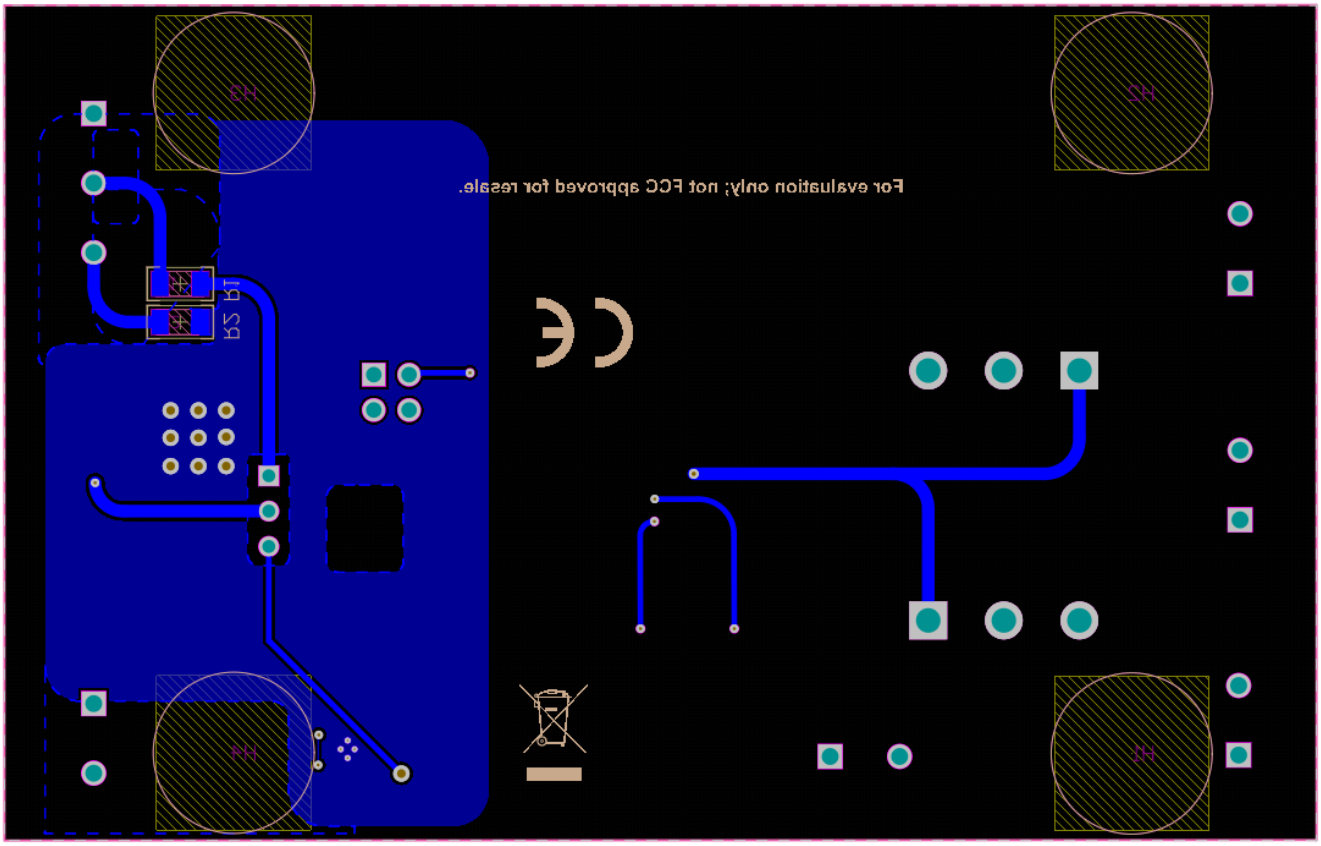


图 11-3. Bottom Layer

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 12-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPSI3052-Q1	Click here	Click here	Click here	Click here	Click here
TPSI3052S-Q1	Click here	Click here	Click here	Click here	Click here

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

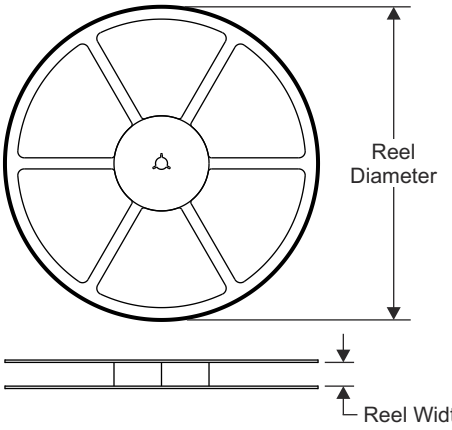
13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

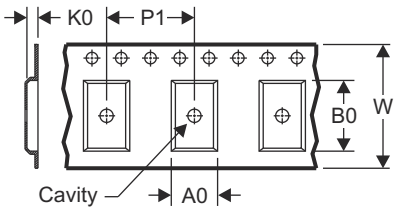
ADVANCE INFORMATION

13.1 Tape and Reel Information

REEL DIMENSIONS

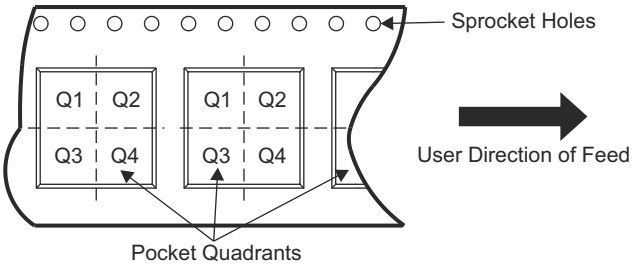


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

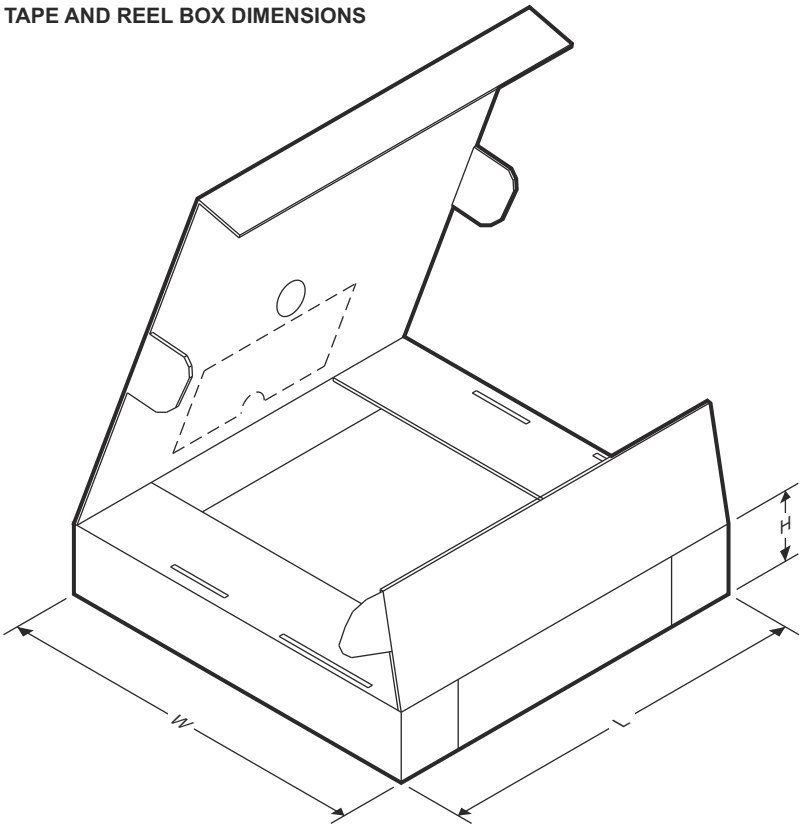
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPSI3052QDWZRQ1	SOIC	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
PTPSI3052SQDWZRQ1	SOIC	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3052QDWZRQ1	SOIC	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
TPSI3052SQDWZRQ1	SOIC	DWZ	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPSI3052QDWZRQ1	SOIC	DWZ	8	1000	350.0	350.0	43.0
PTPSI3052SQDWZRQ1	SOIC	DWZ	8	1000	350.0	350.0	43.0
TPSI3052QDWZRQ1	SOIC	DWZ	8	1000	350.0	350.0	43.0
TPSI3052SQDWZRQ1	SOIC	DWZ	8	1000	350.0	350.0	43.0

ADVANCE INFORMATION

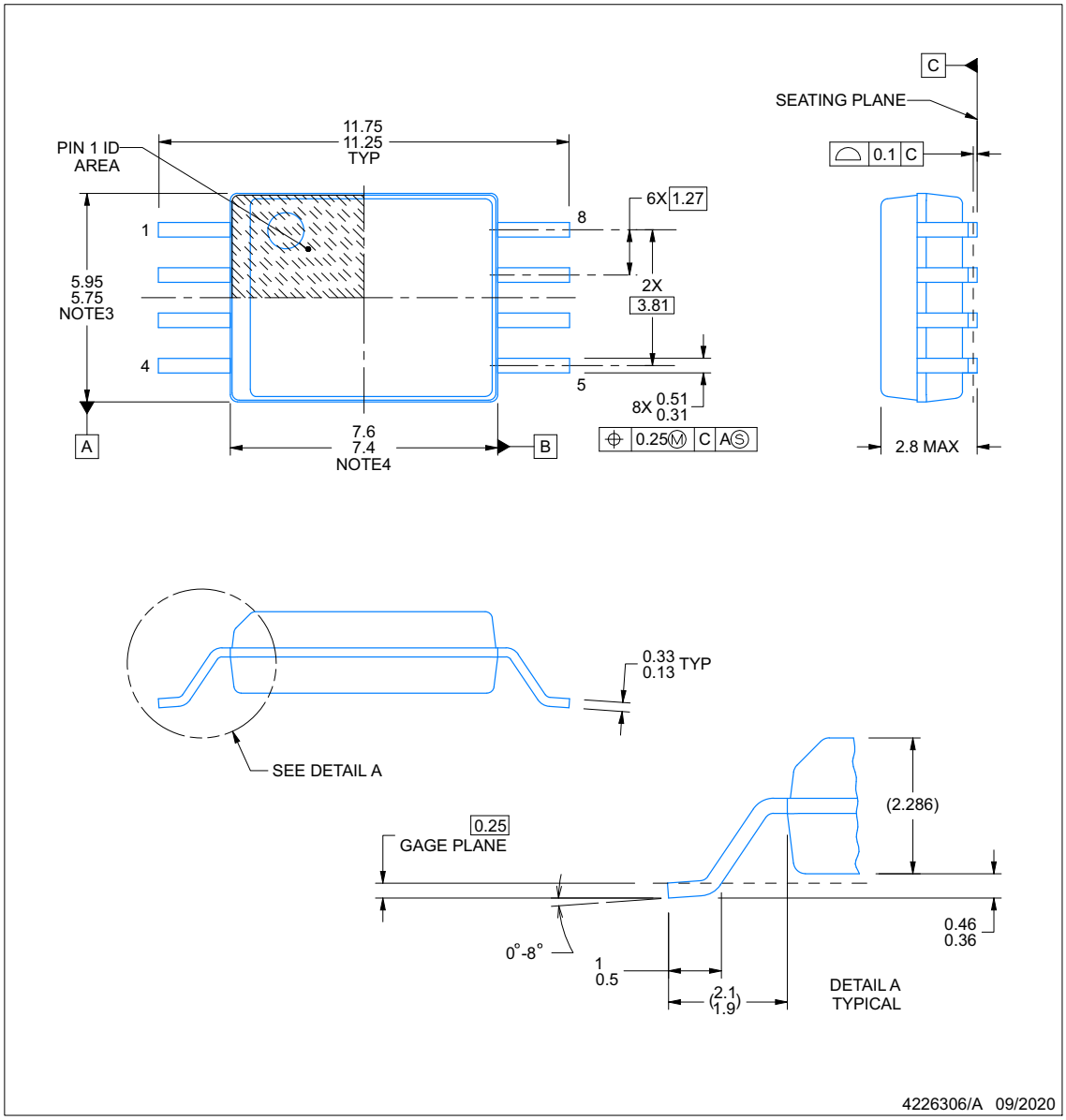
ADVANCE INFORMATION

PACKAGE OUTLINE

DWZ0008A

SOIC - 2.8 mm max height

SMALL OUTLINE PACKAGE



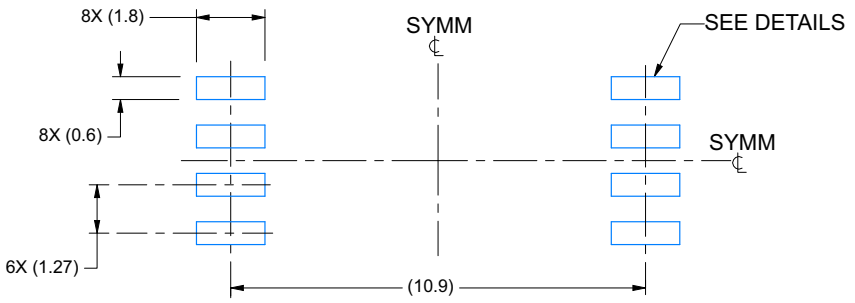
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

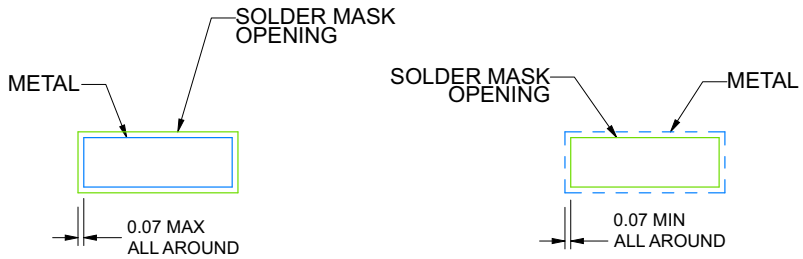
EXAMPLE BOARD LAYOUT

DWZ0008A — **SOIC - 2.8 mm max height**

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE: 6X



SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

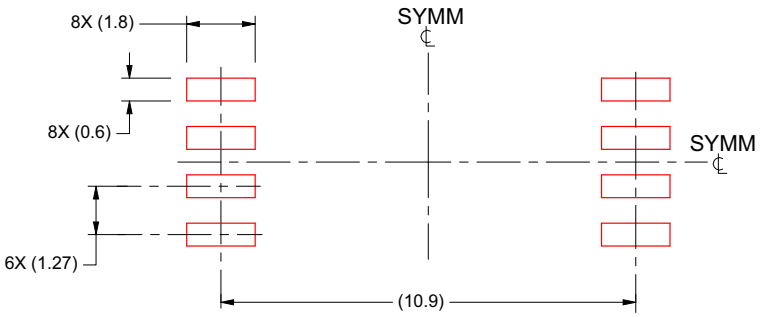
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DWZ0008A — **SOIC - 2.8 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

4226306/A 09/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPSI3052QDWZRQ1	ACTIVE	SO-MOD	DWZ	8	1000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPSI3052-Q1 :

- Catalog : TPSI3052

NOTE: Qualified Version Definitions:

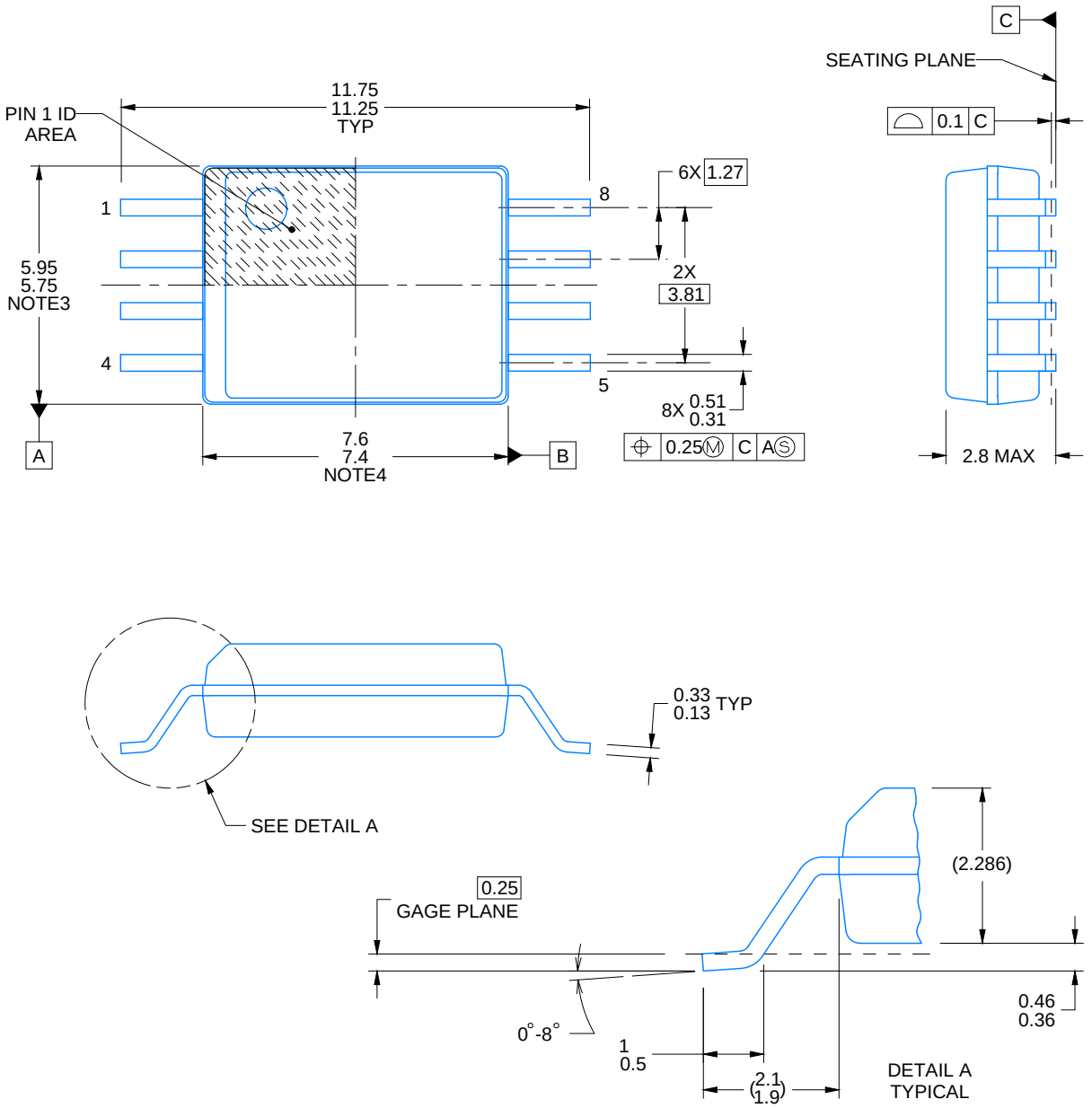
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DWZ0008A

SOIC - 2.8 mm max height

SMALL OUTLINE PACKAGE



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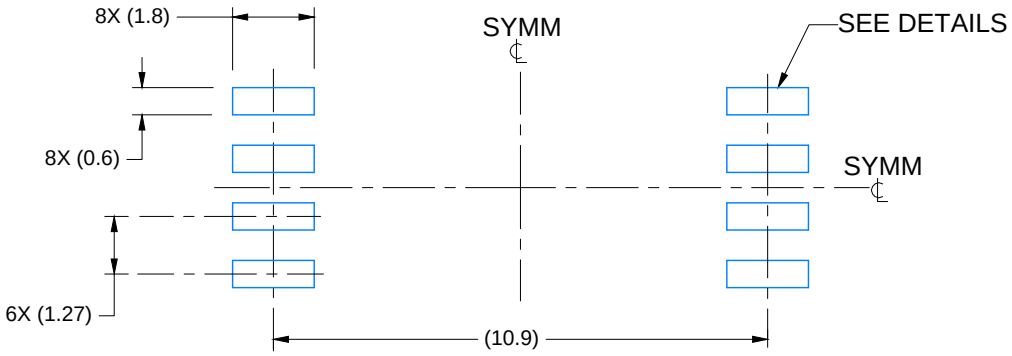
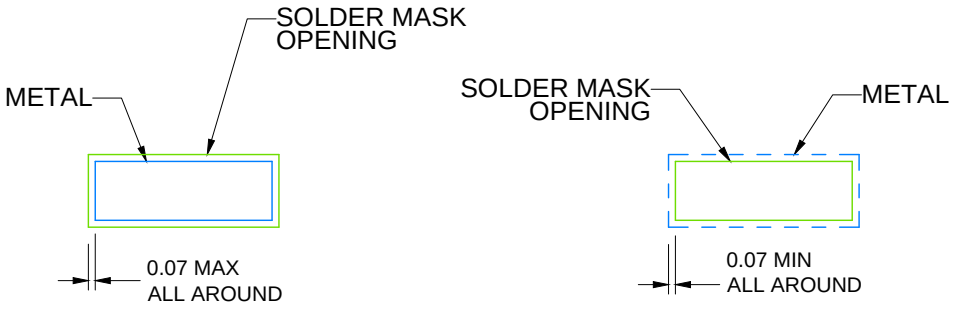
5. Ref. JEDEC registration MS-013



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE: 6X



NON SOLDER MASK
DEFINED

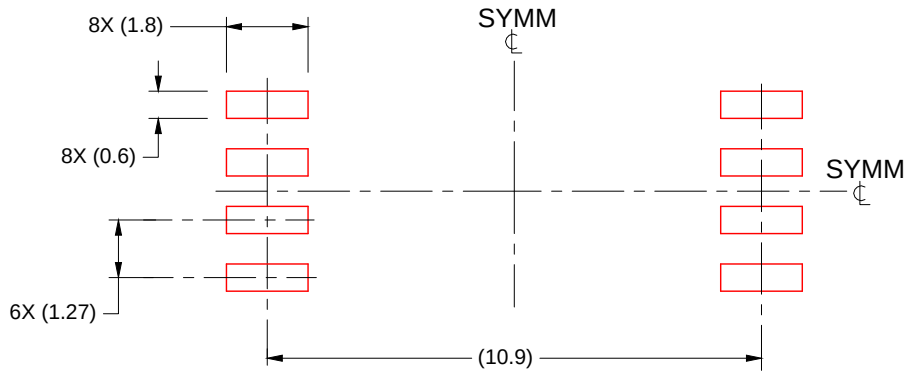
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226306/A 09/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

4226306/A 09/2020

NOTES: (continued)

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8. Board assembly site may have different recommendations for stencil design.

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