

## 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15$ -kV IEC ESD PROTECTION

Check for Samples: [TRS3243E](#)

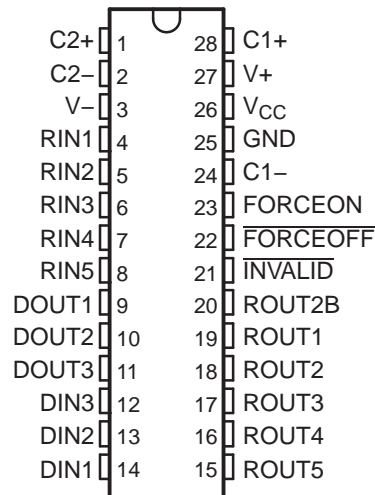
### FEATURES

- Single-Chip and Single-Supply Interface for IBM™ PC/AT™ Serial Port
- ESD Protection for RS-232 Bus Pins
  - $\pm 15$ -kV Human-Body Model (HBM)
  - $\pm 8$ -kV IEC61000-4-2, Contact Discharge
  - $\pm 15$ -kV IEC61000-4-2, Air-Gap Discharge
- Meets or Exceeds Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates With 3-V to 5.5-V  $V_{CC}$  Supply
- Always-Active Noninverting Receiver Output (ROUT2B)
- Designed to Transmit at a Data Rate up to 500 kbit/s
- Low Standby Current . . . 1  $\mu$ A Typ
- External Capacitors . . .  $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Designed to Be Interchangeable With Industry Standard '3243E Devices
- Serial-Mouse Driveability
- Auto-Powerdown Feature to Disable Driver Outputs When No Valid RS-232 Signal Is Sensed
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages

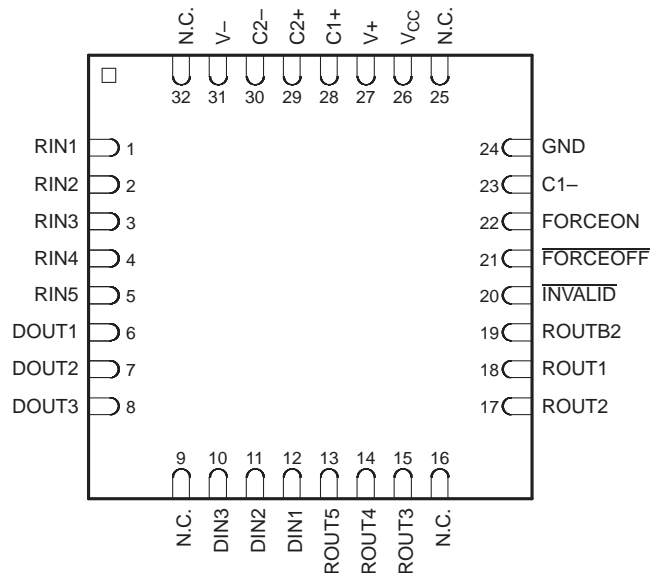
### APPLICATIONS

- Battery-Powered Systems
- PDAs
- Notebooks
- Laptops
- Palmtop PCs
- Hand-Held Equipment

DB, DW, OR PW PACKAGE  
(TOP VIEW)



QFN PACKAGE  
(TOP VIEW)



N.C. – Not internally connected



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## DESCRIPTION/ORDERING INFORMATION

The TRS3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and  $\pm 8$ -kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port used in an IBM PC/AT, or compatible. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1  $\mu$ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and  $\overline{\text{FORCEOFF}}$  are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than  $-2.7$  V or has been between  $-0.3$  V and 0.3 V for less than 30  $\mu$ s. INVALID is low (invalid data) if all receiver input voltages are between  $-0.3$  V and 0.3 V for more than 30  $\mu$ s. Refer to Figure 5 for receiver input levels.

The TRS3243EC is characterized for operation from 0°C to 70°C. The TRS3243EI is characterized for operation from  $-40^\circ\text{C}$  to 85°C.

**Table 1. ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	SSOP – DB	Reel of 2000	TRS3243ECDBR	TRS3243EC
	SOP – DW	Reel of 2000	TRS3243ECDWR	TRS3243EC
	TSSOP – PW	Reel of 2000	TRS3243ECPWR	RS43EC
	QFN – RHB	Reel of 2000	TRS3243ECRHBR	RS43EC
$-40^\circ\text{C}$ to 85°C	SSOP – DB	Reel of 2000	TRS3243EIDBR	TRS3243ECI
	SOP – DW	Reel of 2000	TRS3243EIDWR	TRS3243ECI
	TSSOP – PW	Reel of 2000	TRS3243EIPWR	RS43EI
	QFN – RHB	Reel of 2000	TRS3243EIRHBR	RS43EI

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## FUNCTION TABLES

### Each Driver<sup>(1)</sup>

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
X	L	H	No	Z	Powered off by auto-powerdown feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

### Each Receiver<sup>(1)</sup>

INPUTS			OUTPUT	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation with auto-powerdown disabled/enabled
H	X	H	L	
Open	X	H	H	

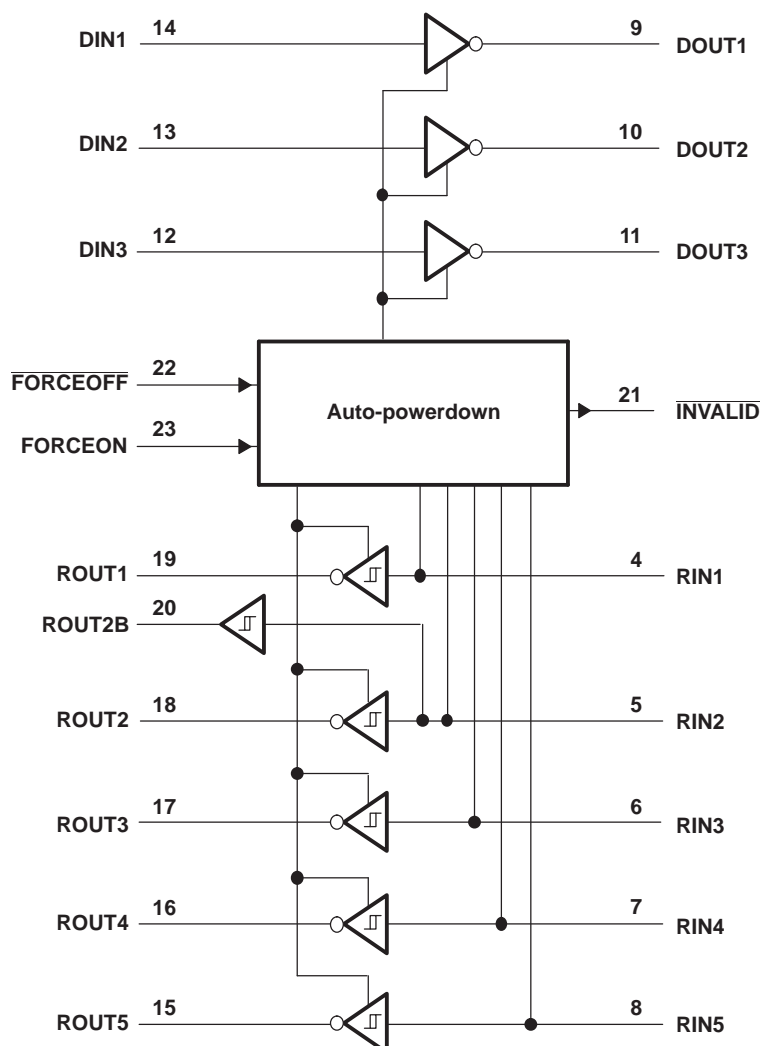
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

### ROUT2B and Outputs $\overline{\text{INVALID}}$ <sup>(1)</sup>

INPUTS				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
Yes	L	X	X	H	L	Always active
Yes	H	X	X	H	H	
Yes	Open	X	X	H	L	
No	Open	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

# **LOGIC DIAGRAM (POSITIVE LOGIC)**



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>		−0.3	6	V
V+	Positive output supply voltage range <sup>(2)</sup>		−0.3	7	V
V−	Negative output supply voltage range <sup>(2)</sup>		0.3	−7	V
V+ − V−	Output supply voltage difference <sup>(2)</sup>			13	V
V <sub>I</sub>	Input voltage range	Driver ( $\overline{\text{FORCEOFF}}$ , FORCEON)	−0.3	6	V
		Receiver	−25	25	
V <sub>O</sub>	Output voltage range	Driver	−13.2	13.2	V
		Receiver ( $\overline{\text{INVALID}}$ )	−0.3	V <sub>CC</sub> + 0.3	
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup> <sup>(4)</sup>	DB package		62	°C/W
		DW package		46	
		PW package		62	
Lead temperature 1,6 mm (1/16 in) from case for 10 s				260	°C
T <sub>stg</sub>	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T<sub>J</sub>(max),  $\theta_{JA}$ , and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J</sub>(max) – T<sub>A</sub>)/ $\theta_{JA}$ . Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

See [Figure 6](#)

		MIN	NOM	MAX	UNIT
Supply voltage	V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
	V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub> Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$ , FORCEON	V <sub>CC</sub> = 3.3 V	2		V
		V <sub>CC</sub> = 5 V	2.4		
V <sub>IL</sub> Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$ , FORCEON			0.8	V
V <sub>I</sub> Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$ , FORCEON	0		5.5	V
V <sub>I</sub> Receiver input voltage		–25		25	V
T <sub>A</sub> Operating free-air temperature	TRS3243EC	0		70	°C
	TRS3243EI	–40		85	

- (1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.

## Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
I <sub>I</sub> Input leakage current	$\overline{\text{FORCEOFF}}$ , FORCEON		$\pm 0.01$	$\pm 1$	$\mu$ A
I <sub>CC</sub> Supply current (T <sub>A</sub> = 25°C)	Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V <sub>CC</sub>	0.3	1	mA
	Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND	1	10	
	Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ at V <sub>CC</sub> , FORCEON at GND, All RIN are open or grounded, All DIN are grounded	1	10	$\mu$ A

- (1) Test conditions are C1–C4 = 0.1  $\mu$ F at V<sub>CC</sub> = 3.3 V  $\pm$  0.3 V; C1 = 0.047  $\mu$ F, C2–C4 = 0.33  $\mu$ F at V<sub>CC</sub> = 5 V  $\pm$  0.5 V.
- (2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## DRIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub> High-level output voltage	All DOUT at R <sub>L</sub> = 3 kΩ to GND	5	5.4		V
V <sub>OL</sub> Low-level output voltage	All DOUT at R <sub>L</sub> = 3 kΩ to GND	–5	–5.4		V
V <sub>O</sub> Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V <sub>CC</sub> , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5			V
I <sub>IH</sub> High-level input current	V <sub>I</sub> = V <sub>CC</sub>		±0.01	±1	μA
I <sub>IL</sub> Low-level input current	V <sub>I</sub> at GND		±0.01	±1	μA
V <sub>hys</sub> Input hysteresis				±1	V
I <sub>OS</sub> Short-circuit output current <sup>(3)</sup>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V			±60	mA
	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V				
r <sub>O</sub> Output resistance	V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = ±2 V	300	10M		Ω
I <sub>off</sub> Output leakage current	FORCEOFF = GND, V <sub>O</sub> = ±12 V, V <sub>CC</sub> = 0 to 5.5 V			±25	μA

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### Switching Characteristics<sup>(1)</sup>

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
Maximum data rate	C <sub>L</sub> = 1000 pF, R <sub>L</sub> = 3 kΩ One DOUT switching, See Figure 1	250	500		kbit/s
t <sub>sk(p)</sub> Pulse skew <sup>(3)</sup>	C <sub>L</sub> = 150 pF to 2500 pF, R <sub>L</sub> = 3 kΩ to 7 kΩ, See Figure 2		100		ns
SR(tr) Slew rate, transition region (see Figure 1)	V <sub>CC</sub> = 3.3 V, R <sub>L</sub> = 3 kΩ to 7 kΩ, PRR = 250 kbit/s			6	V/μs
	C <sub>L</sub> = 150 pF to 1000 pF			30	
	C <sub>L</sub> = 150 pF to 2500 pF			4	30

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

### ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver outputs (pins 9–11)	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

## RECEIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = –1 mA	V <sub>CC</sub> – 0.6	V <sub>CC</sub> – 0.1		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OH</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.6	2.4	V
		V <sub>CC</sub> = 5 V		1.9	2.4	
V <sub>IT–</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
		V <sub>CC</sub> = 5 V	0.8	1.4		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> – V <sub>IT–</sub> )			0.5		V
I <sub>off</sub>	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	µA
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See Figure 3	150	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output		150	ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See Figure 4	200	ns
t <sub>dis</sub>	Output disable time		200	ns
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	See Figure 3	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

### ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver outputs (pins 4–8)	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

## AUTO-POWERDOWN SECTION

### Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for <b>INVALID</b> high-level output voltage	FORCEON = GND, FORCEOFF = $V_{CC}$		2.7	V
$V_{IT-(valid)}$	Receiver input threshold for <b>INVALID</b> high-level output voltage	FORCEON = GND, FORCEOFF = $V_{CC}$	-2.7		V
$V_{T(invalid)}$	Receiver input threshold for <b>INVALID</b> low-level output voltage	FORCEON = GND, FORCEOFF = $V_{CC}$	-0.3	0.3	V
$V_{OH}$	<b>INVALID</b> high-level output voltage	$I_{OH} = -1\text{ mA}$ , FORCEON = GND, FORCEOFF = $V_{CC}$	$V_{CC} - 0.6$		V
$V_{OL}$	<b>INVALID</b> low-level output voltage	$I_{OL} = 1.6\text{ mA}$ , FORCEON = GND, FORCEOFF = $V_{CC}$		0.4	V

### Switching Characteristics

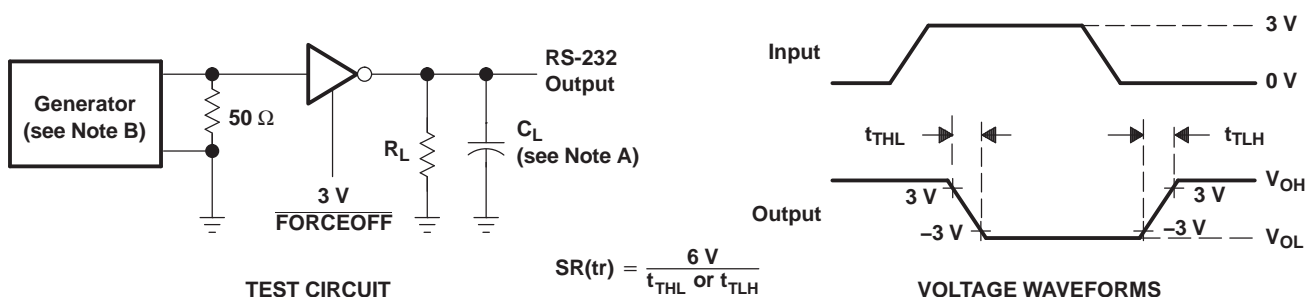
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	UNIT
$t_{valid}$	Propagation delay time, low- to high-level output	$V_{CC} = 5\text{ V}$	1	$\mu\text{s}$
$t_{invalid}$	Propagation delay time, high- to low-level output	$V_{CC} = 5\text{ V}$	30	$\mu\text{s}$
$t_{en}$	Supply enable time	$V_{CC} = 5\text{ V}$	100	$\mu\text{s}$

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

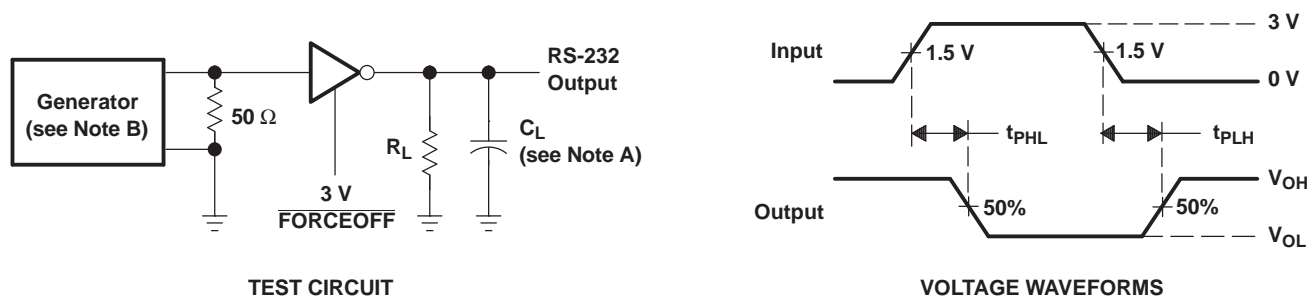


## PARAMETER MEASUREMENT INFORMATION



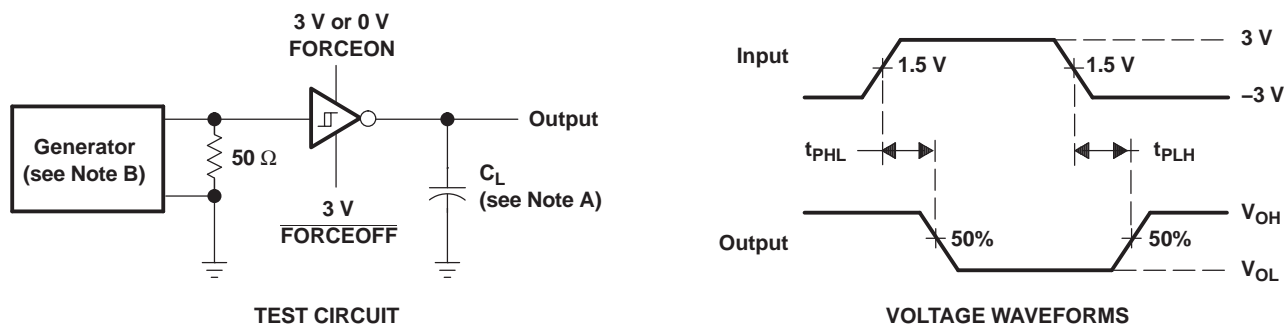
NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

Figure 1. Driver Slew Rate



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

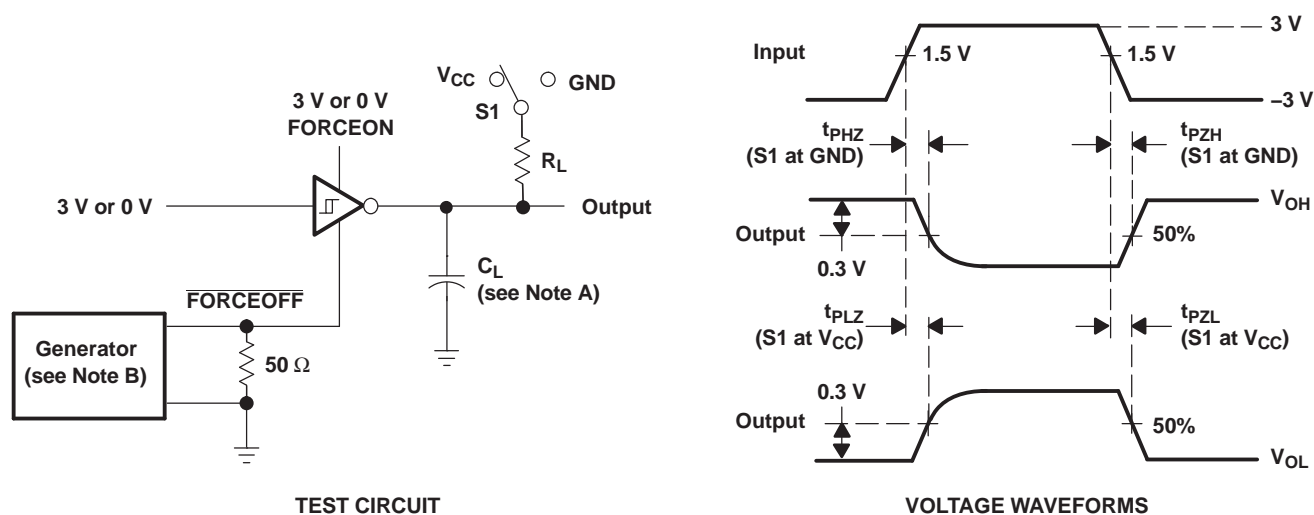
Figure 2. Driver Pulse Skew



NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .

Figure 3. Receiver Propagation Delay Times

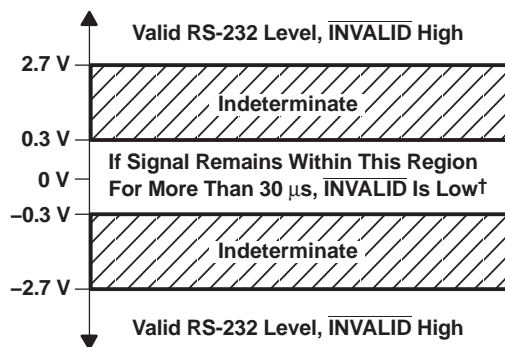
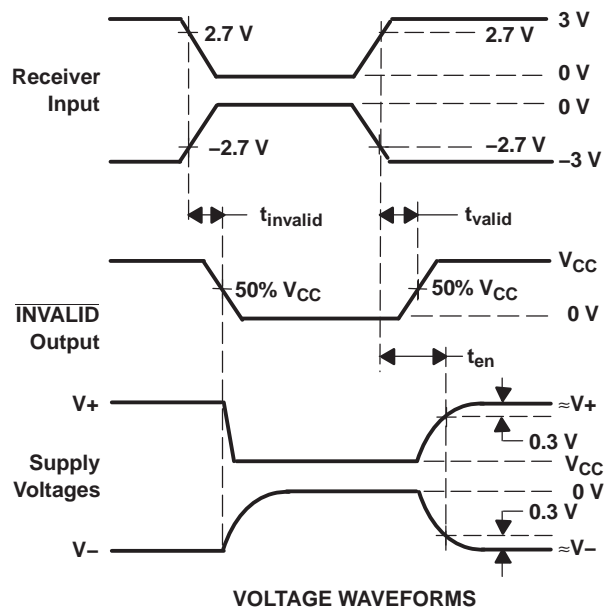
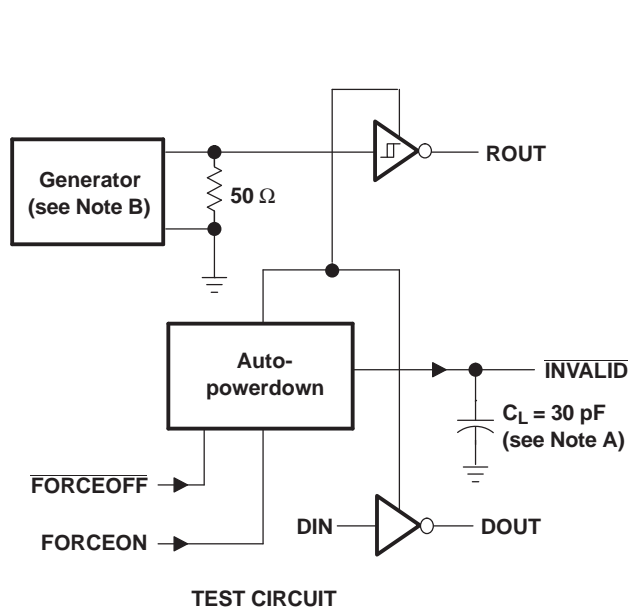
## PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. The pulse generator has the following characteristics:  $Z_O = 50\ \Omega$ , 50% duty cycle,  $t_r \leq 10\text{ ns}$ ,  $t_f \leq 10\text{ ns}$ .  
 C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

**Figure 4. Receiver Enable and Disable Times**

## PARAMETER MEASUREMENT INFORMATION



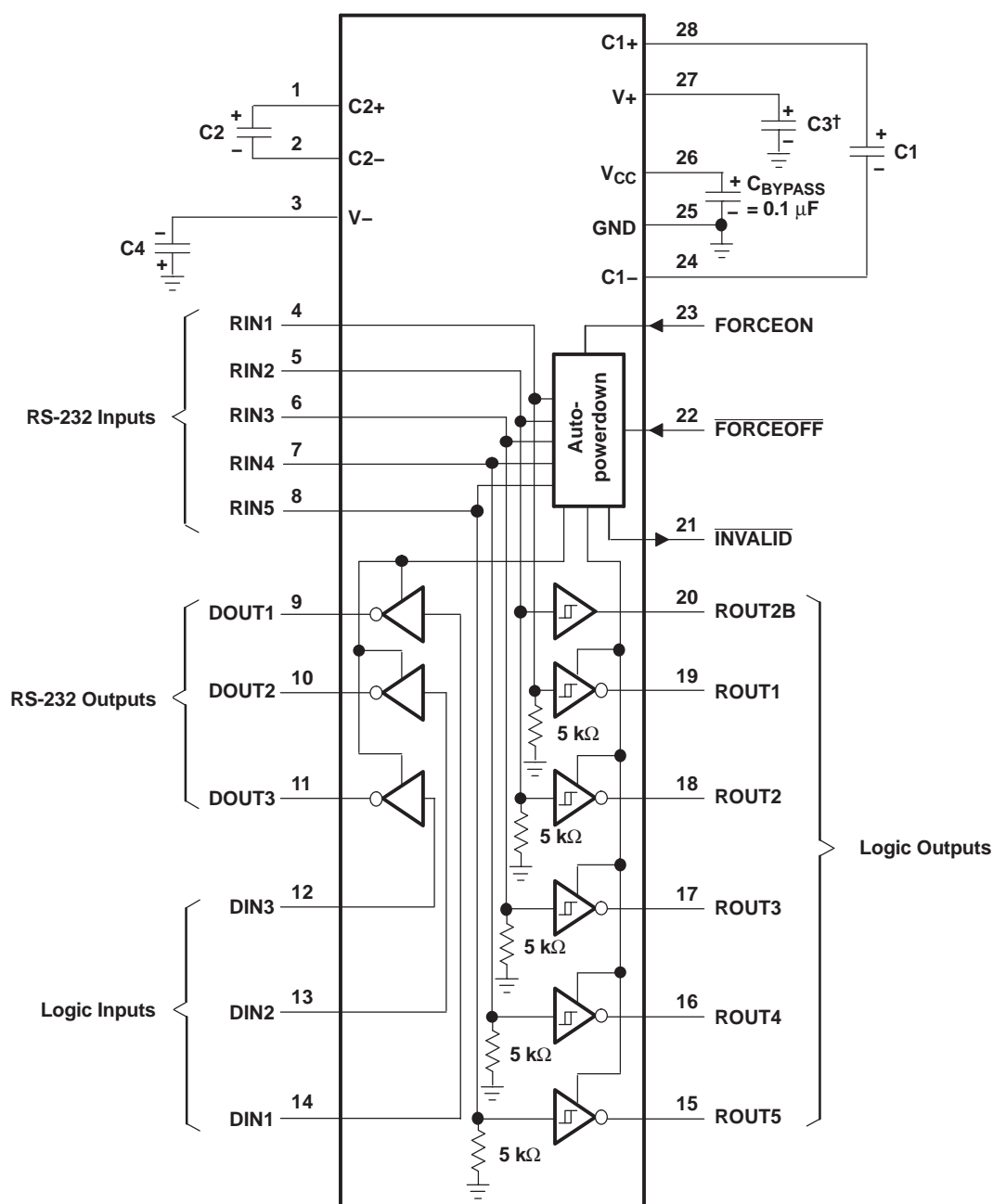
<sup>†</sup> Auto-powerdown disables drivers and reduces supply current to 1  $\mu\text{A}$ .

NOTES: A.  $C_L$  includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

Figure 5.  $\overline{\text{INVALID}}$  Propagation Delay Times and Supply Enabling Time

## APPLICATION INFORMATION



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

## APPLICATION INFORMATION

### ESD Protection

TI TRS3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of  $\pm 15$ -kV in all states: normal operation, shutdown, and powered down. The TRS3243E devices are designed to continue functioning properly after an ESD occurrence without any latchup.

The TRS3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

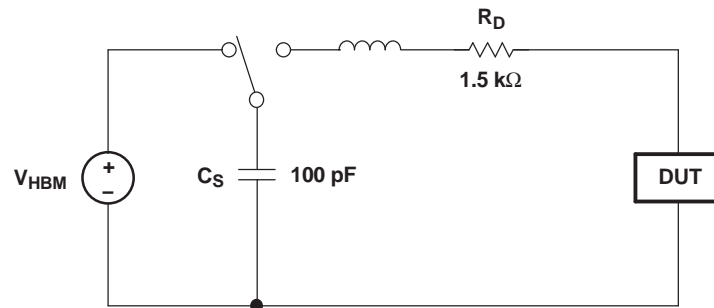
- $\pm 15$ -kV Human-Body Model (HBM)
- $\pm 15$ -kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- $\pm 8$ -kV IEC61000-4-2, Contact Discharge

### ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

### Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 7, while Figure 8 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5-k $\Omega$  resistor.



**Figure 7. HBM ESD Test Circuit**

## APPLICATION INFORMATION

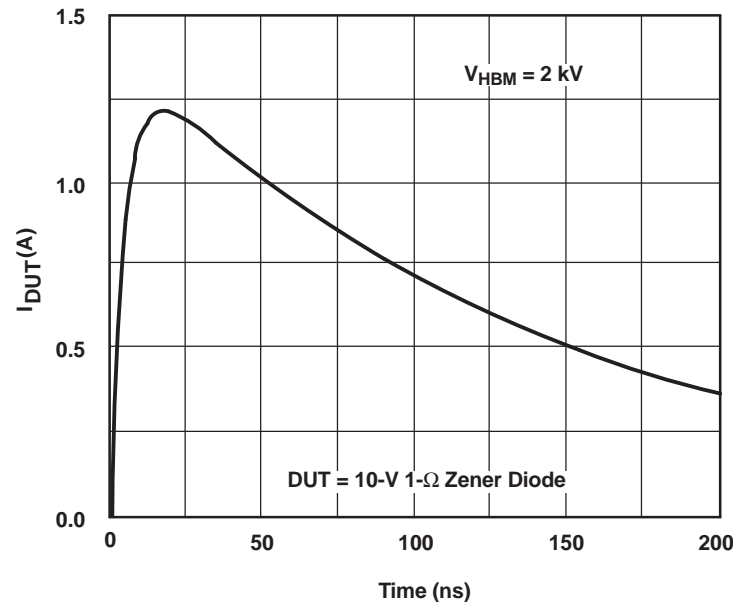


Figure 8. Typical HBM Current Waveform

### IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The TRS3243E is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

Figure 9 shows the IEC61000-4-2 model, and Figure 10 shows the current waveform for the corresponding  $\pm 8$ -kV contact-discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding  $\pm 15$ -kV (Level 4) air-gap discharge test involves approaching the DUT with an already energized probe.

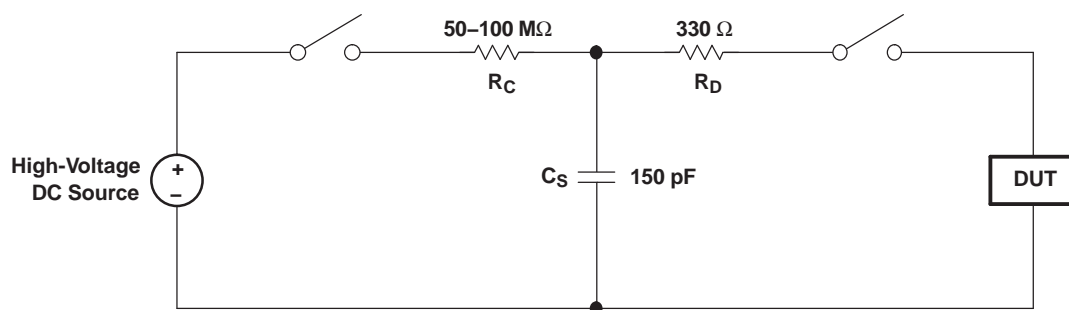
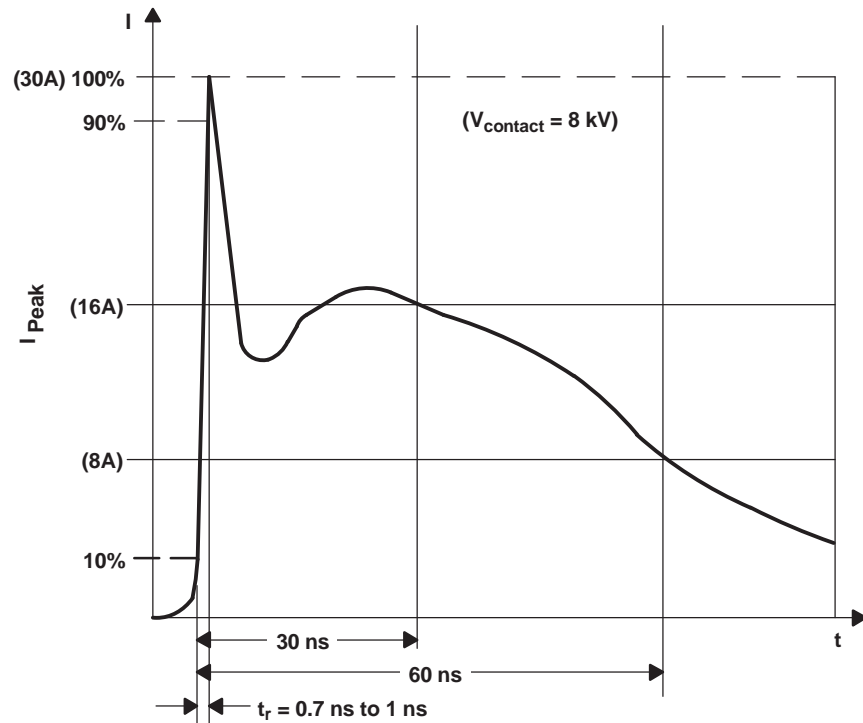


Figure 9. Simplified IEC61000-4-2 ESD Test Circuit

## APPLICATION INFORMATION



**Figure 10. Typical Current Waveform of IEC61000-4-2 ESD Generator**

### Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test is no longer as pertinent to the RS-232 pins.

## REVISION HISTORY

Changes from Revision B (July 2009) to Revision C	Page
• Deleted "VALID RIN RS-232 LEVEL" from INPUTS. ....	<a href="#">3</a>
• Deleted "ROUT2B is active" RECEIVER STATUS and combined ROUT outputs. ....	<a href="#">3</a>
• Added New Table "ROUT2B and <u>INVALID</u> Outputs" defining truth table for ROUT2B and INVALID outputs. ....	<a href="#">3</a>



## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3243ECDB	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	<a href="#">Samples</a>
TRS3243ECDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	<a href="#">Samples</a>
TRS3243ECDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	<a href="#">Samples</a>
TRS3243ECDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243EC	<a href="#">Samples</a>
TRS3243ECPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC	<a href="#">Samples</a>
TRS3243ECPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43EC	<a href="#">Samples</a>
TRS3243ECRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	RS43EC	<a href="#">Samples</a>
TRS3243EIDB	ACTIVE	SSOP	DB	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	<a href="#">Samples</a>
TRS3243EIDBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	<a href="#">Samples</a>
TRS3243EIDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	<a href="#">Samples</a>
TRS3243EIDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243EI	<a href="#">Samples</a>
TRS3243EIPW	ACTIVE	TSSOP	PW	28	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI	<a href="#">Samples</a>
TRS3243EIPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43EI	<a href="#">Samples</a>
TRS3243EIRHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI	<a href="#">Samples</a>
TRS3243EIRHBRG4	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	RS43EI	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3243ECDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243ECDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243ECPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3243ECRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRS3243EIDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243EIDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
TRS3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3243EIRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

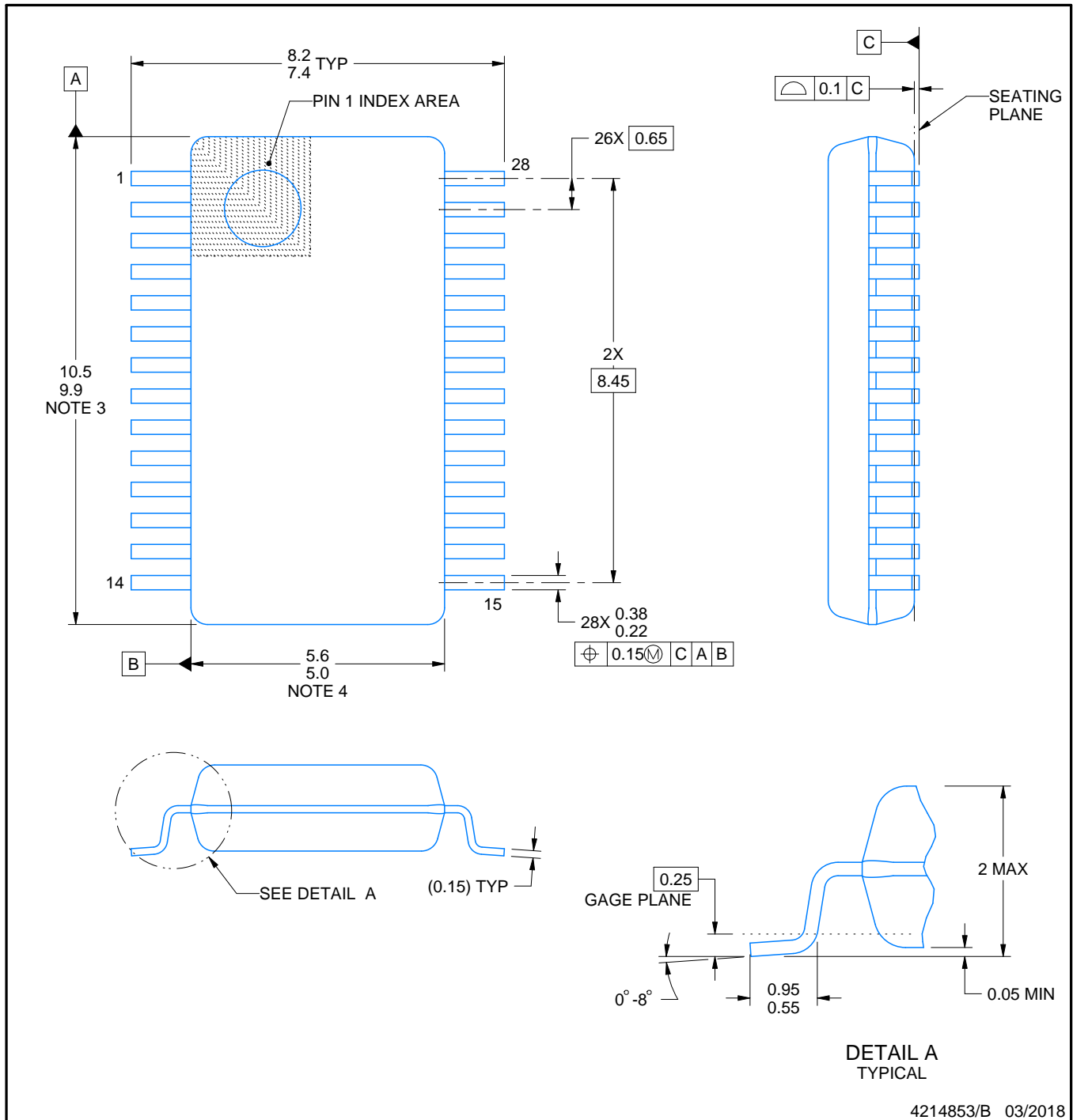
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3243ECDDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS3243ECDWR	SOIC	DW	28	1000	350.0	350.0	66.0
TRS3243ECPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
TRS3243ECRHBR	VQFN	RHB	32	3000	356.0	356.0	35.0
TRS3243EIDBR	SSOP	DB	28	2000	356.0	356.0	35.0
TRS3243EIDWR	SOIC	DW	28	1000	350.0	350.0	66.0
TRS3243EIPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
TRS3243EIRHBR	VQFN	RHB	32	3000	356.0	356.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TRS3243ECDB	DB	SSOP	28	50	530	10.5	4000	4.1
TRS3243ECDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
TRS3243ECPW	PW	TSSOP	28	50	530	10.2	3600	3.5
TRS3243ECPW	PW	TSSOP	28	50	530	10.2	3600	3.5
TRS3243EIDB	DB	SSOP	28	50	530	10.5	4000	4.1
TRS3243EIDW	DW	SOIC	28	20	506.98	12.7	4826	6.6
TRS3243EIPW	PW	TSSOP	28	50	530	10.2	3600	3.5
TRS3243EIPW	PW	TSSOP	28	50	530	10.2	3600	3.5



4214853/B 03/2018

## NOTES:

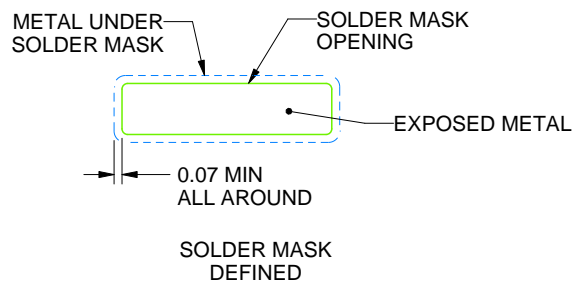
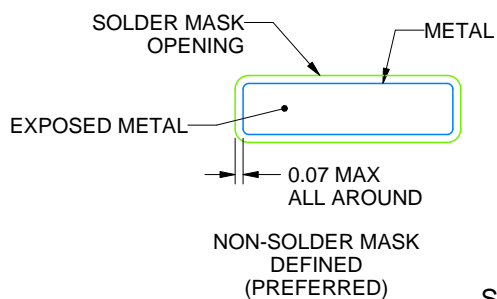
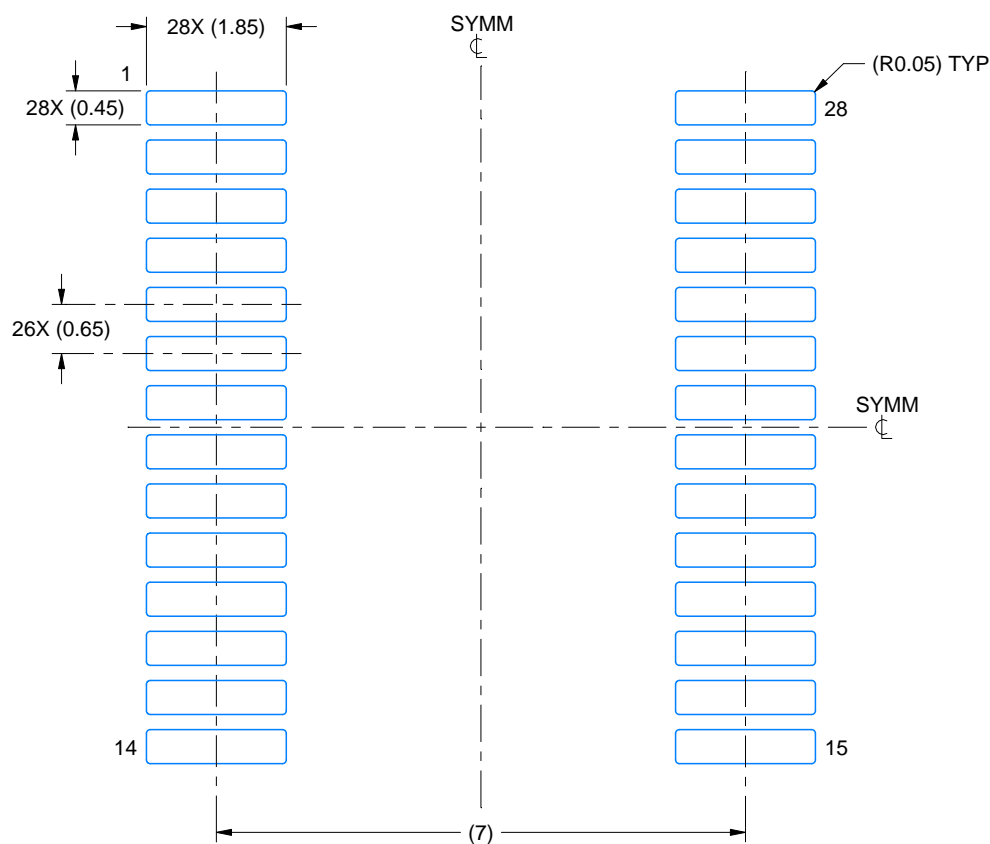
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



## SOLDER MASK DETAILS

4214853/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

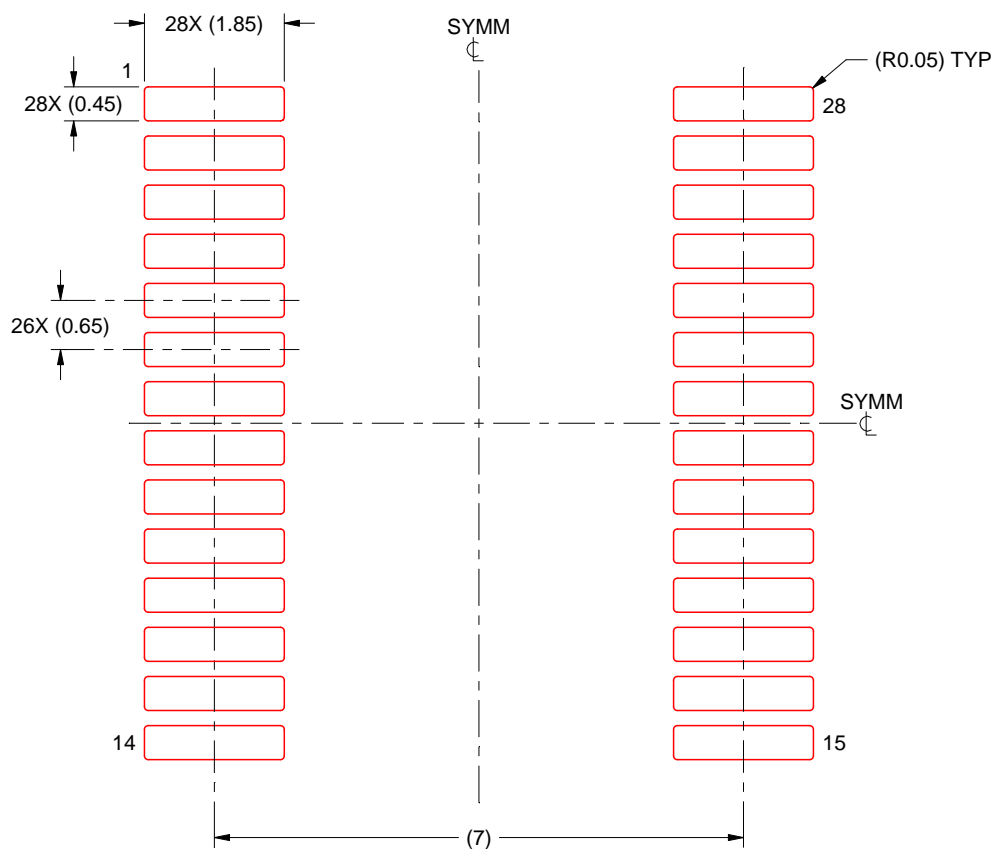
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214853/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A

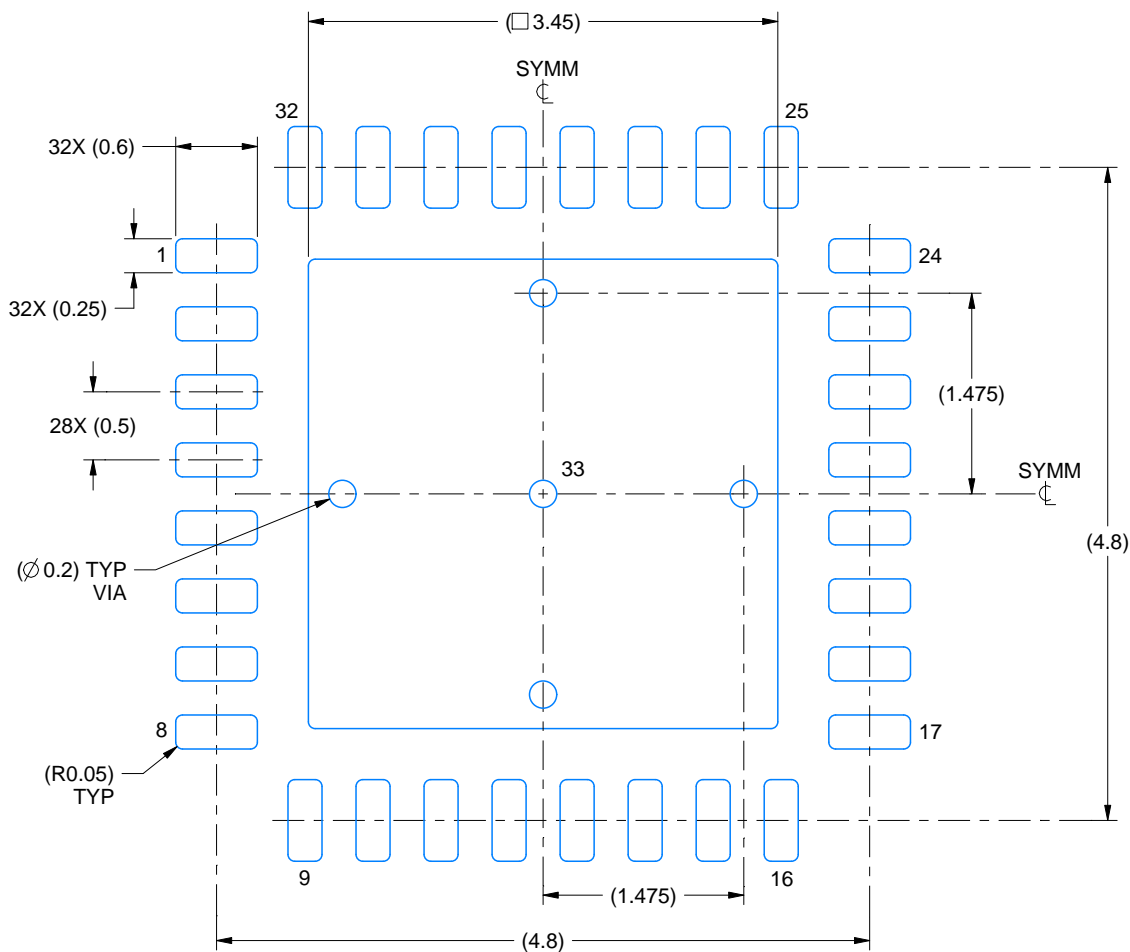
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

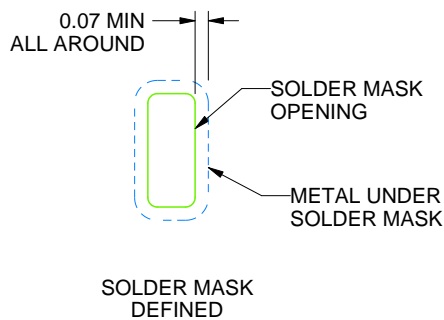
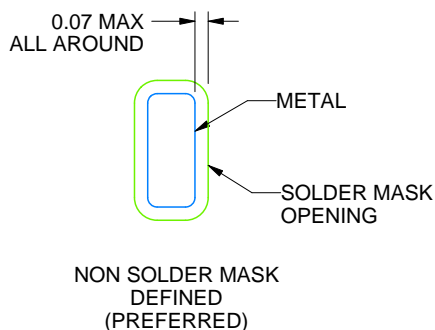
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

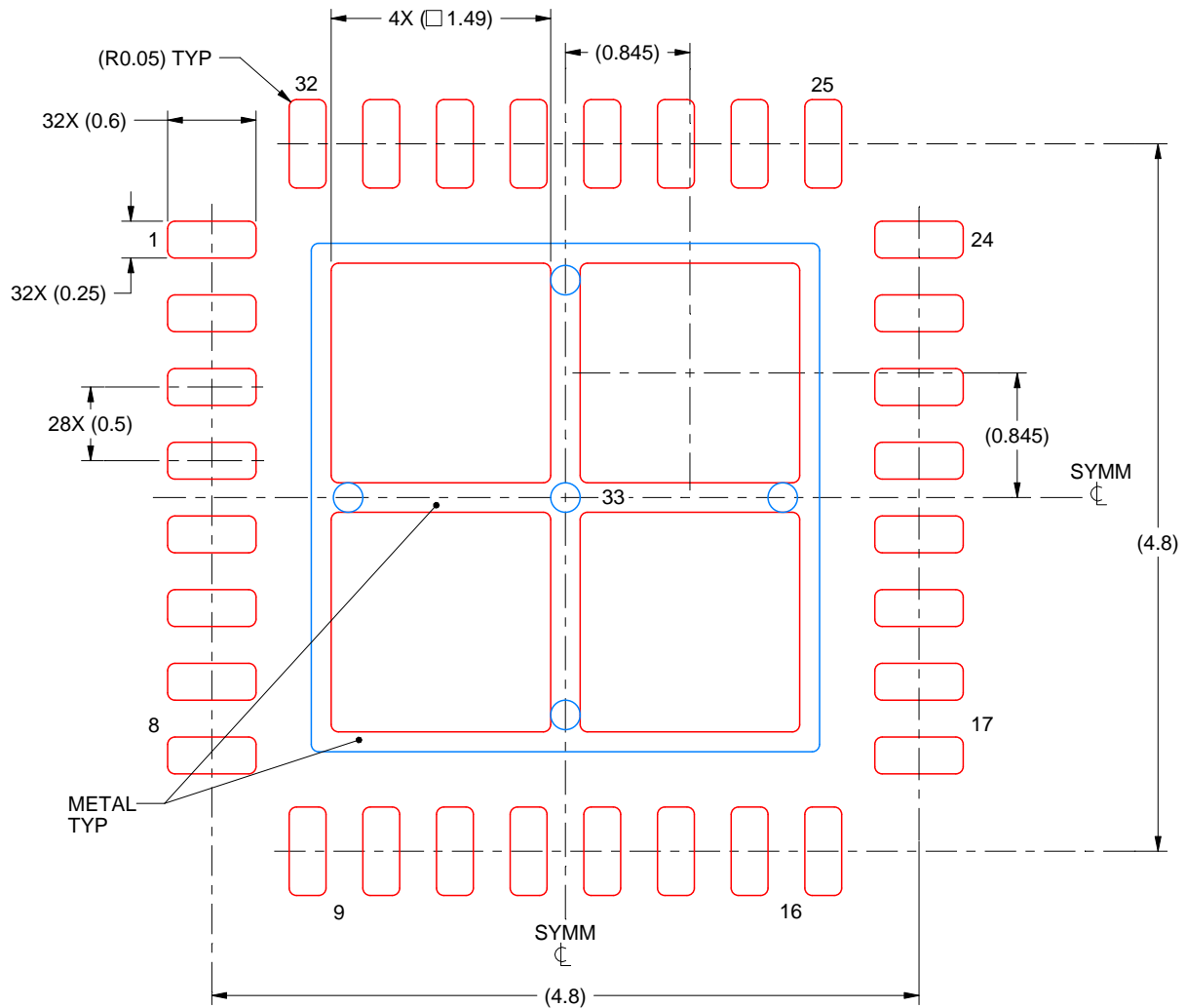
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

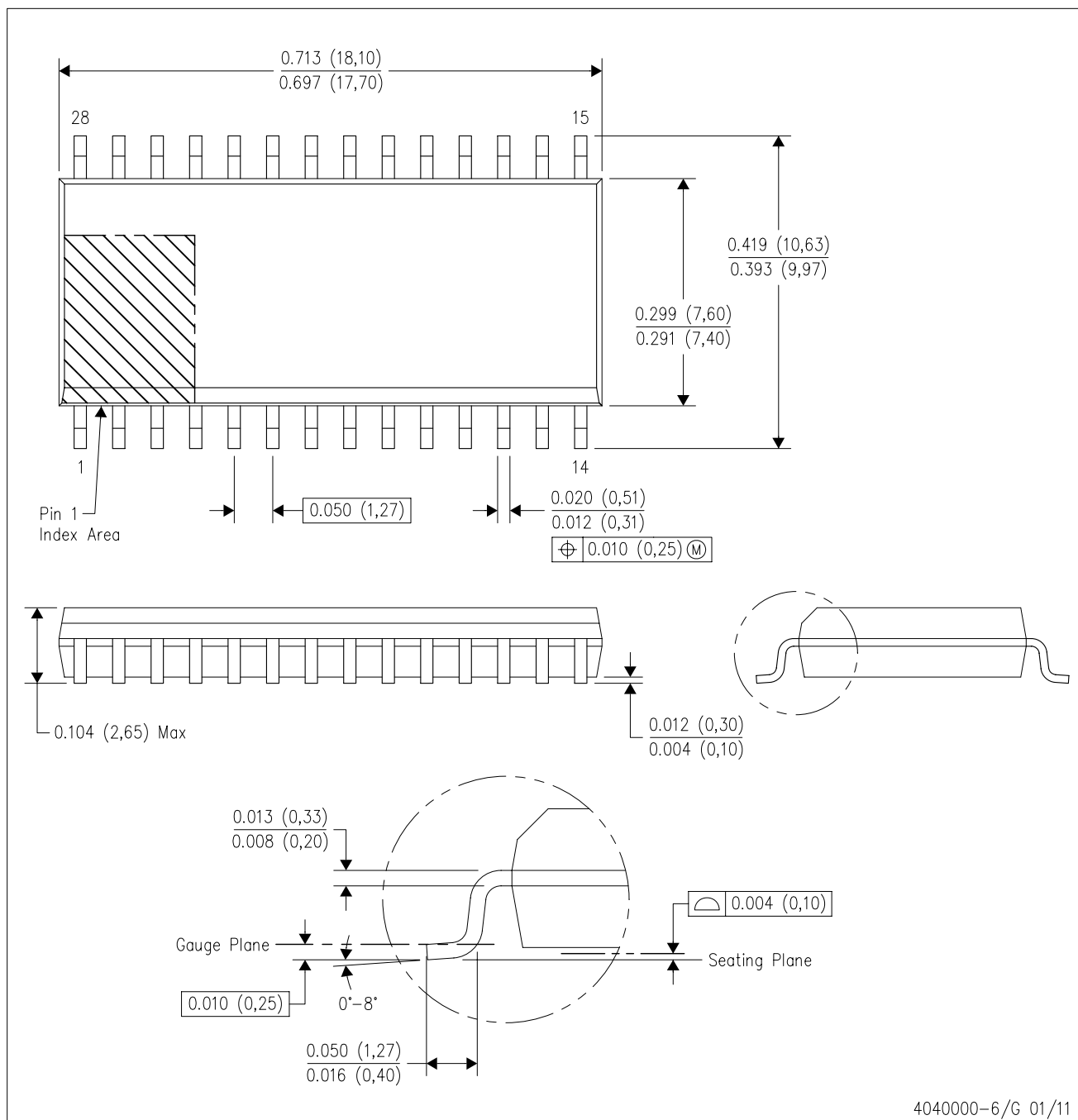
4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DW (R-PDSO-G28)

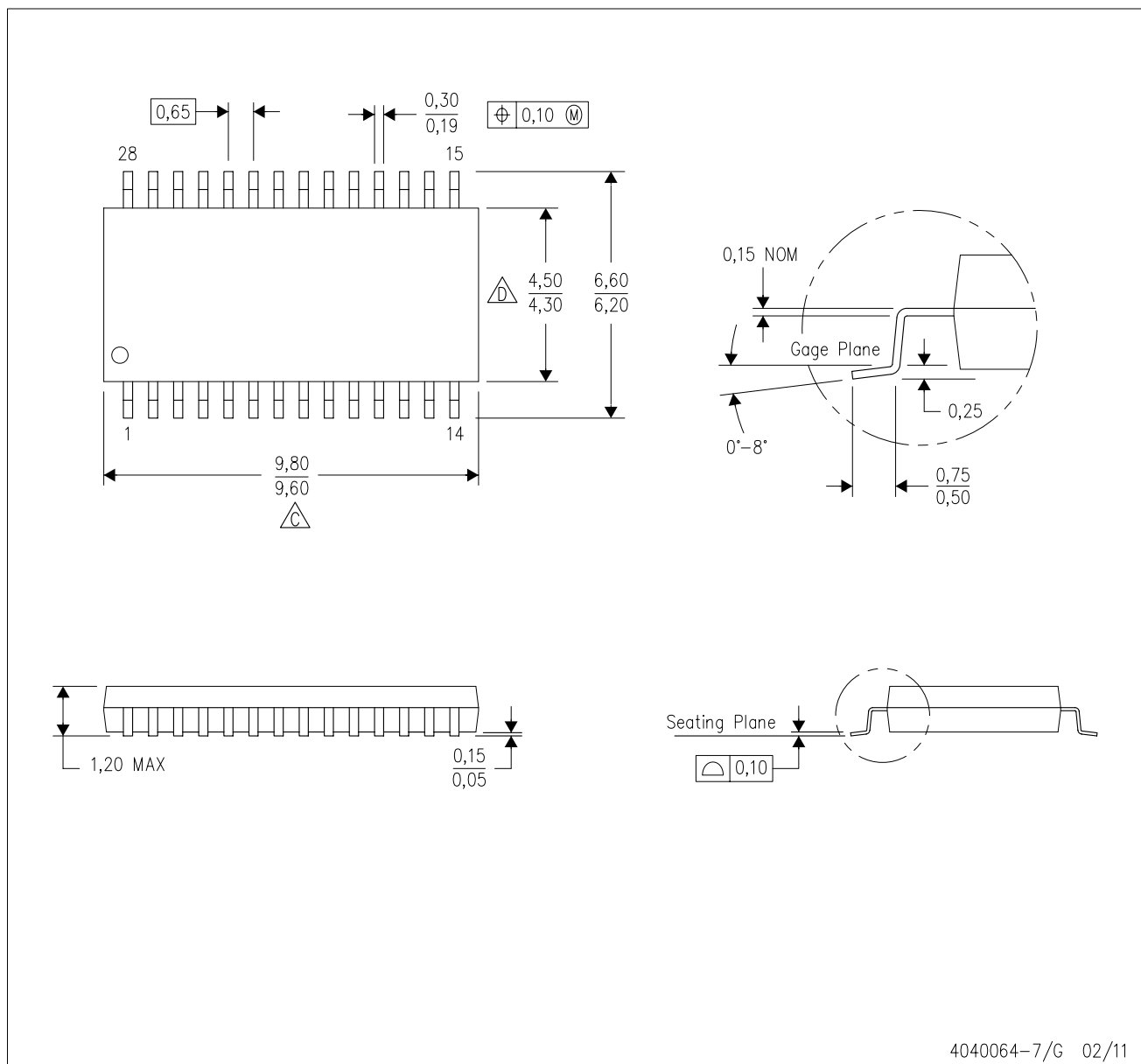
## PLASTIC SMALL OUTLINE



- NOTES: A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
D. Falls within JEDEC MS-013 variation AE.

PW (R-PDSO-G28)

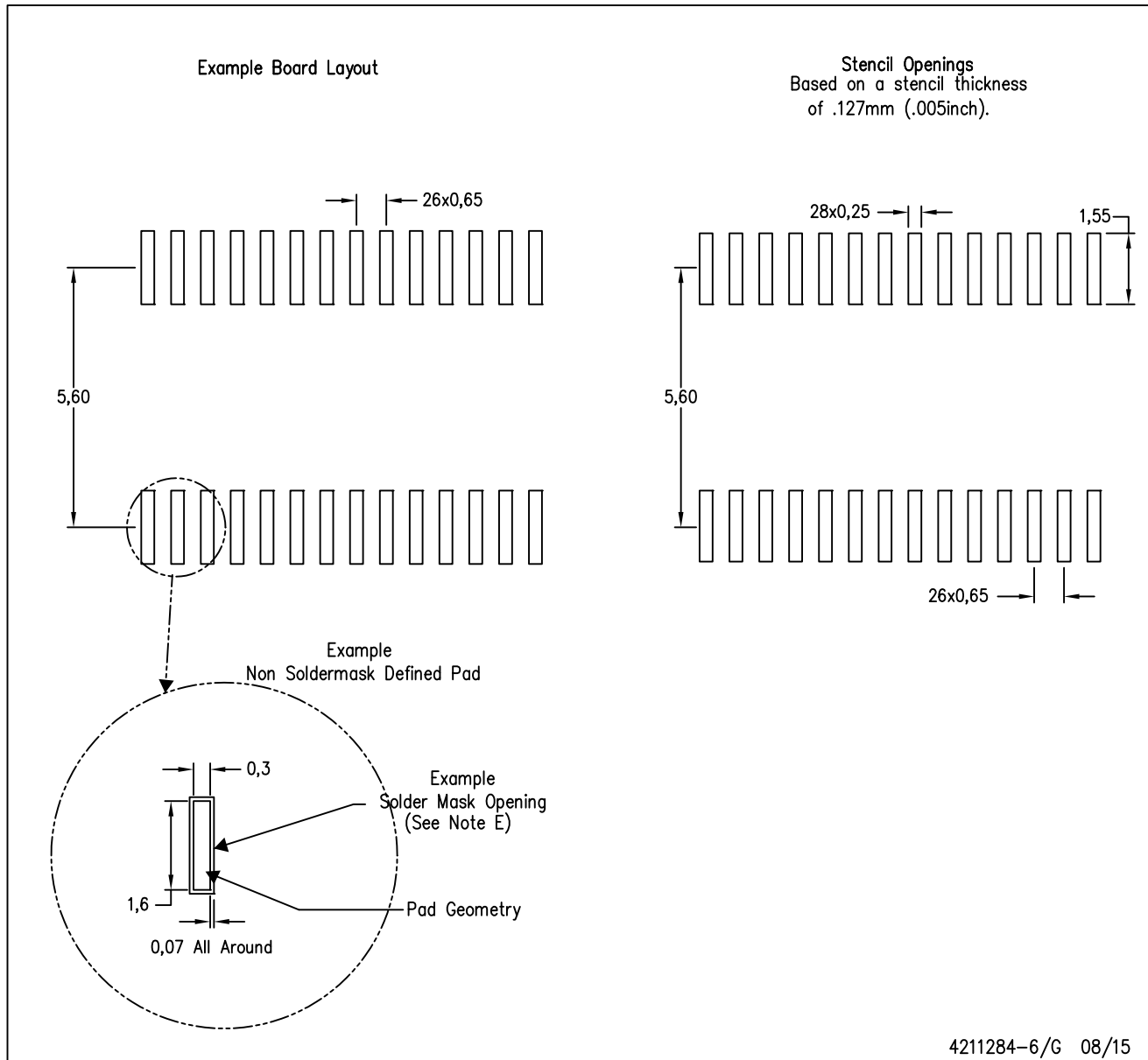
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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