TS5A3359 1Ω SP3T 双向模拟开关 5V/3.3V 单通道 3:1 多路复用器和多路解复用器

1 特性

- 断电模式隔离，V_{CC} = 0
- 指定的先断后合开关
- 低导通电阻 (1 Ω)
- 控制输入为 5.5V 耐压
- 低电荷注入 (5 pC V_{CC} = 1.8V)
- 出色的导通状态电阻匹配
- 低总谐波失真 (THD)
- 1.65V 至 5.5V 单电源运行
- 闩锁性能超过 100 mA，符合 JESD 78 II 类规范
- ESD 性能经测试符合 JESD 22 规范
  - 2000V 人体放电模型（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 手机
- PDA
- 便携式仪表
- 音频和视频信号路由
- 低电压数据采集系统
- 通信电路
- 调制解调器
- 硬盘
- 计算机外设
- 无线终端和外设

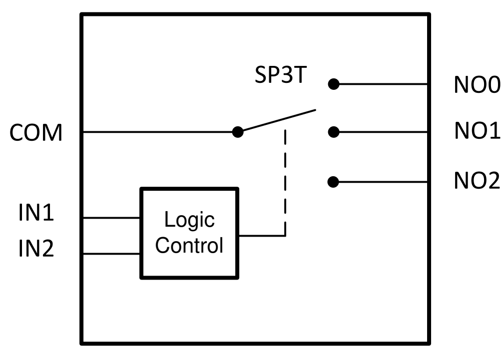
3 说明

TS5A3359 器件是一款工作电压范围为 1.65V 至 5.5V 的双向、单通道、单刀三掷 (SP3T) 模拟开关。TS5A3359 器件提供信号切换解决方案，同时保持出色的信号完整性，因此适用于各种市场中的广泛应用，包括个人电子产品、测试和测量设备以及便携式仪器。该器件拥有低导通电阻、出色的导通状态电阻匹配以及最小总谐波失真 (THD) 性能，可维持信号完整性。TS5A3359 器件还具有指定的先断后合特性，可防止信号在跨通道传输时出现失真。该器件能耗超低，可在 V_{CC} = 0 时提供隔离。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TS5A3359	US8 (8)	2.30mm × 2.00mm
	DSBGA (8)	1.25mm × 2.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (January 2016) to Revision F (December 2021) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式.......... 1
- 更新了*器件信息* 表中 DSBGA (8) 封装的封装尺寸.......... 1

Changes from Revision D (May 2015) to Revision E (January 2016) — **Page**

- Added T_J Junction Temperature to the *Absolute Maximum Ratings* 4
- Changed Input leakage current UNIT value From: µA To: nA in *Electrical Characteristics for 5-V Supply* 5

Changes from Revision C (June 2008) to Revision D (May 2015) — **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分.......... 1
- Changed YZP pinout numbering.......... 3

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5 Pin Configuration and Functions

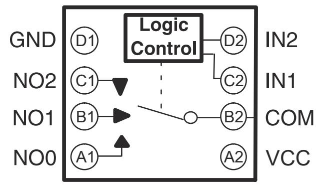

图 5-1. YZP Package 8-Pin DSBGA Bottom View

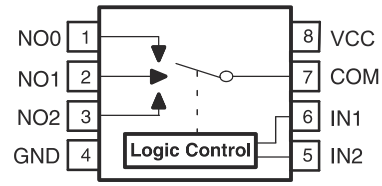

图 5-2. DCU Package 8-Pin US8 Top View

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DCU	YZP		
NO0	1	A1	I/O	Normally open
NO1	2	B1	I/O	Normally open
NO2	3	C1	I/O	Normally open
GND	4	D1	—	Ground
IN2	5	D2	I	Digital control to connect COM to NO
IN1	6	C2	I	Digital control to connect COM to NO
COM	7	B2	I/O	Common
VCC	8	A2	—	Power supply

(1) I = input, O = output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[(3)]		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage[(3)] [(4)] [(5)]		–0.5	V_{CC} + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0	–50		mA
I_{NO} I_{COM}	On-state switch current	V_{NO}, V_{COM} = 0 to V_{CC}	–200	200	mA
			–400	400	
V_I	Digital input voltage[(3)] [(4)]		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5-V maximum.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Analog voltage	1.65	5.5	V
V_{NO} V_{COM}		0	V_{CC}	V
V_I	Digital input voltage	0	V_{CC}	V

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6.4 Thermal Information

THERMAL METRIC[(1)]		TS5A3359 DCU (US8) 8 PINS	TS5A3359 YZP (DSBGA) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.2	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76.2	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	82.9	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	82.5	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)[(1)]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
Peak ON resistance	r_{peak}	$0 \leqslant (V_{NO}) \leqslant V_{CC}$, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C	4.5 V		0.8	1.1	Ω
				Full				1.5	
ON-state resistance	r_{on}	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C	4.5 V		0.7	0.9	Ω
				Full				1.1	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C	4.5 V		0.1	0.1	Ω
				Full				0.1	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leqslant (V_{NO}) \leqslant V_{CC}$, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C	4.5 V		0.15		Ω
		V_{NO} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C			0.1	0.25	
				Full				0.25	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V or 4.5 V, V_{COM} = 1 V to 4.5 V,	Switch OFF, See 图 7-2	25°C	5.5 V	–20	5	20	nA
				Full		–150		150	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,	Switch OFF, See 图 7-2	25°C	0 V	–1	0.8	1	µA
				Full		–25		25	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V or 4.5 V, V_{COM} = Open,	Switch ON, See 图 7-2	25°C	5.5 V	–30	5	30	nA
				Full		–220		220	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 4.5 V or 1 V, V_{COM} = 1 V or 4.5 V,	Switch OFF, See 图 7-2	25°C	5.5 V	–25	8	25	nA
				Full		–250		250	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 5.5 V, V_{NO} = 5.5 V to 0,	Switch OFF, See 图 7-2	25°C	0 V	–8	0.1	8	µA
				Full		–50		50	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 1 V or 4.5 V,	Switch ON, See 图 7-2	25°C	5.5 V	–30	5	30	nA
				Full		–220		220	
DIGITAL CONTROL INPUTS (IN1, IN2)[(2)]									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V

6.5 Electrical Characteristics for 5-V Supply (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)[(1)]

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0	25°C	5.5 V	–2		2	nA
			Full		–20		20	

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6.5 Electrical Characteristics for 5-V Supply (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turnon time	t_{ON}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-5	25°C	5 V	1	2.5	21	ns
				Full	4.5 V to 5.5 V	1		23.5	
Turnoff time	t_{OFF}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-5	25°C	5 V	1	6	10.5	ns
				Full	4.5 V to 5.5 V	1		12	
Break-before-make time	t_{BBM}	$V_{NO} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-6	25°C	5 V	0.5	8.5	18	ns
				Full	4.5 V to 5.5 V	0.5		23	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See 图 7-10	25°C	5 V		20		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_{CC}$ or GND, Switch OFF,	See 图 7-4	25°C	5 V		18		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND, Switch OFF,	See 图 7-4	25°C	2.5 V		54		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_{CC}$ or GND, Switch ON,	See 图 7-4	25°C	5 V		78		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$or GND, Switch ON,	See 图 7-4	25°C	5 V		78		pF
Digital input capacitance	C_I	$V_I = V_{CC}$ or GND,	See 图 7-4	25°C	5 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See 图 7-7	25°C	5 V		75		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz ,	Switch OFF, See 图 7-8	25°C	5 V		–64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz ,	Switch ON, See 图 7-9	25°C	5 V		–64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See 图 7-11	25°C	5 V		0.005%		
SUPPLY									
Positive supply current	I_{CC}	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	5.5 V		16	50	nA
				Full				1200	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.6 Electrical Characteristics for 3.3-V Supply

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C	3 V		1.3	1.6	Ω
				Full				2	
ON-state resistance	r_{on}	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C	3 V		1.2	1.6	Ω
				Full				1.8	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C	3 V		0.1	0.15	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C	3 V		0.2		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See 图 7-1	25°C			0.2	0.35	
				Full				0.35	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 1 V or 3 V, V_{COM} = 1 V to 3 V,	Switch OFF, See 图 7-2	25°C	3.6 V	–15	3	15	nA
				Full		–30		30	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,	Switch OFF, See 图 7-2	25°C	0 V	–1	0.2	1	µA
				Full		–10		10	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 1 V or 3 V, V_{COM} = Open,	Switch ON, See 图 7-2	25°C	3.6 V	–15	3	15	nA
				Full		–40		40	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 0 V to 3.6 V, V_{COM} = 1 V or V_{NO} = 3.6 V to 0, V_{COM} = 3 V,	Switch OFF, See 图 7-2	25°C	3.6 V	–15	3	15	nA
				Full		–75		75	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NO} = 3.6 V to 0,	Switch OFF, See 图 7-2	25°C	0 V	–1	0.2	1	µA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 1 V or 3 V,	Switch ON, See 图 7-2	25°C	3.6 V	–15	4	15	nA
				Full		–40		40	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–2		2	nA
				Full		–20		20	

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6.6 Electrical Characteristics for 3.3-V Supply (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turnon time	t_{ON}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-5	25°C	3.3 V	1	16	30.5	ns
				Full	3 V to 3.6 V	1		34	
Turnoff time	t_{OFF}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-5	25°C	3.3 V	1	6	11.5	ns
				Full	3 V to 3.6 V	1		12.5	
Break-before-make time	t_{BBM}	$V_{NO} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-6	25°C	3.3 V	0.5	13	26	ns
				Full	3 V to 3.6 V	0.5		30	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See 图 7-10	25°C	3.3 V		12		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_{CC}$ or GND, Switch OFF,	See 图 7-4	25°C	3.3 V		18		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND, Switch OFF,	See 图 7-4	25°C	3.3 V		55		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_{CC}$ or GND, Switch ON,	See 图 7-4	25°C	3.3 V		78		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND, Switch ON,	See 图 7-4	25°C	3.3 V		78		pF
Digital input capacitance	C_I	$V_I = V_{CC}$ or GND,	See 图 7-4	25°C	3.3 V		2.5		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See 图 7-7	25°C	3.3 V		73		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See 图 7-8	25°C	3.3 V		–64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See 图 7-9	25°C	3.3 V		–64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See 图 7-11	25°C	3.3 V		0.01%		
SUPPLY									
Positive supply current	I_{CC}	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	3.6 V		2	20	nA
				Full				350	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

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6.7 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
Peak ON resistance	r_{peak}	$0 \leq (V_{NO}) \leq V_{CC}$, I_{COM} = –8 mA,	Switch ON, See 图 7-1	25°C	2.3 V		1.8	2.5	Ω
				Full				2.7	
ON-state resistance	r_{on}	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See 图 7-1	25°C	2.3 V		1.5	2	Ω
				Full				2.4	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See 图 7-1	25°C	2.3 V			0.2	Ω
				Full				0.2	
ON-state resistance flatness	$r_{on(flat)}$	$0 \leq (V_{NO}) \leq V_{CC}$, I_{COM} = –8 mA,	Switch ON, See 图 7-1	25°C	2.3 V		0.6		Ω
		V_{NO} = 0.8 V, 1.8 V I_{COM} = –8 mA,	Switch ON, See 图 7-1	25°C			0.6	1	
				Full				1	
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} = 0.5 V or 2.3 V, V_{COM} = 0.5 V to 2.3 V,	Switch OFF, See 图 7-2	25°C	2.7 V	–15	3	15	nA
				Full		–30		30	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,	Switch OFF, See 图 7-2	25°C	0 V	–1	0.1	1	μA
				Full		–10		10	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} = 0.5 V or 2.3 V, V_{COM} = Open,	Switch ON, See 图 7-2	25°C	2.7 V	–15	3	15	nA
				Full		–35		35	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 0.3 V to 2.3 V, V_{COM} = 0.5 V or 2.3 V,	Switch OFF, See 图 7-2	25°C	2.7 V	–15	3	15	nA
				Full		–60		60	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 2.7 V, V_{NO} = 2.7 V to 0,	Switch OFF, See 图 7-2	25°C	0 V	–1	0.1	1	μA
				Full		–10		10	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0.5 V or 2.2 V,	Switch ON, See 图 7-2	25°C	2.7 V	–15	3.5	15	nA
				Full		–40		40	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	1		1	nA
				Full		10		10	

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6.7 Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turnon time	t_{ON}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-5	25°C	2.5 V	2	4.5	43	ns
				Full	2.3 V to 2.7 V	2		47.5	
Turnoff time	t_{OFF}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-5	25°C	2.5 V	2	8.5	11	ns
				Full	2.3 V to 2.7 V	2		12.5	
Break-before-make time	t_{BBM}	$V_{NO} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See 图 7-6	25°C	2.5 V	0.5	18.5	38.5	ns
				Full	2.3 V to 2.7 V	0.5		43	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See 图 7-10	25°C	2.5 V		8		pC
NO OFF capacitance	$C_{NO(OFF)}$	$V_{NO} = V_{CC}$ or GND, Switch OFF,	See 图 7-4	25°C	2.5 V		18.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND, Switch OFF,	See 图 7-4	25°C	2.5 V		55		pF
NO ON capacitance	$C_{NO(ON)}$	$V_{NO} = V_{CC}$ or GND, Switch ON,	See 图 7-4	25°C	2.5 V		78		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND, Switch ON,	See 图 7-4	25°C	2.5 V		78		pF
Digital input capacitance	C_I	$V_I = V_{CC}$ or GND,	See 图 7-4	25°C	2.5 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See 图 7-7	25°C	2.5 V		73		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See 图 7-8	25°C	2.5 V		–64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See 图 7-9	25°C	2.5 V		–64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See 图 7-11	25°C	2.5 V		0.03%		
SUPPLY									
Positive supply current	I_{CC}	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	2.7 V		1	10	nA
				Full				250	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

6.8 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
Analog signal range	V_{COM}, V_{NO}					0		V_{CC}	V
Peak ON resistance	r_{peak}	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –2 mA,	Switch ON, See 图 7-1	25°C	1.65 V		5		Ω
				Full				30	
ON-state resistance	r_{on}	V_{NO} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See 图 7-1	25°C	1.65 V		2	2.5	Ω
				Full				3.5	
ON-state resistance match between channels	Δr_{on}	V_{NO} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See 图 7-1	25°C	1.65 V		0.15	0.4	Ω
				Full				0.4	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ (V_{NO}) ≤ V_{CC}, I_{COM} = –2 mA,	Switch ON, See 图 7-1	25°C	1.65 V		5		Ω
		V_{NO} = 0.6 V, 1.5 V I_{COM} = –2 mA,	Switch ON, See 图 7-1	25°C			4.5		
				Full			5		
NO OFF leakage current	$I_{NO(OFF)}$	V_{NO} =0.3 V or 1.65 V, V_{COM} = 0.3 V to 1.65 V,	Switch OFF, See 图 7-2	25°C	1.95 V	–15	3	15	nA
				Full		–30		30	
	$I_{NO(PWROFF)}$	V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,	Switch OFF, See 图 7-2	25°C	0 V	–1	0.1	1	µA
				Full		–15		15	
NO ON leakage current	$I_{NO(ON)}$	V_{NO} =0.3 V or 1.65 V, V_{COM} = Open,	Switch ON, See 图 7-2	25°C	1.95 V	–15	3	15	nA
				Full		–30		30	
COM OFF leakage current	$I_{COM(OFF)}$	V_{NO} = 0.3 V to 1.65 V, V_{COM} =0.3 V or 1.65 V,	Switch OFF, See 图 7-2	25°C	1.95 V	–15	3	15	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 1.95 V, V_{NO} = 1.95 V to 0,	Switch OFF, See 图 7-2	25°C	0 V	–1	0.1	1	µA
				Full		–10		10	
COM ON leakage current	$I_{COM(ON)}$	V_{NO} = Open, V_{COM} = 0.3 V or 1.65 V,	Switch ON, See 图 7-2	25°C	1.95 V	–15	3	15	nA
				Full		–30		30	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	–2		2	nA
				Full		–20		20	

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6.8 Electrical Characteristics for 1.8-V Supply (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = – 40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
DYNAMIC									
Turnon time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See 图 7-5	25°C	1.8 V	3	38.5	85	ns
				Full	1.65 V to 1.95 V	3		90	
Turnoff time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See 图 7-5	25°C	1.8 V	2	8.5	16	ns
				Full	1.65 V to 1.95 V	2		18	
Break-before-make time	t_{BBM}	V_{NO} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See 图 7-6	25°C	1.8 V	1	33	75	ns
				Full	1.65 V to 1.95 V	1		80	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See 图 7-10	25°C	1.8 V		5		pC
NO OFF capacitance	$C_{NO(OFF)}$	V_{NO} = V_{CC} or GND, Switch OFF,	See 图 7-4	25°C	1.8 V		18.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND, Switch OFF,	See 图 7-4	25°C	1.8 V		55		pF
NO ON capacitance	$C_{NO(ON)}$	V_{NO} = V_{CC} or GND, Switch ON,	See 图 7-4	25°C	1.8 V		78		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND, Switch ON,	See 图 7-4	25°C	1.8 V		78		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See 图 7-4	25°C	1.8 V		3		pF
Bandwidth	BW	R_L = 50 Ω, Switch ON,	See 图 7-7	25°C	1.8 V		73		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 M Hz ,	Switch OFF, See 图 7-8	25°C	1.8 V		– 64		dB
Crosstalk	X_{TALK}	R_L = 50 Ω, f = 1 MHz,	Switch ON, See 图 7-9	25°C	1.8 V		– 64		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See 图 7-11	25°C	1.8 V		0.08%		
SUPPLY									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	1.95 V		1		nA
				Full				200	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

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6.9 Typical Characteristics

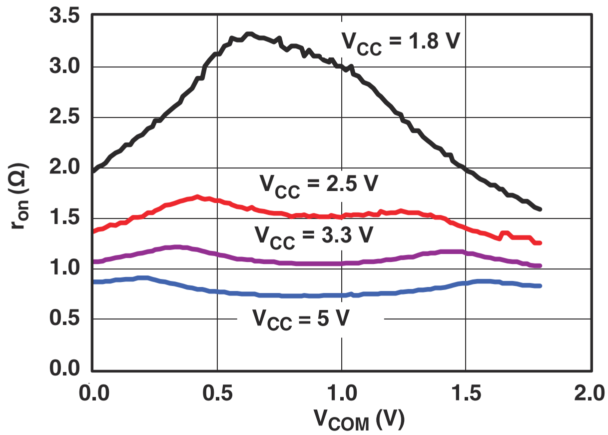

图 6-1. R_{on} vs V_{COM}

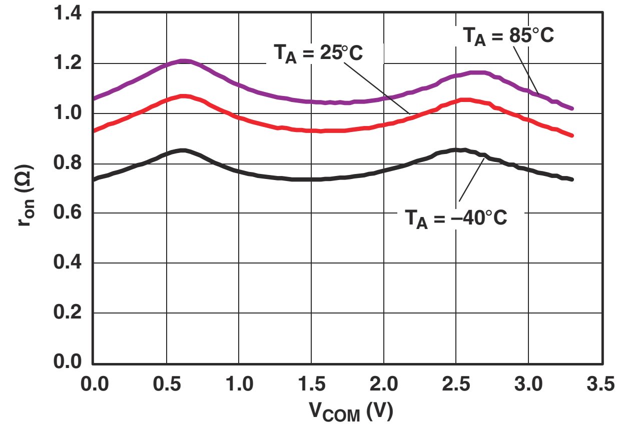

图 6-2. R_{on} vs V_{COM} Over Temperature (V_{CC} = 3.3 V)

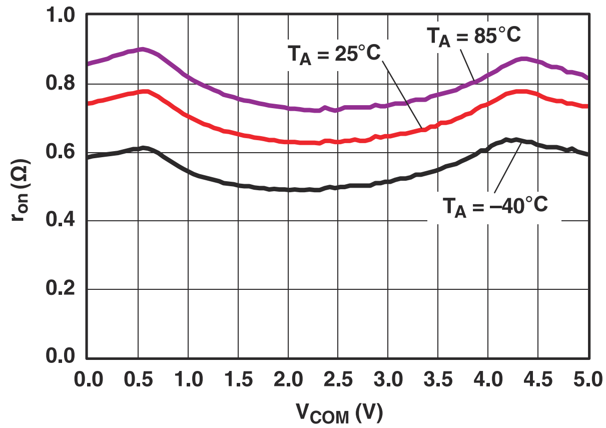

图 6-3. R_{on} vs V_{COM} Over Temperature(V_{CC} = 5 V)

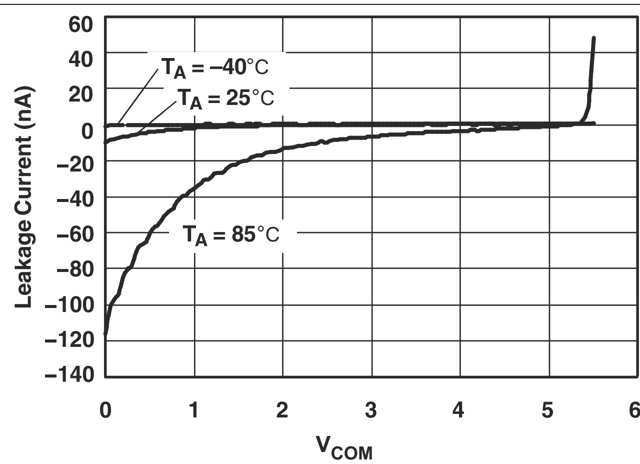

图 6-4. $I_{COM(OFF)}$Leakage Current vs V_{COM} Over Temperature (V_{CC} = 5 V)

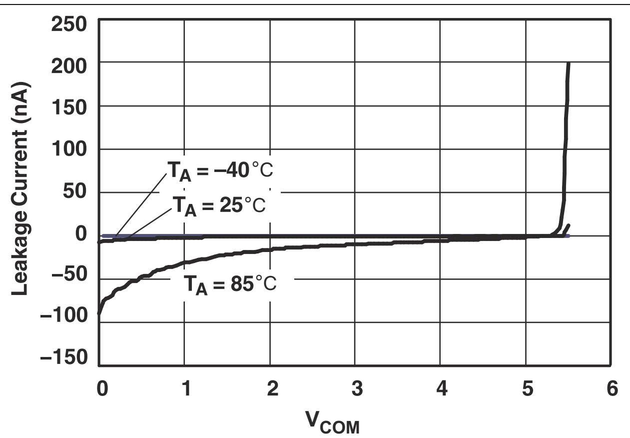

图 6-5. $I_{NO(OFF)}$Leakage Current vs V_{COM} Over Temperature (V_{CC} = 5 V)

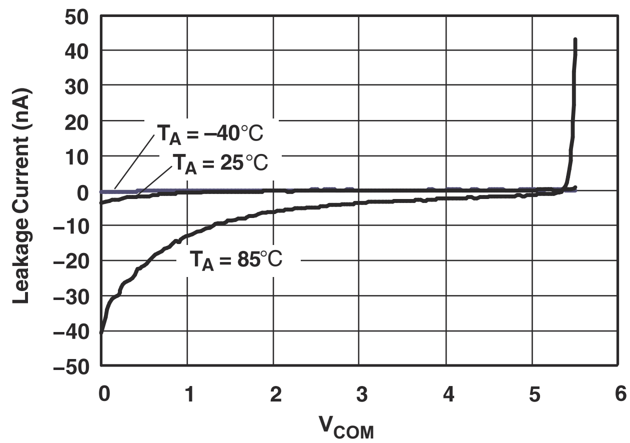

图 6-6. $I_{COM(ON)}$Leakage Current vs V_{COM} Over Temperature (V_{CC} = 5 V)

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6.9 Typical Characteristics (continued)

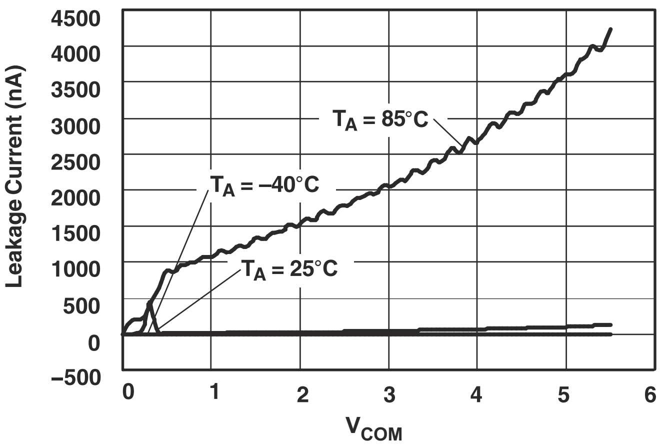

图 6-7. $I_{COM(PWROFF)}$ Leakage Current vs V_{COM} Over Temperature (V_{CC} = 0 V)

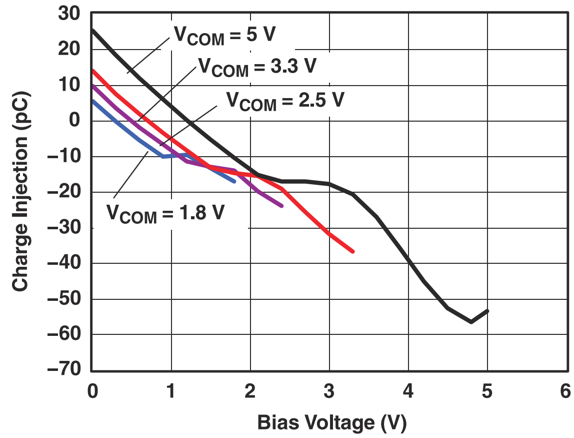

图 6-8. Charge Injection (Q_C) vs V_{COM}

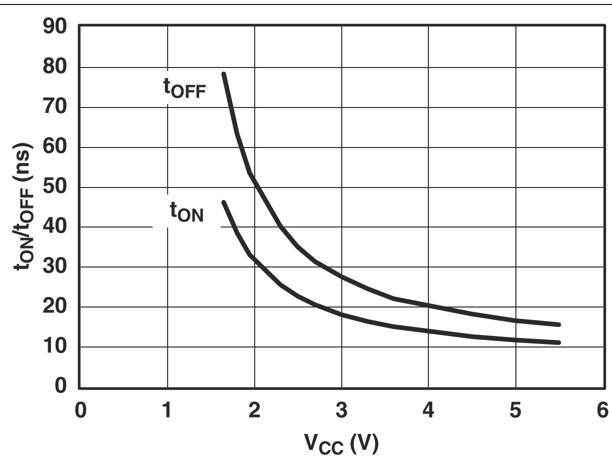

图 6-9. t_{ON} and t_{OFF} vs Supply Voltage

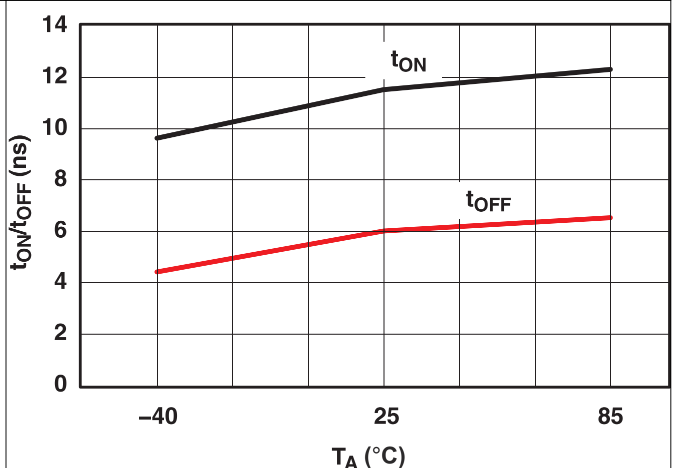

图 6-10. T_{ON} and T_{OFF} vs Temperature

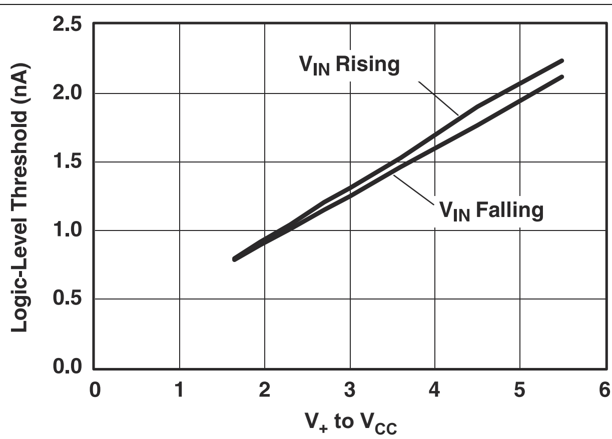

图 6-11. Logic-Level Threshold vs V_{CC}

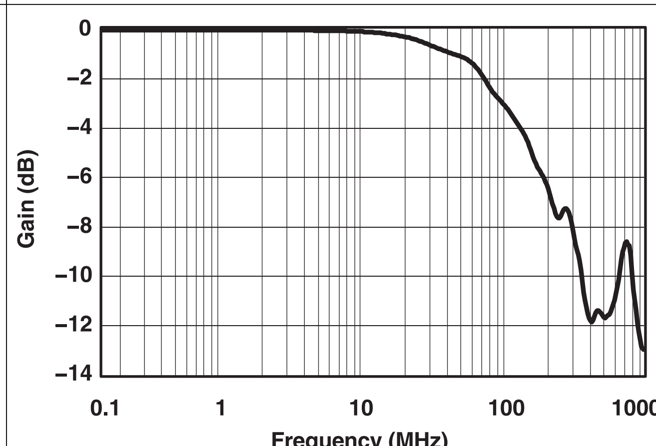

图 6-12. Bandwidth (V_{CC} = 5 V)

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6.9 Typical Characteristics (continued)

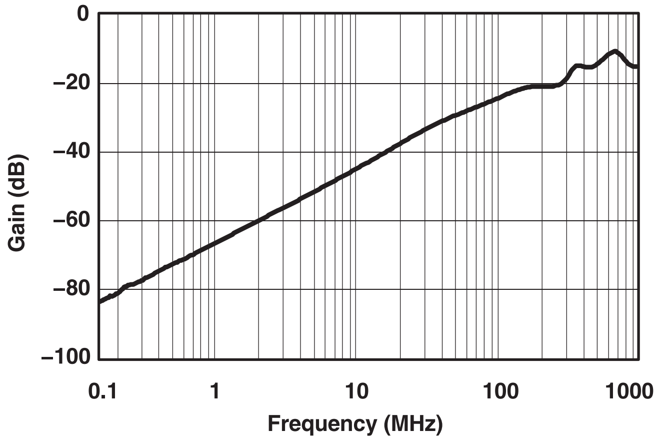

图 6-13. Off Isolation (V_{CC} = 5 V)

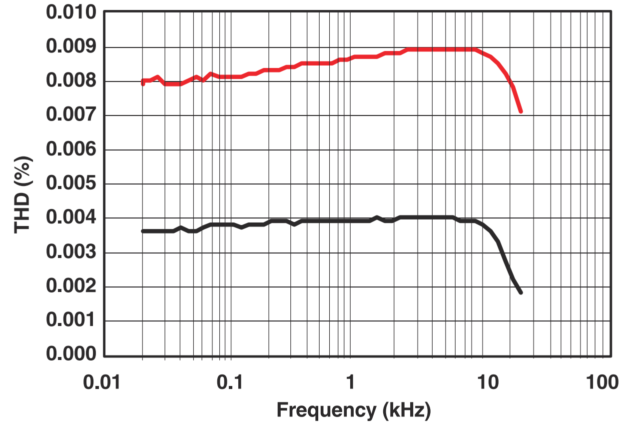

图 6-14. Total Harmonic Distortion vs Frequency (V_{CC} = 5 V)

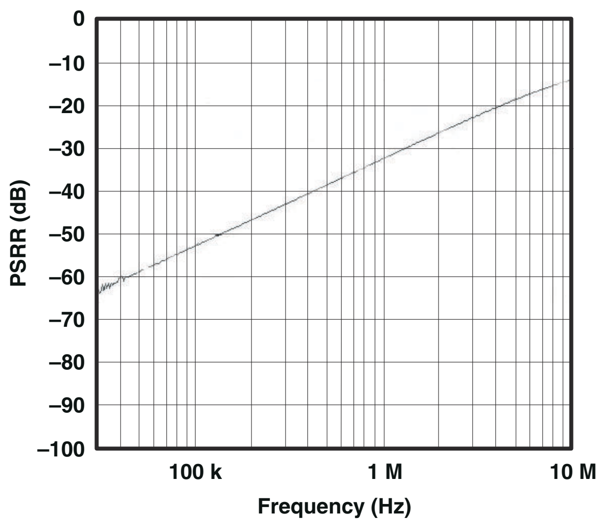

图 6-15. Com Port to No2 PSRR, In1 = V_{CC}, In2 = V_{CC} (V_{CC} = 5 V)

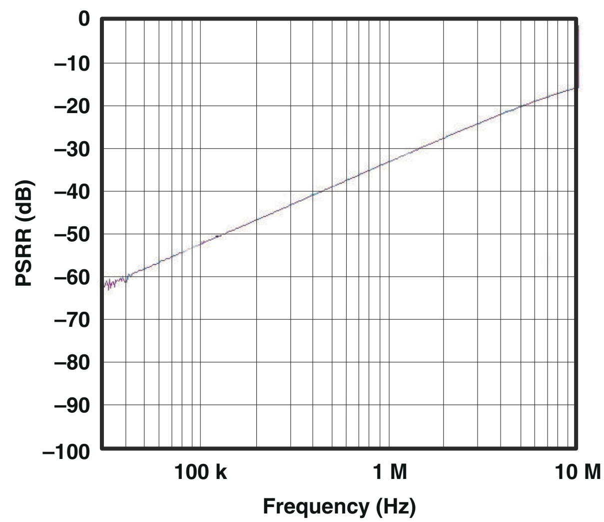

图 6-16. Com Port to No0 PSRR, In1 = V_{CC}, In2 = V_{CC} (V_{CC} = 5 V)

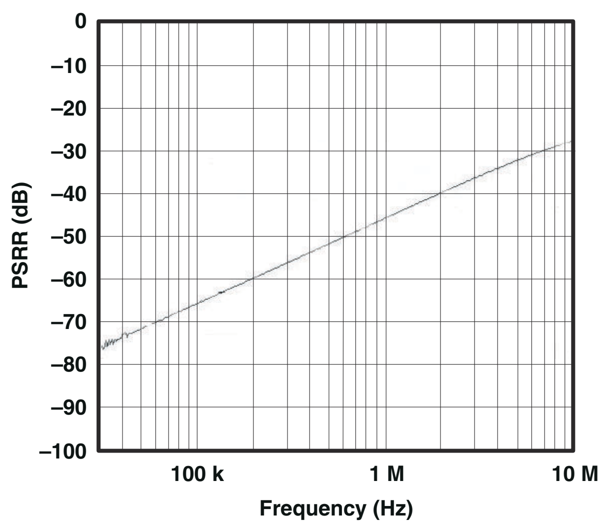

图 6-17. Com Port Hi-Z PSRR, In1 = 0 V, In2 = 0 V (V_{CC} = 5 V)

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7 Parameter Measurement Information

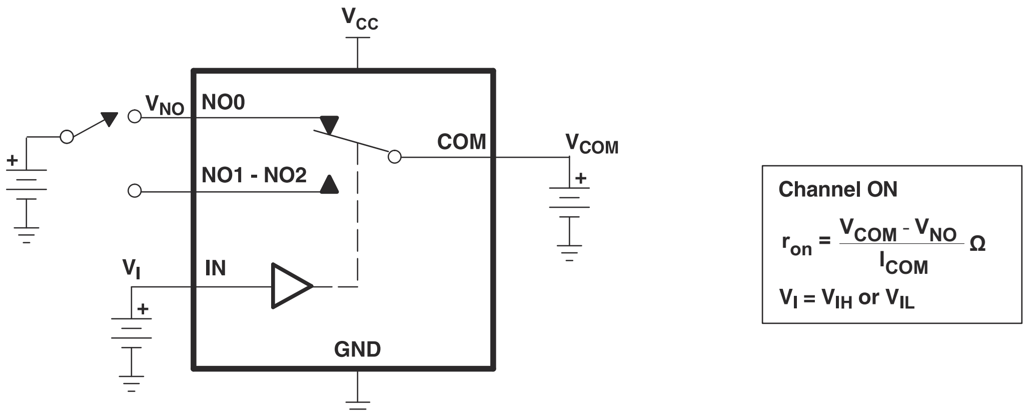

图 7-1. ON-State Resistance (R_{on})

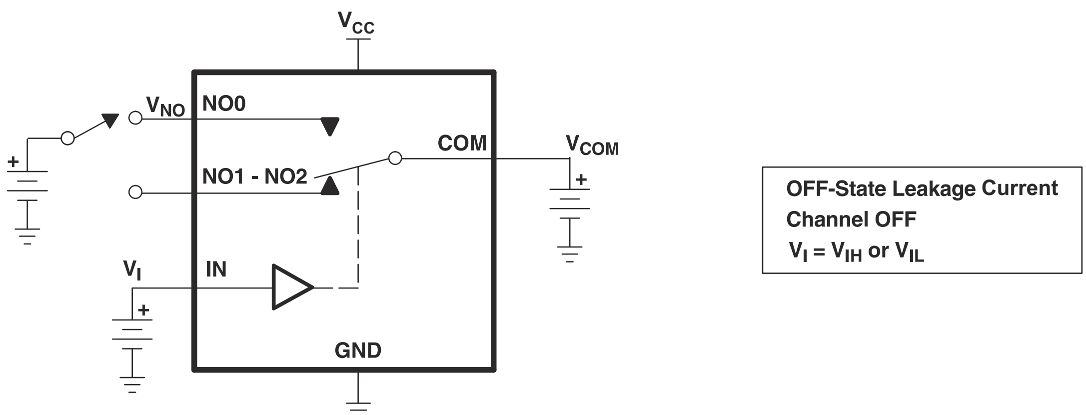

图 7-2. OFF-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$, $I_{NO(PWROFF)}$, $I_{COM(OFF)}$, $I_{COM(PWROFF)}$)

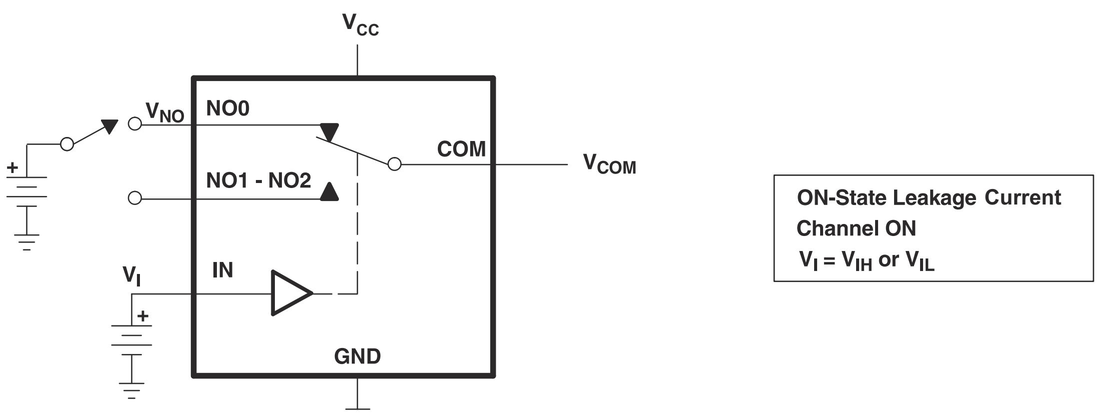

图 7-3. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

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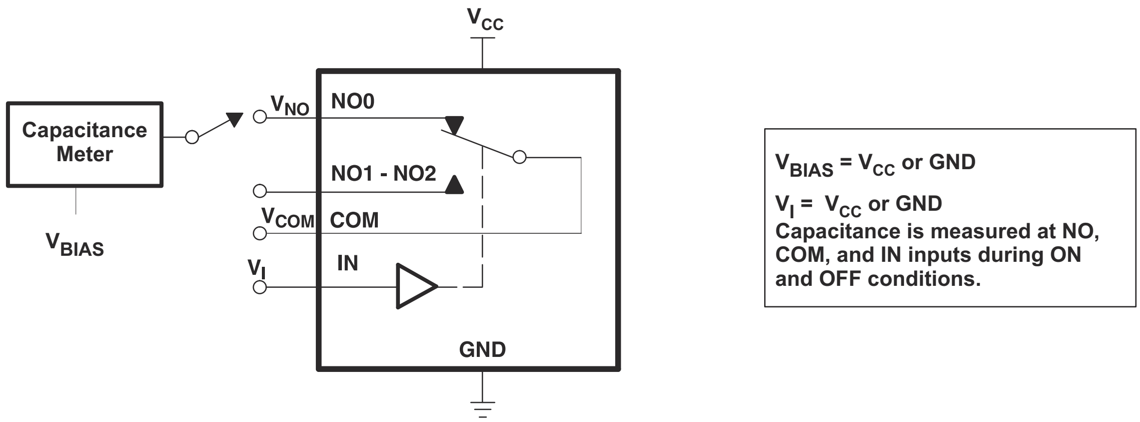
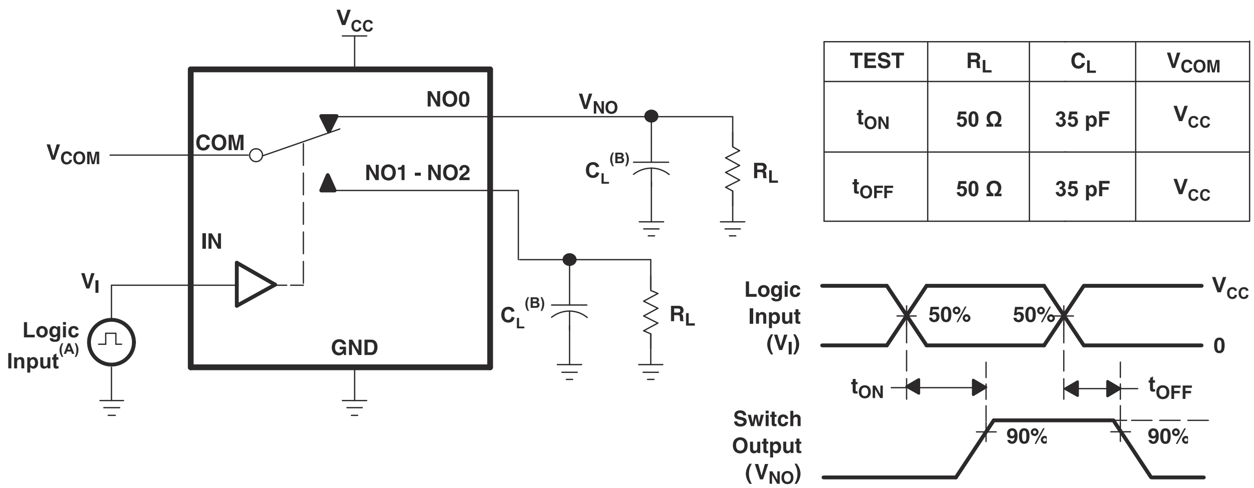


图 7-4. Capacitance (C_I, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{COM(OFF)}$, $C_{NO(ON)}$)

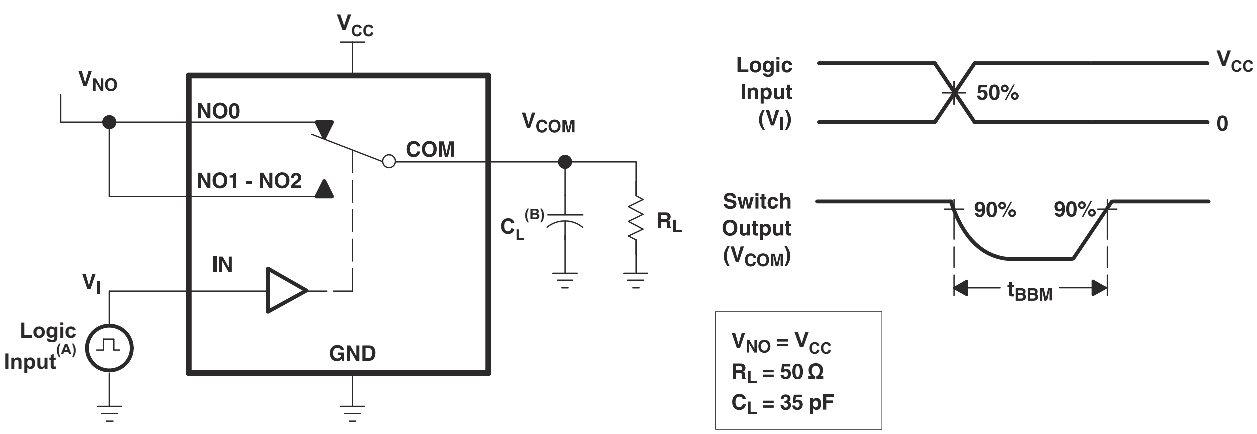


TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{CC}
t_{OFF}	50 Ω	35 pF	V_{CC}

A. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, ZO = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

图 7-5. Turnon (t_{ON}) and Turnoff Time (t_{OFF})



A. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, ZO = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

图 7-6. Break-Before-Make Time (t_{BBM})

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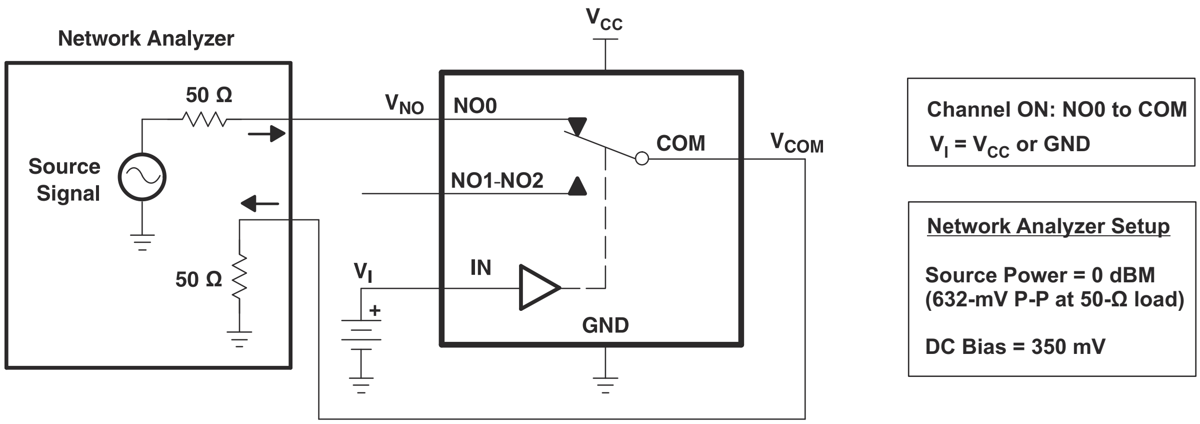


图 7-7. Bandwidth (BW)

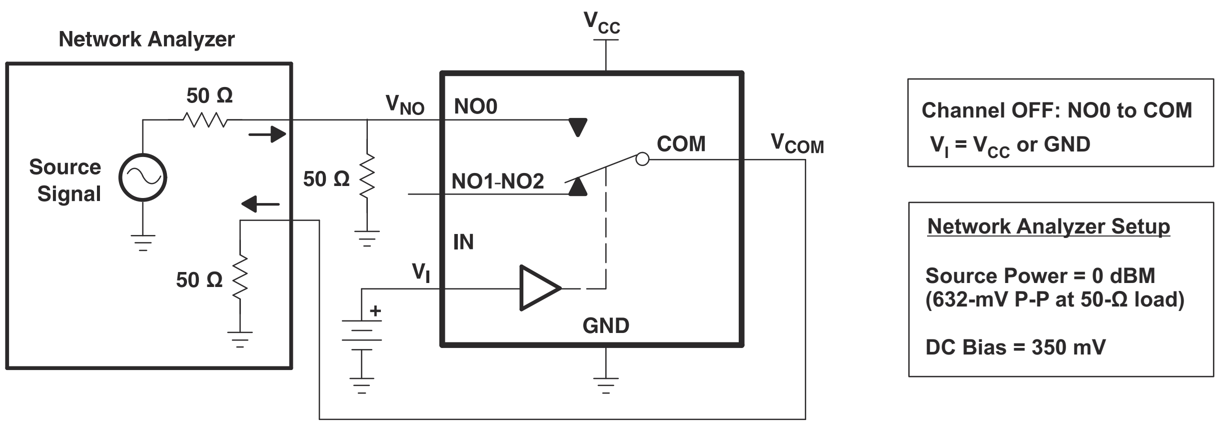


图 7-8. Off Isolation (O_{ISO})

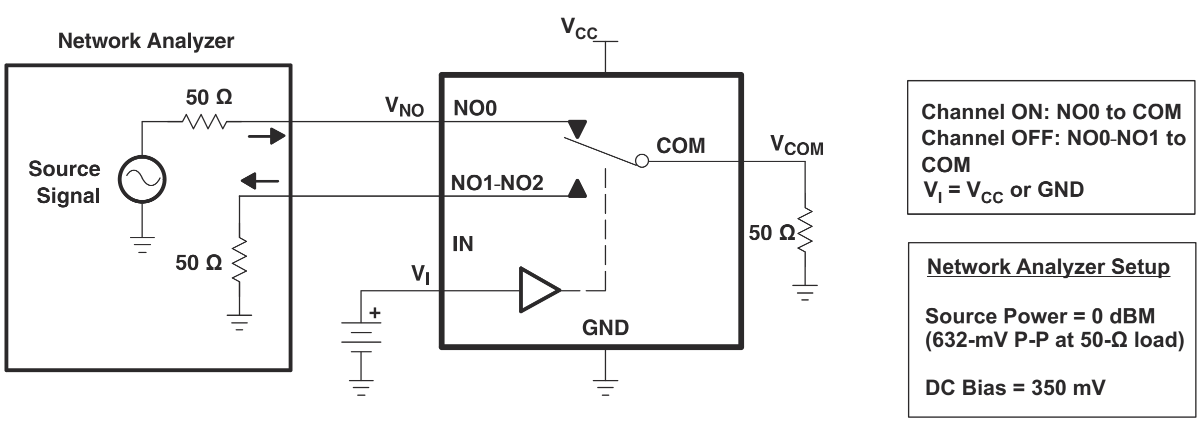
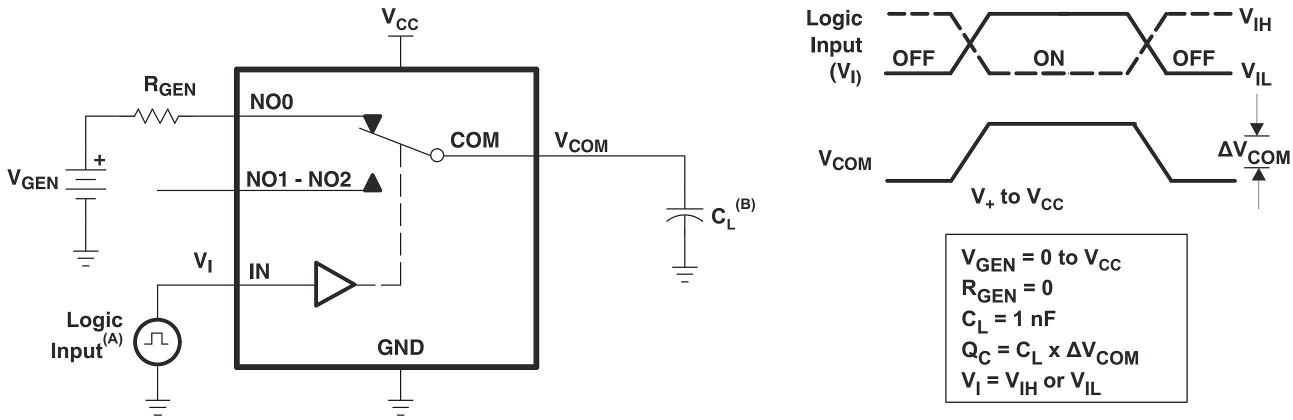


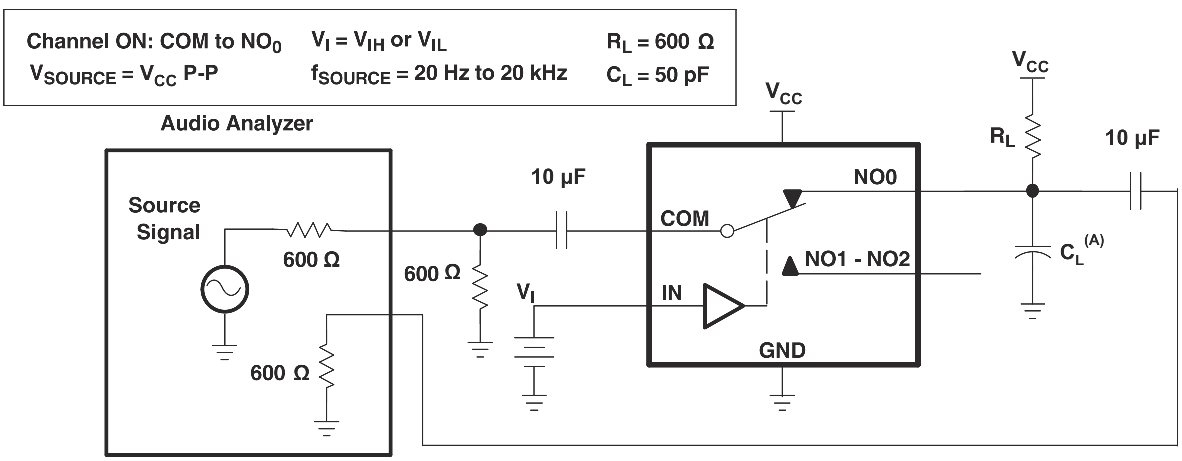
图 7-9. Crosstalk (X_{TALK})



A. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, ZO = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

图 7-10. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

图 7-11. Total Harmonic Distortion (THD)

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表 7-1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports when the channel is ON
r_{peak}	Peak ON-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels in a specific device
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(PWROFF)}$	Leakage current measured at the NO port during the power-down condition, V_{CC} = 0.
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) open
$I_{COM(OFF)}$	Leakage current measured at the COM port during the power-down condition, V_{CC} = 0
$I_{COM(PWROFF)}$	Leakage current measured at the COM port during the power-down condition, V_{CC} = 0.
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO) when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input.Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB less than the DC gain.
THD	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_{CC}	Static power-supply current with the control (IN) pin at V_{CC} or GND

表 7-2. Summary of Characteristics(1)

PARAMETER	CHARACTERISTIC
Configuration	Triple 3:1 Multiplexer/ Demultiplexer (1 × SP3T)
Number of channels	1
ON-state resistance (r_{on})	1.1 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turnon/turnoff time (t_{ON}/t_{OFF})	40 ns/35 ns
Break-before-make time (t_{BBM})	1 ns
Charge injection (Q_C)	40 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	–65 dB at 10 MHz
Crosstalk (X_{TALK})	–66 dB at 10 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{COM(OFF)}/I_{NO(OFF)}$)	±20 μA
Power supply current (I_{CC})	0.1 μA
Package options	8-pin DCU or YZP

(1) V_{CC} = 5 V, T_A = 25°C

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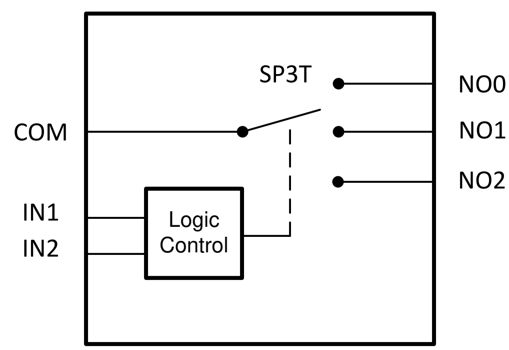
8 Detailed Description

8.1 Overview

The TS5A3359 is a bidirectional, single-channel, single-pole triple-throw (SP3T) analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3359 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS5A3359 device also has a specified break-before-make feature. The device consumes very low power and provides isolation when V_{CC} = 0.

8.2 Functional Block Diagram



8.3 Feature Description

Isolation in Power-Down Mode, V_{CC} = 0

When power is not supplied to the VCC pin, V_{CC} = 0 , the signal paths NO and COM are high impedance. This is specificed in the electrical characterisitics table under the COM and NO OFF leakage current when V_{CC} = 0. Because the device is high impedance when it is not powered, you may connect other signals to the signal chain without interference of the TS5A3359.

8.4 Device Functional Modes

表 8-1. Function Table

IN2	IN1	COM TO NO, NO TO COM
L	L	OFF
L	H	COM = NO0
H	L	COM = NO1
H	H	COM = NO2

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TS5A3359 switch is bidirectional, so the NO and COM pins can be used as either inputs or outputs. This switch is typically used when there is only one signal path that needs to be able to communicate to 3 different signal paths.

9.2 Typical Application

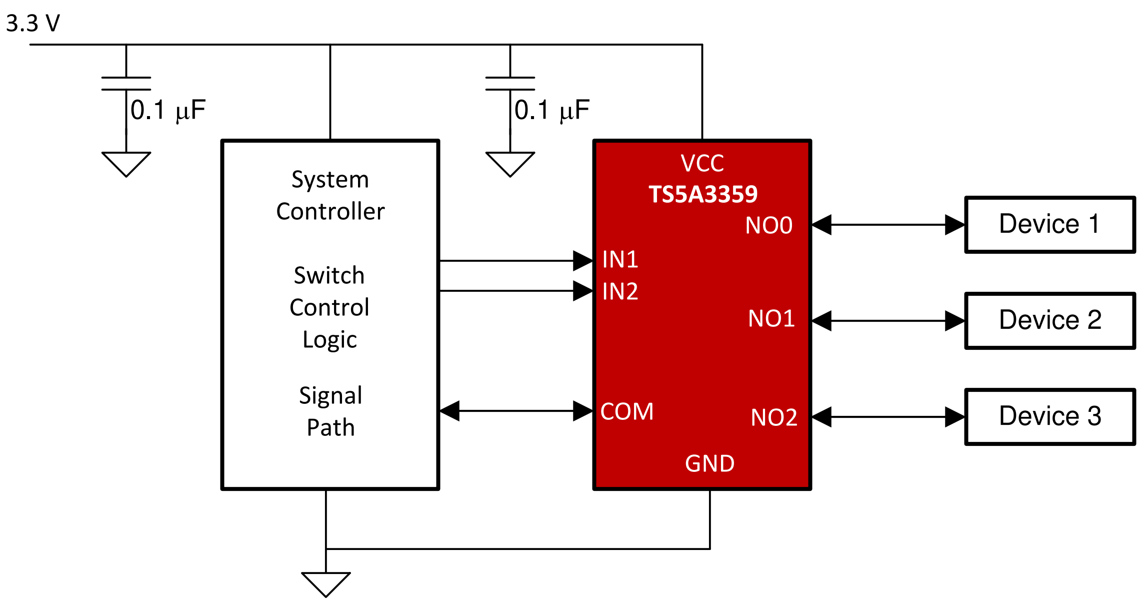


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

The TS5A3359 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3359 input and output signal swing through NO and COM are dependent on the supply voltage V_{CC}. For example, if the desired signal level to pass through the switch is 5 V, V_{CC} must be greater than or equal to 5 V. V_{CC} = 3.3 V would not be valid for passing a 5-V signal since the Analog signal voltage cannot exceed the supply.

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9.2.2 Detailed Design Procedure

The TS5A3359 device can be properly operated without any external components. However, TI recommends connecting unused pins to ground through a 50-Ω resistor to prevent signal reflections back into the device. TI also recommends pulling up the digital control pins (IN1 and IN2) to VCC or pulling down to GND to avoid undesired switch positions that could result from the floating pin.

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3359 input/output signal swing through NO and COM are dependant of the supply voltage V_{CC}.

9.2.3 Application Curve

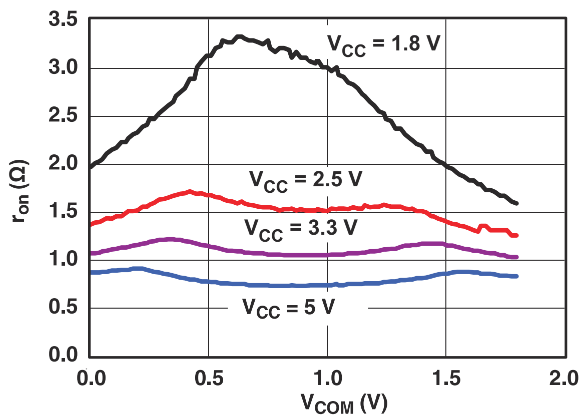

图 9-2. R_{on} vs V_{COM}

10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO or COM.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

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11 Layout

11.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

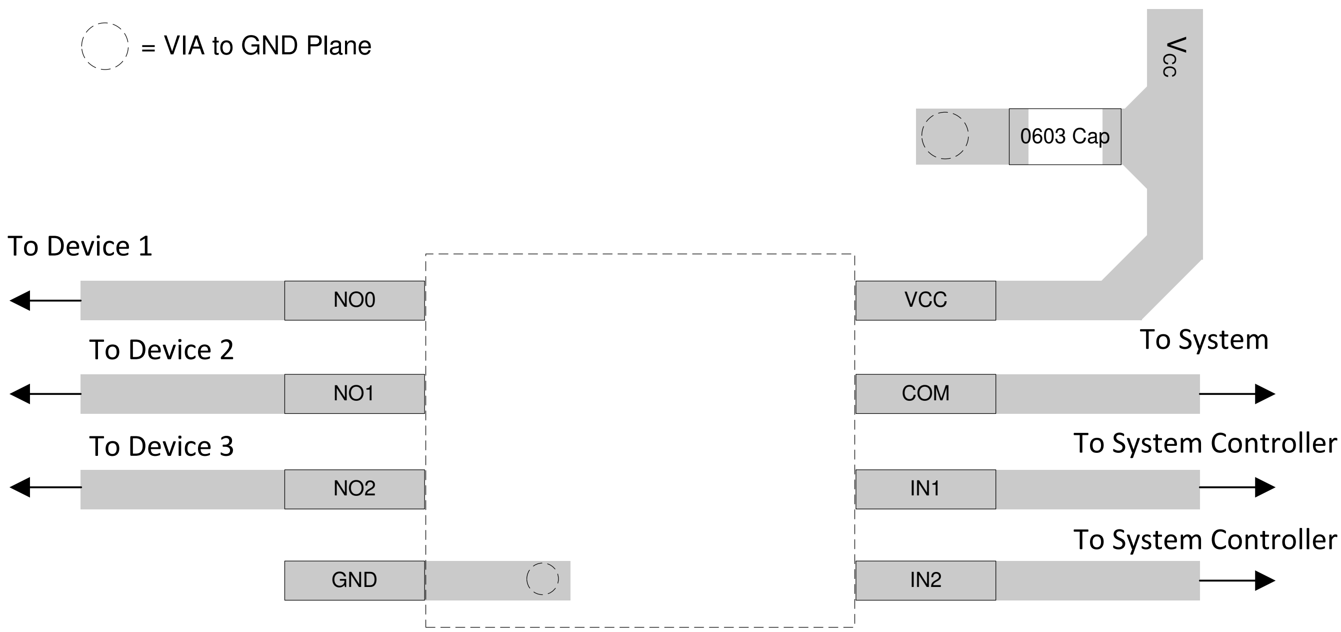

图 11-1. Recommended Layout

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12 Device and Documentation Support

12.1 接收文档更新通知

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12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3359DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL, JALR) JZ	Samples
TS5A3359DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL, JALR) JZ	Samples
TS5A3359DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(AL, JALR) JZ	Samples
TS5A3359YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	J9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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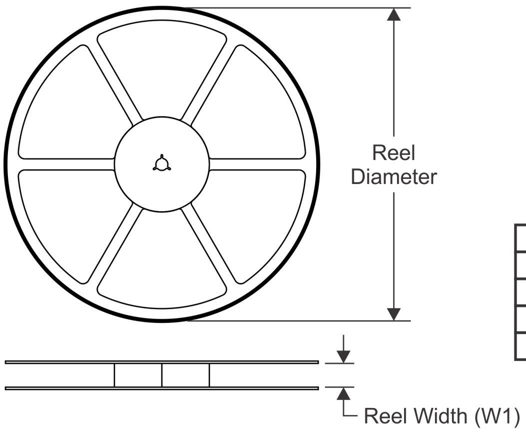
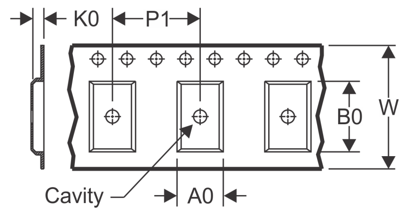
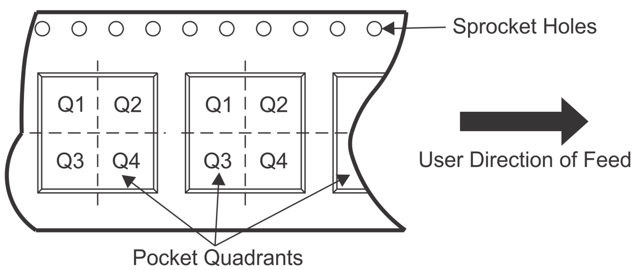
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

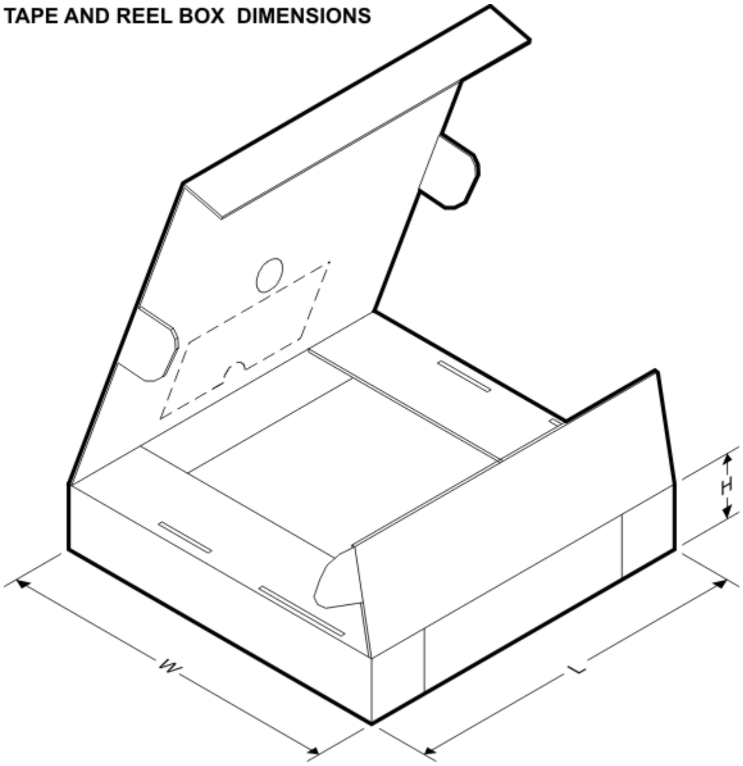
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

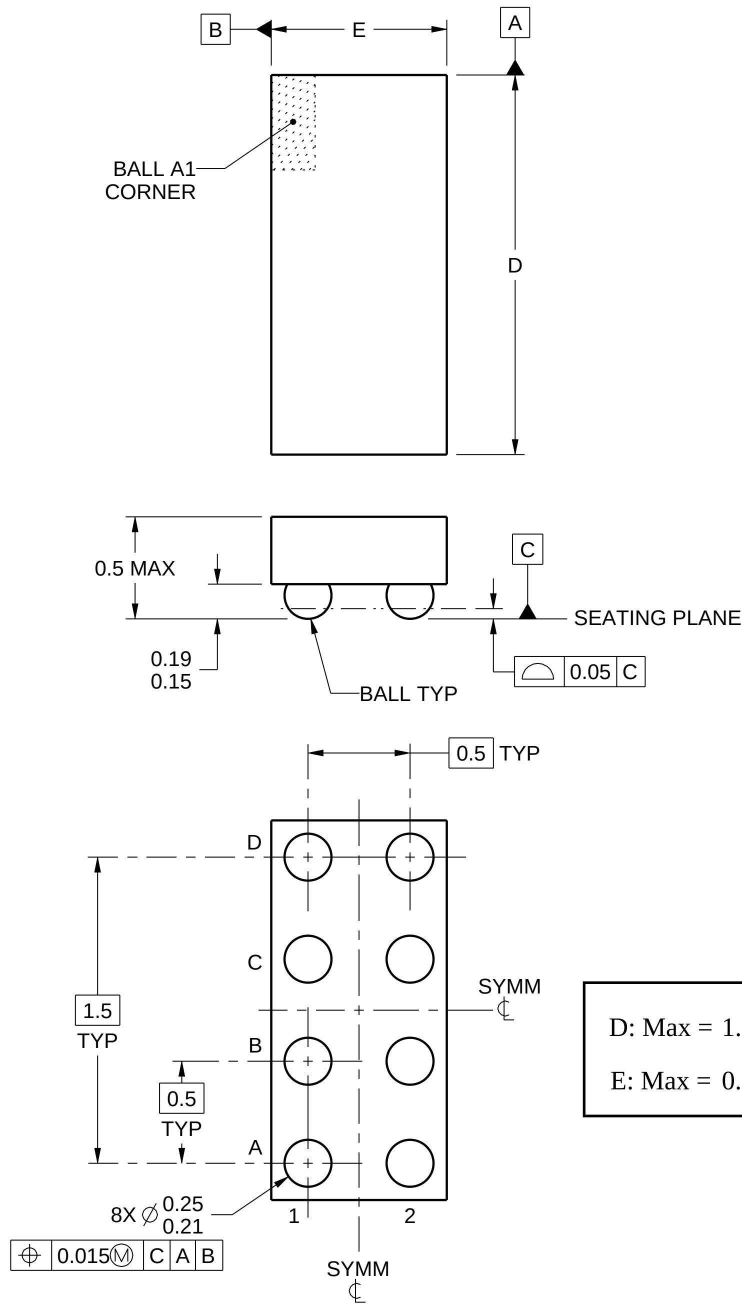
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3359DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
TS5A3359YZPR	DSBGA	YZP	8	3000	180.0	8.4	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3359DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
TS5A3359YZPR	DSBGA	YZP	8	3000	210.0	185.0	35.0



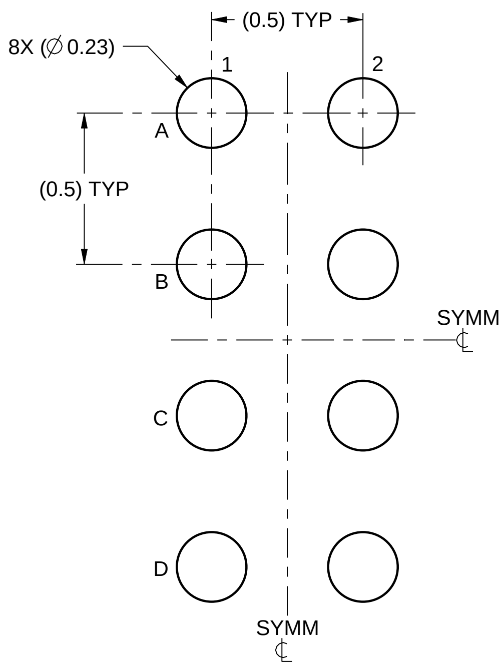
D: Max = 1.918 mm, Min =1.858 mm

E: Max = 0.918 mm, Min =0.858 mm

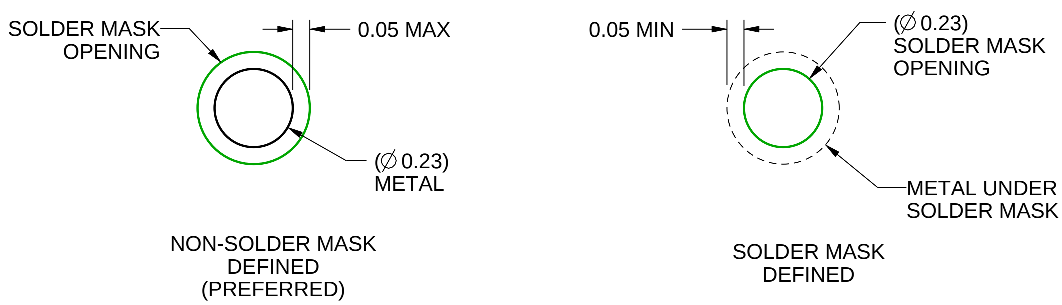
4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

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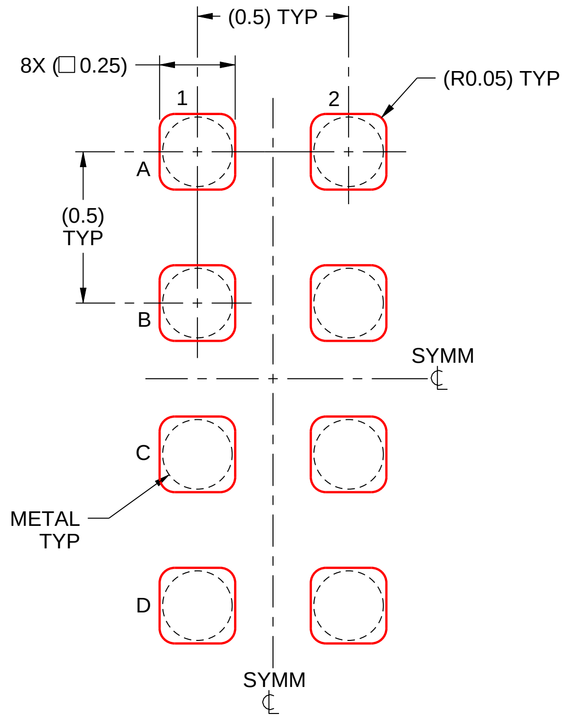
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



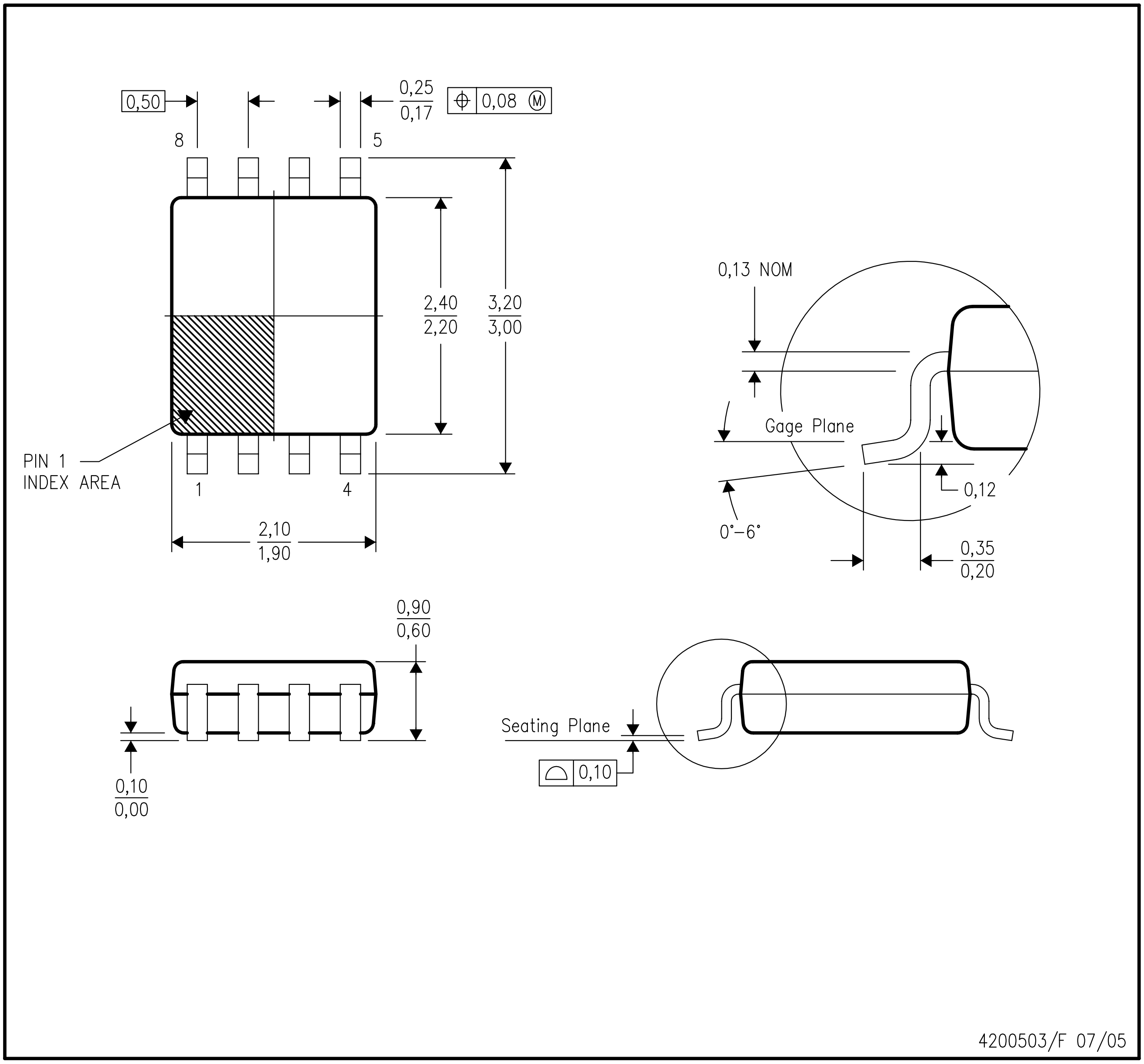
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

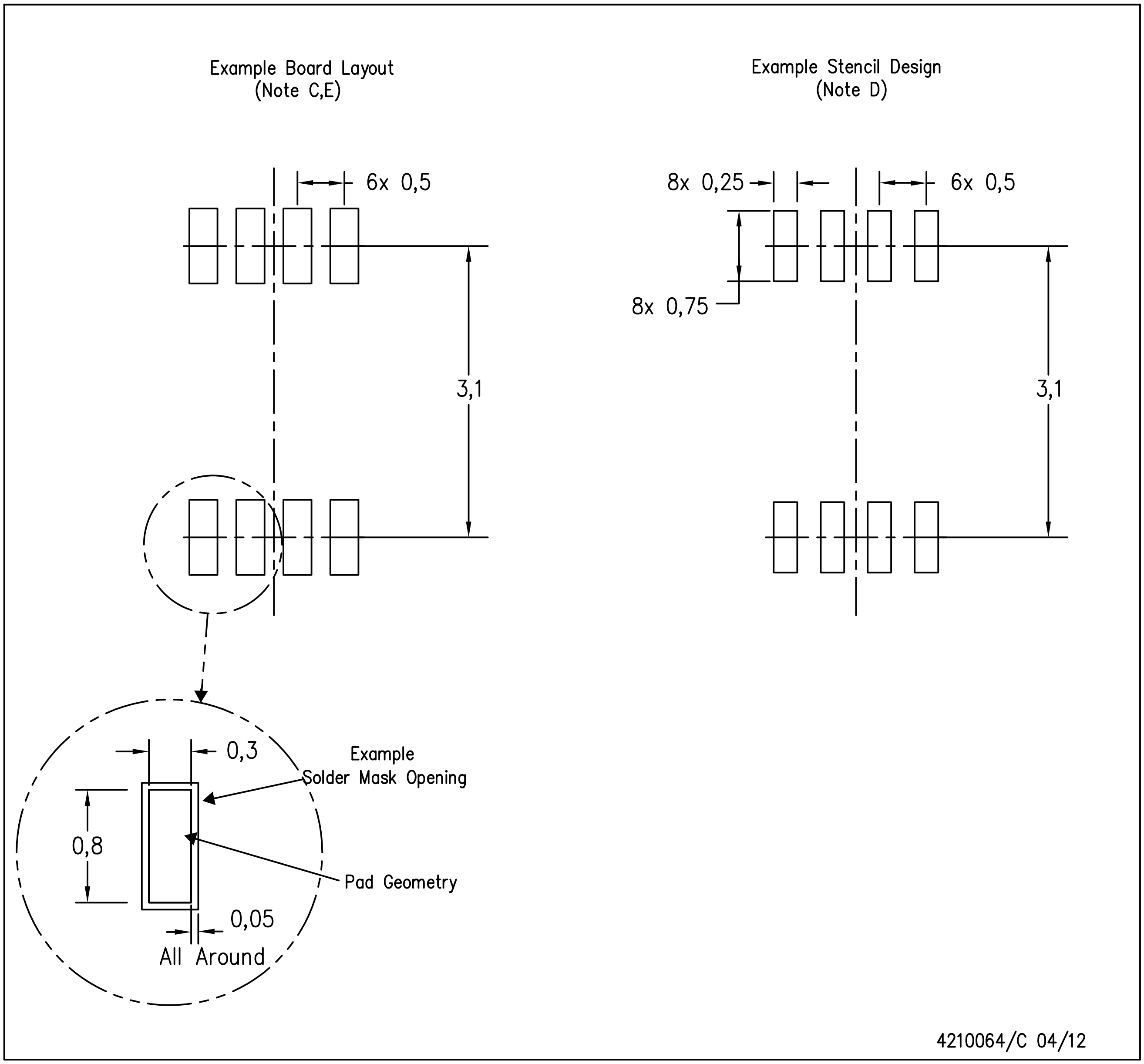
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DCU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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