TEXAS INSTRUMENTS
UCC14240-Q1
ZHCSOX6 – SEPTEMBER 2021

UCC14240-Q1 1.5W、24V V_{IN} 高效 > 3kV_{RMS} 隔离式直流/直流模块

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C ≤ T_J ≤ 150°C
  - 温度等级 1：–40°C ≤ T_A ≤ 125°C
- 采用隔离变压器的完全集成高效隔离式直流/直流转换器
- 隔离式直流/直流模块，用于驱动：IGBT、SiC FET
- T_A = 105°C 时输出功率 > 1.5W
- 输入电压范围：21V 至 27V，绝对最大值为 32V
- 可调节的 (VDD – VEE) 输出电压（通过外部电阻器）：在整个温度范围内为 18V 至 25V，精度为 ±1.3%
- 可调节的 (COM – VEE) 输出电压（通过外部电阻器）：从 2.5V 到 (VDD – VEE)，精度为 ±1.3%
- 电磁辐射低
- UVLO、OVLO、电源正常、软启动、短路、功率限制和过热保护
- CMTI > 150kV/μs
- 36 引脚宽体 SOIC 封装
- 计划的安全相关认证：
  - 符合 DIN V VDE V 0884-11:2017-01 标准的 5657VPK 隔离
  - 长达 1 分钟的 3000VRMS 隔离，符合 UL 1577 标准
  - 获得 UL 认证，符合 IEC 60950-1、IEC 62368-1 和 IEC 60601-1 终端设备标准
  - 符合 GB4943.1-2011 的 CQC 认证

2 应用

- 混合动力、电动和动力总成系统 (EV/HEV)
  - 汽车直流/直流转换器
  - 混合动力汽车/电动汽车逆变器和电机控制
  - 电动汽车充电站电源模块
  - 车载充电器 (OBC) 和无线充电器
- 电网基础设施
  - 直流充电（桩）站
  - 串式逆变器
- 电机驱动器
- 机器人伺服驱动器

3 说明

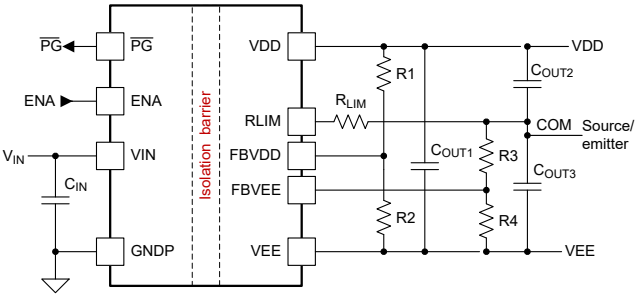
UCC14240-Q1 是一款高隔离电压直流/直流模块，旨在为 IGBT 或 SiC 栅极驱动器供电。高精度输出电压可提供更好的通道增强，从而实现更高的系统效率，不会对功率器件栅极造成过应力。该模块集成了具有专有架构的变压器和直流/直流控制器，可实现较高的效率和极低的辐射。

UCC14240-Q1 可以高效提供大于 1.5W（典型值）的隔离式输出功率。该模块需要非常少的外部元件，并且具有片上器件保护功能，可提供额外的特性，例如输入欠压锁定、过压锁定、输出电压电源正常比较器、过热关断、软启动时序、可调隔离式正负输出电压、使能引脚和开漏输出电源正常引脚。

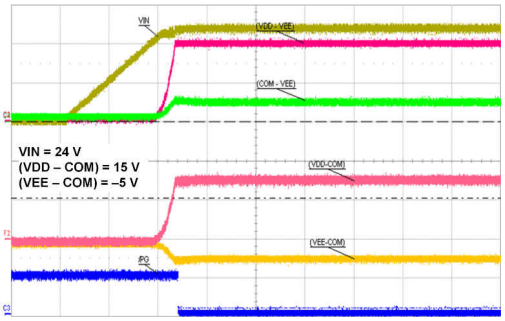
器件信息

器件型号(1)	封装	封装尺寸（标称值）
UCC14240-Q1	SSOP	12.83 mm × 7.50 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用



典型上电序列

ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
September 2021	*	Initial release

5 Pin Configuration and Functions

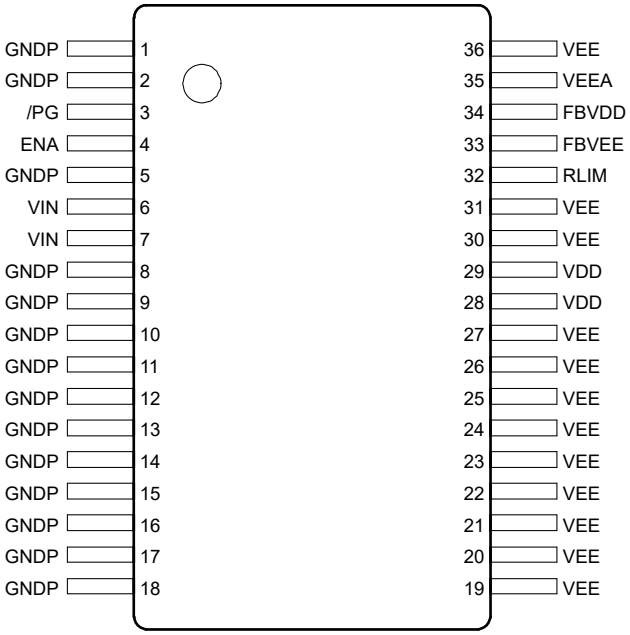


图 5-1. DWN Package, 36-Pin SSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
GNDP	1, 2, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	G	Primary-side ground connection for VIN. Place several vias to copper pours for thermal relief. See *Layout Guidelines*.
/PG	3	O	Active low powergood open-drain output pin. /PG pulled low when (UVLO ⩽ VIN ⩽ OVLO); (UVP1 ⩽ (VDD – VEE) ⩽ OVP1); (UVP2 ⩽ (COM – VEE) ⩽ OVP2); $T_{J\_Primary} \leqslant T_{SHUT\_primary}$; and $T_{J\_secondary} \leqslant T_{SHUT\_secondary}$
ENA	4	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5-V recommended maximum.
VIN	6, 7	P	Primary input voltage. Connect a 2.2-µF ceramic capacitor from VIN to GNDP. Connect a 0.1-µF high-frequency bypass ceramic capacitor close the pins.
VEE	19, 20, 21, 22, 23, 24, 25,26, 27, 30,31, 36	G	Secondary-side reference connection for VDD and COM. The VEE pins are used for the high current return paths.
VDD	28, 29	P	Secondary-side isolated output voltage from transformer. Connect a 2.2-µF and a parallel 0.1-µF ceramic capacitor from VDD to VEE. The 0.1-µF ceramic capacitor is the high frequency bypass and must be next to the IC pins.
RLIM	32	P	Secondary-side second isolated output voltage resistor to limit the source current from VDD to COM node, and the sink current from COM to VEE. Connect a resistor from RLIM to COM to regulate the (COM – VEE) voltage. See 节 8.2.2.1 for more detail.
FBVEE	33	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect a resistor divider from COM to VEE so that the midpoint is connected to FBVEE, and the equivalent FBVEE voltage when regulating is 2.5 V. Add a 100-pF to 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 0.1-µF ceramic capacitor for high frequency bypass must be next to the FBVEE and VEEA IC pins on top layer or back layer connected with vias.

ADVANCE INFORMATION

表 5-1. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
FBVDD	34	I	Feedback (VDD – VEE) output voltage sense pin and to adjust the output (VDD – VEE) voltage. Connect a resistor divider from VDD to VEE so that the midpoint is connected to FBVDD, and the equivalent FBVDD voltage when regulating is 2.5 V. Add a 100-pF to 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 0.1-µF ceramic capacitor for high frequency bypass must be next to the FBVDD and VEEA IC pins on top layer or back layer connected with vias.
VEEA	35	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback inputs, FBVDD and FBVEE. Connect the low-side feedback resistors and high frequency decoupling filter capacitor close to the VEEA pin and respective feedback pin FBVDD or FBVEE. Connect to secondary-side gate drive lowest voltage reference, VEE. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the VEEA pin. See *Layout Guidelines*.

(1) P = power, G = ground, I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	VIN to GNDP	–0.3	32	V
	ENA, /PG to GNDP	–0.3	7	V
	VDD, VEE, FBVDD, FBVEE to VEE	–0.3	32	V
P_{LOSS_MAX}	Total power loss at T_A = 25 °C,		2.45	W
$P_{OUT\_VDD\_MAX}$	Total (VDD - VEE) output power at T_A = 25 °C,		4	W
$P_{OUT\_VEE\_MAX}$	Total (COM - VEE) output power at T_A = 25 °C,		0.75	W
T_J	Operating junction temperature range	–0.3	150	°C
T_{stg}	Storage temperature	–0.3	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed in the *Recommended Operating Conditions* table. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VIN}	Primary-side input voltage to GNDP	21	24	27	V
V_{ENA}	Enable to GNDP	0		5.5	V
$V_{/PG}$	Powergood to GNDP	0		5.5	V
V_{VDD}	VDD to VEE	18		25	V
V_{VEE}	COM to VEE	2.5		VDD – VEE	V
V_{FBVDD}	FBVDD to VEE	0	2.5	5.5	V
V_{FBVEE}	FBVEE to VEE	0	2.5	5.5	V
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		UCC14240-Q1 DWN (SOIC) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.6	°C/W

ADVANCE INFORMATION

6.4 Thermal Information (continued)

THERMAL METRIC(1)		UCC14240-Q1 DWN (SOIC) 36 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	25.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Power Ratings

V_{IN} = 24 V, C_{IN} = C_{OUT} = 2.2 µF, T_J = 150 °C

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Power dissipation	(VDD – VEE) = 25 V, I_{VDD} = 1500 mW, (COM – VEE) = 5 V; I_{RLIM} = 375 mW	540	mW
P_{DP}	Power dissipation by driver side (primary)		120	mW
P_{DS}	Power dissipation by rectifier side (secondary)		100	mW
P_{DT}	Power dissipation by transformer		320	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 120	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Over-voltage Category	Rated mains voltage ⩽ 300 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 600 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 1000 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01(2) (Planned Certification Targets)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1202	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	850	V_{RMS}
		DC voltage	1202	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification); V_{TEST} = 1.2 × V_{IOTM}, t = 1s (100% production)	4243	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, V_{TEST} = 1.3 × V_{IOSM} = 6500 V_{PK} (qualification)	5000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1442 V_{PK}, t_m = 10 s	⩽ 5	pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 1442 V_{PK}, t_m = 10 s	⩽ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.5 × V_{IORM} = 1803 V_{PK}, t_m = 1 s	⩽ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2 π ft), f = 1 MHz	approximately 3.5	pF

ADVANCE INFORMATION

6.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577 (Planned Certification Target)				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 3000 V_{RMS}, t = 60 s (qualification); V_{TEST} = 1.2 × V_{ISO} = 3600 V_{RMS}, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements must be applied according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Electrical Characteristics

Over operating temperature range (= – 40 °C ≤ T_J ≤ 150 °C, 21 V ≤ V_{IN} ≤ 27 V, C_{IN} = C_{OUT} = 2.2 µF, V_{ENA} = 5 V, R_{LIM} = 1 kΩ unless otherwise noted. All typical values at T_A = 25 °C and V_{IN} = 24 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)						
V_{VIN}	Input voltage range	Primary-side input voltage to GNDP	21	24	27	V
I_{VINQ_OFF}	VIN quiescent current,disabled	ENA = 0 V, VIN = 21 V – 27 V; IOUT = no load			500	µA
$I_{VIN\_ON\_NO\_LOAD}$	VIN operating current, no load	ENA = 5 V; VIN = 21 V – 27 V; (VDD – VEE) regulating; I((VDD – VEE)) = no load			8	mA
$I_{VIN\_ON\_FULL\_LOAD}$	VIN operating current, full load	ENA = 5 V; VIN = 21 V – 27 V; (VDD – VEE) = 25-V regulating; I((VDD – VEE)) = 60 mA			135	mA
UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_UVLOP\_RISING}$	VIN under-voltage lockout rising threshold	Voltage at VIN pin while VIN rising		20		V
$V_{VIN\_UVLOP\_FALLING}$	VIN under-voltage lockout falling threshold	Voltage at VIN pin while VIN falling		18		V
OVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_OVLO\_RISING}$	VIN over-voltage lockout rising threshold	Voltage at VIN pin while VIN rising		31		V
$V_{VIN\_OVLO\_FALLING}$	VIN over-voltage lockout falling threshold	Voltage at VIN pin while VIN falling		29		V
TSHUTP THERMAL SHUTDOWN COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$TSHUTP_{PRIMARY\_RISE}$	Primary-side over-temperature shutdown rising threshold	First time at power-up T_j needs to be < 140 °C to turn-on.	150	160		°C
$TSHUTP_{PRIMARY\_HYST}$	Primary-side over-temperature shutdown hysteresis			20		°C
EN INPUT PIN (Primary-side. All voltages with respect to GNDP)						
V_{EN_IR}	Input voltage rising threshold, logic HIGH	Rising edge			2.1	V

ADVANCE INFORMATION

6.7 Electrical Characteristics (continued)

Over operating temperature range (= –40 °C ≤ T_J ≤ 150 °C, 21 V ≤ V_{IN} ≤ 27 V, C_{IN} = C_{OUT} = 2.2 µF, V_{ENA} = 5 V, R_{LIM} = 1 kΩ unless otherwise noted. All typical values at T_A = 25 °C and V_{IN} = 24 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{EN_IF}	Input voltage falling threshold, logic LOW	Falling edge	0.8			V
I_{EN}	Enable Pin Input Current	V_{EN} = 5.0 V		5	10	µA
/PG OPEN-DRAIN OUTPUT PIN (Primary-side. All voltages with respect to GNDP) [/PG is Active Low]						
$V_{/PG\_OUT\_LO}$	/PG output-low saturation voltage	Sink Current = 5 mA, power is good			0.5	V
$I_{/PG\_OUT\_HI}$	/PG Leakage current	/PG = 5.5 V, power is not good			5	µA
SWITCHING FREQUENCY (Primary-side. All voltages with respect to GNDP)						
$F_{SW\_CARRIER}$	Switching frequency range	ENA = 5 V; (VDD – VEE) = 25 V	11	13	17	MHz
VDD OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
V_{VDD_RANGE}	(VDD - VEE) Output voltage range	Secondary-side (VDD – VEE), adjust with external resistor divider	18	22	25	V
$V_{VDD\_DC\_ACCURACY}$	(VDD - VEE) Output voltage DC regulation accuracy	Secondary-side (VDD – VEE) over load, line and temperature; externally adjust with external resistor divider	-1.3		1.3	%
VDD REGULATION HYSTERETIC COMPARATOR (Secondary-side. All voltages with respect to VEE)						
V_{FBVDD_REF}	Feedback regulation reference voltage for (VDD - VEE)	During secondary soft-start, the (VDD – VEE) reference is stepped-up		2.5		V
VEE OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
V_{VEE_RANGE}	(COM - VEE) Output voltage range	Secondary-side (COM – VEE), adjust with external resistor divider	2.5	5	(VDD-VEE)	V
$V_{(VDD-VEE)\_DC\_ACCURACY}$	(VDD - VEE) Output voltage DC regulation accuracy	Secondary-side VDD output voltage to VEE over load, line and temperature; externally adjust with external resistor divider	-1.3		1.3	%
VEE REGULATION HYSTERETIC COMPARATOR (Secondary-side. All voltages with respect to VEE)						
V_{FBVEE_REF}	Feedback regulation reference voltage for (COM - VEE)	During secondary soft-start, the (COM – VEE) reference is stepped-up same as (VDD – VEE) reference		2.5		V
UVLOS COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_UVLO\_RISING}$	(VDD - VEE) under-voltage lockout rising threshold	Voltage at FBVDD, using an external resistor divider from VDD to VEE, midpoint connected to FBVDD.		0.9		V
$V_{VDD\_UVLO\_HYST}$	(VDD - VEE) under-voltage lockout hysteresis	Voltage at FBVDD, using an external resistor divider from VDD to VEE, midpoint connected to FBVDD.		0.2		V
$t_{VDD\_UVLO\_DEGLITCH}$	(VDD - VEE) under-voltage lockout deglitch time	Voltage at FBVDD, using an external resistor divider from VDD to VEE, midpoint connected to FBVDD.		2.5		µs
OVLOS COMPARATOR (Secondary-side. All voltages with respect to VEE)						

ADVANCE INFORMATION

6.7 Electrical Characteristics (continued)

Over operating temperature range (= –40 °C ⩽ T_J ⩽ 150 °C, 21 V ⩽ V_{IN} ⩽ 27 V, C_{IN} = C_{OUT} = 2.2 µF, V_{ENA} = 5 V, R_{LIM} = 1 kΩ unless otherwise noted. All typical values at T_A = 25 °C and V_{IN} = 24 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VDD\_OVLOS\_RISING}$	(VDD - VEE) over-voltage lockout rising threshold	Voltage from VDD to VEE		31		V
$V_{VDD\_OVLOS\_FALLING}$	(VDD - VEE) over-voltage lockout falling threshold	Voltage from VDD to VEE		29		V
$t_{VDD\_OVLOS\_DEGLITCH}$	(VDD - VEE) over-voltage lockout deglitch time			32		µs
SOFT-START (Secondary-side. All voltages with respect to VEE)						
VREF_Voltage_per_Steps	Voltage per step	8 Steps start from 1.1 V and end at 2.5 V. That is, 200 mV per step.		0.2		V
VREF_Voltage_Start	VREF voltage at Start of secondary-side soft-start	8 Steps start from 1.1 V and end at 2.5 V. That is, 200 mV per step.		1.1		V
VREF_Voltage_End	VREF voltage at End of secondary-side soft-start	8 Steps start from 1.1 V and end at 2.5 V. That is, 200 mV per step.		2.5		V
$t_{duration}$	Time duration per step, until get to the last one			128		µs
UVP1, UNDER -VOLTAGE PROTECTION COMPARATOR VDD OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_UVP\_RISING}$	(VDD – VEE) under-voltage protection rising threshold	V_{UVP} = V_{REF} × 90%		2.25		V
$V_{VDD\_UVP\_HYST}$	(VDD – VEE) under-voltage protection hysteresis			25		mV
$t_{VDD\_UVP\_DEGLITCH}$	(VDD – VEE) under-voltage protection deglitch time			32		µs
$t_{VDD\_UVP\_FAULT\_DEGLITCH}$	(VDD – VEE) under-voltage protection fault latch-off deglitch time			64		µs
OVP1, OVER-VOLTAGE PROTECTION COMPARATOR VDD OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_OVP\_RISING}$	(VDD – VEE) over-voltage protection rising threshold	V_{OVP} = V_{REF} × 110%		2.75		V
$V_{VDD\_OVP\_HYST}$	(VDD – VEE) over-voltage protection hysteresis			25		mV
$t_{VDD\_OVP\_DEGLITCH}$	(VDD – VEE) over-voltage protection deglitch time			32		µs
$t_{VDD\_OVP\_FAULT\_DEGLITCH}$	(VDD – VEE) over-voltage protection fault latch-off deglitch time			64		µs
UVP2, UNDER -VOLTAGE PROTECTION COMPARATOR (COM – VEE) OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
$V_{VEE\_UVP\_RISING}$	(COM – VEE) under-voltage protection rising threshold	V_{UVP} = V_{REF} × 90%		2.25		V
$V_{VEE\_UVP\_HYST}$	(COM – VEE) under-voltage protection hysteresis			25		mV
$t_{VEE\_UVP\_DEGLITCH}$	(COM – VEE) under-voltage protection deglitch time			32		µs
$t_{VEE\_UVP\_FAULT\_DEGLITCH}$	(COM – VEE) under-voltage protection fault latch-off deglitch time	Fault is communicated to primary at any time to protect and enter a safe state.		64		µs

ADVANCE INFORMATION

6.7 Electrical Characteristics (continued)

Over operating temperature range (= –40 °C ≤ T_J ≤ 150 °C, 21 V ≤ V_{IN} ≤ 27 V, C_{IN} = C_{OUT} = 2.2 µF, V_{ENA} = 5 V, R_{LIM} = 1 kΩ unless otherwise noted. All typical values at T_A = 25 °C and V_{IN} = 24 V

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVP2, OVER-VOLTAGE PROTECTION COMPARATOR (COM – VEE) OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
$V_{VEE\_OVP\_RISING}$	(COM – VEE) over-voltage protection rising threshold	V_{OVP} = V_{REF} × 110%		2.75		V
$V_{VEE\_OVP\_HYST}$	(COM – VEE) over-voltage protection hysteresis			25		mV
$t_{VEE\_OVP\_DEGLITCH}$	(COM – VEE) over-voltage protection deglitch time			32		µs
$t_{VEE\_OVP\_FAULT\_DEGLITCH}$	(COM – VEE) over-voltage protection fault latch-off deglitch time	Fault is communicated to primary at any time to protect and enter a safe state.		64		µs
TSHUTS THERMAL SHUTDOWN COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$TSHUTS_{SECONDARY\_RISE}$	Secondary-side over-temperature shutdown rising threshold	First time at power-up T_J needs to be < 140 °C to turn-on.	150	160		°C
$TSHUTS_{SECONDARY\_HYST}$	Secondary-side over-temperature shutdown hysteresis			20		°C
$t_{TSHUTS\_DEGLITCH}$	Secondary-side over-temp shutdown deglitch time.	Rising and falling deglitch times		64		µs
WATCHDOG TIMEOUT (Primary-side. All voltages with respect to VEE)						
$t_{WATHCHDOG\_TIMEOUT}$	Primary-side Watchdog shutdown timeout time	Counts while no communication through isolation channel. Communication resets timer.		100		µs
HEARTBEAT TIMEOUT (Secondary-side. All voltages with respect to VEE)						
$t_{HEARTBEAT\_TIMEOUT}$	Secondary-side heartbeat interval time - reports Power is Good, Power is Not Good, or FAULT	Fixed time to reset WDT if active and okay, but no communication change needed.		30		µs
CMTI (Common Mode Transient Immunity)						
CMTI	Common mode transient immunity	Positive VEE with respect to GNDP	150			µs
		Negative VEE with respect to GNDP	| –150 |			µs
INTEGRATED TRANSFORMER (Primary-side to Secondary-side.)						
$N_{PRIMARY\_TO\_SECONDARY}$	Effective turns ratio			1.2		-

ADVANCE INFORMATION

6.8 Typical Characteristics

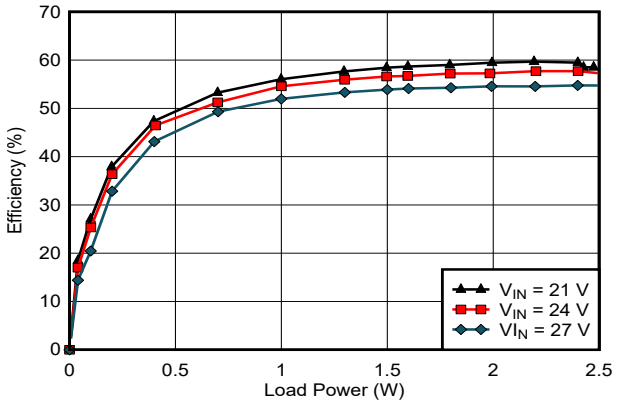


图 6-1. Efficiency vs Output Power

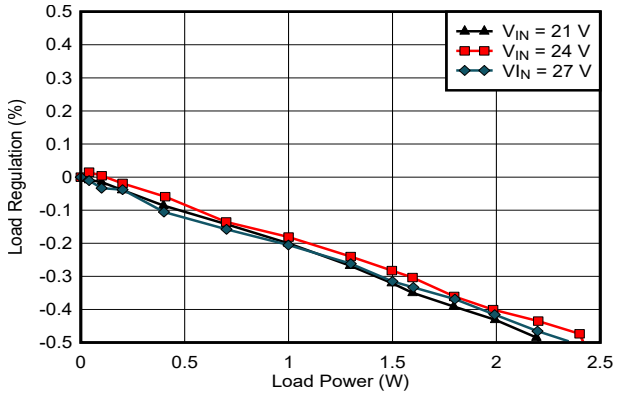


图 6-2. (VDD – VEE) Regulation Accuracy vs Output Power

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

UCC14240-Q1 device is suitable for applications that have limited board space and require more integration. These devices are also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive. The low-profile, low-center of gravity, and low weight provides a higher vibration tolerance than systems using large bulky transformers. The device is easy-to-use and provides flexibility to adjust both positive and negative output voltages as needed when optimizing the gate voltage for maximum efficiency while protecting gate oxide from over-stress with its tight voltage regulation accuracy.

The device integrates a high-efficiency, low-emissions isolated DC/DC converter for powering the gate drive of SiC or IGBT power devices in traction inverter motor drives, industrial motor drives, or other high voltage DC/DC converters. This DC/DC converter provides greater than 1.5 W of power across a 3000 V_{RMS} basic isolation barrier.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The integrated transformer provides power delivery throughout a wide temperature range while maintaining a 3000-V_{RMS} isolation, and an 850-V_{RMS} continuous working voltage. The low isolation capacitance of the transformer provides high CMTI allowing fast dv/dt switching and higher switching frequencies, while emitting less noise.

The VIN supply is provided to the primary-side power controller that switches the input stage connected to the integrated transformer. Power is transferred to the secondary-side output stage, and regulated to a level set by the resistor divider connected between the (VDD – VEE) pin and the FBVDD pin with respect to the VEE pin. The output voltage is adjustable with external resistor divider allowing a wide (VDD – VEE) range.

For optimal performance ensure to maintain the VIN input voltage within the recommended operating voltage range. Do not exceed the absolute maximum voltage rating to avoid over-stressing the input pins.

A fast hysteretic feedback burst control loop monitors (VDD – VEE) and ensures the output voltage is kept within the hysteresis with low overshoots and undershoots during load and line transients. The burst control loop enables efficient operation across full load and allows a wide VOUT adjustability throughout the whole VIN range. The undervoltage lockout (UVLO) protection monitors the input voltage pin, VIN, with hysteresis and input filter ensuring robust system performance under noisy conditions. The overvoltage lockout (OVLO) protection monitors the input voltage pin, VIN, protects against over-voltage stress by disabling switching and reducing the internal peak voltage. Controlled soft-start timing, provided throughout the full power-up time, limits the peak input inrush current while charging the output capacitor and load.

The UCC14240-Q1 also provides a second output rail, (COM – VEE), that is used as a negative bias for the gate drivers, allowing quicker turn-off switching for the IGBTs, and also to protect from unwanted turn-on during fast switching of SiC devices. (COM – VEE) is a simple, yet fast and efficient bias controller to ensure the positive and negative rails are regulated during the PWM switching. The COM pin can be connected from the source of SiC device or emitter of and IGBT device. An external current limiting resistor allows the designer to program the sink and source current peak according to the needs of the gate drive system.

A fault protection and powergood status pin provides a mechanism for the host controller to monitor the status of the DC/DC converter and provide proper sequencing of power and PWM control signals to the gate driver. Fault protection includes undervoltage, overvoltage, over-temperature shutdown, and isolated channel communication interface watchdog timer.

A typical soft-start ramp-up time is approximately 3 ms, but varies based on input voltage, output voltage, output capacitance, and load. If either output is shorted or over-loaded, the device is not able to power-up within the 16-ms soft-start watch-dog-timer protection time, so the device latches off for protection. The latch can be reset by toggling the ENA pin or powering VIN down and up.

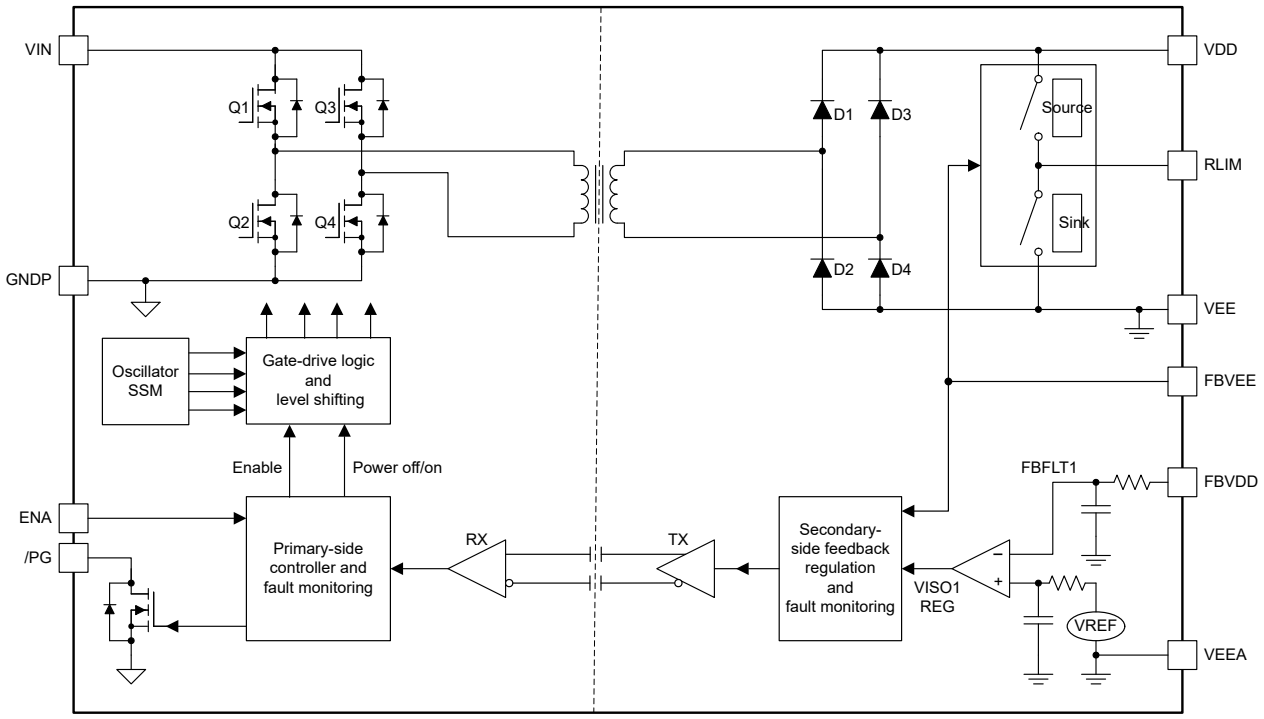
The output load must be kept low until start-up is complete and /PG pin is low. When powering up, do not apply a heavy load to (VDD – VEE) or (COM – VEE) outputs until the /PG pin has indicated power is good (pulling logic low) to avoid problems providing the power to ramp-up the voltage.

TI recommends to use the /PG status indicator as a trigger point to start the PWM signal into the gate driver. /PG output removes any ambiguity as to when the outputs are ready by providing a robust closed loop indication of when both (VDD – VEE) and (COM – VEE) outputs have reached their regulation threshold within ±10%.

Do not allow the host to begin PWM to gate driver until after /PG goes low. This action typically occurs less than 16 ms after VIN > UVLOp and ENA goes high. The /PG status output indicates the power is good after soft-start of (VDD – VEE) and (COM – VEE) and are within ±10% of regulation.

If the host is not monitoring /PG, then ensure that the host does not begin PWM to gate driver until 20 ms after VIN > UVLOp and ENA goes high in order to allow enough time for power to be good after soft-start of VDD and VEE.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Stage Operation

The UCC14240-Q1 module uses an active full-bridge inverter on the primary-side and a passive full-bridge rectifier on the secondary-side. The small integrated transformer has a relatively high carrier frequency to reduce the size for integrating into the 36-pin SOIC package. The power stage carrier frequency operates within 10 MHz to 16 MHz. Spread spectrum modulation, SSM, is used to reduce emissions. ZVS operation is maintained to reduce switching power losses.

7.3.2 Digital I/O ENA and /PG

The ENA input pin and /PG output pin on the primary-side use 5-V TTL and 3.3-V LVTTL level logic thresholds.

The active-high enable input (ENA) pin is used to turn-on the isolated DC/DC converter of the module. Either 3.3-V or 5-V logic rails can be used. Maintain the ENA pin voltage below 5.5 V.

ADVANCE INFORMATION

The active-low powergood (/PG) pin is an open-drain output that indicates (low) when the module has no fault and the output voltages are within ±10% of the output voltage regulation setpoints. Connect a pull-up resistor (> 1 kΩ) from /PG pin to either a 5-V or 3.3-V logic rail. Maintain the /PG pin voltage below 5.5 V.

7.3.3 Power-Up and Power-Down Sequencing

For the first pre-production samples, the ENA pin sequence must follow the recommendations below to allow the device to operate within the safe operating region.

Case A: After VIN has been applied and $V_{(ENA)}$ > V_{EN_IR}: Never set $V_{(ENA)}$ < V_{EN_IF} with $V_{(VIN)}$ > $V_{VIN\_UVLOP\_FALLING}$.

Case B: To reset a fault condition detected by the module that resulted in /PG = high, while keeping V(ENA) > V_{EN_IR}:

1. Set $V_{(VIN)}$ = 0 V
2. Wait until the (VDD – VEE) and (COM – VEE) rails are discharged
3. Set $V_{(VIN)}$ > $V_{VIN\_UVLOP\_RISING}$

Case C: To power-down and power-up, use this ENA triggered power-up sequence:

1. Set $V_{(VIN)}$ = 0 V while keeping V(ENA) > V_{EN_IR}
2. Wait until the (VDD – VEE) and (COM – VEE) rails are discharged
3. Set $V_{(ENA)}$ = 0 V
4. Set $V_{(VIN)}$ > $V_{VIN\_UVLOP\_RISING}$
5. Set $V_{(ENA)}$ > V_{EN_IR}

7.4 Device Functional Modes

表 7-1 lists the supply functional modes for this device. The ENA pin has an internal weak pull-down resistance to ground, but leaving this pin open is not recommended

表 7-1. Device Functional Modes

INPUT			OUTPUTS		
V_{VIN}	ENA	FAULT	$V_{(VDD - VEE)}$ Isolated Output1	$V_{(COM - VEE)}$ Isolated Output2	/PG Open Drain
V_{VIN} < UVLOp	X	X	OFF	OFF	HIGH
UVLOp < V_{VIN} < OVLOp	LOW	X	OFF	OFF	HIGH
UVLOp < V_{VIN} < OVLOp	HIGH	NO FAULT	Regulating at Setpoint	Regulating at Setpoint	LOW
UVLOp < V_{VIN} < OVLOp	HIGH	YES FAULT	OFF	OFF	HIGH
V_{VIN} > OVLOp	X	X	OFF	OFF	HIGH

ADVANCE INFORMATION

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCC14240-Q1 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

8.2 Typical Application

The following figures show the typical application schematics for the UCC14240-Q1 device configurations supplying an isolated load.

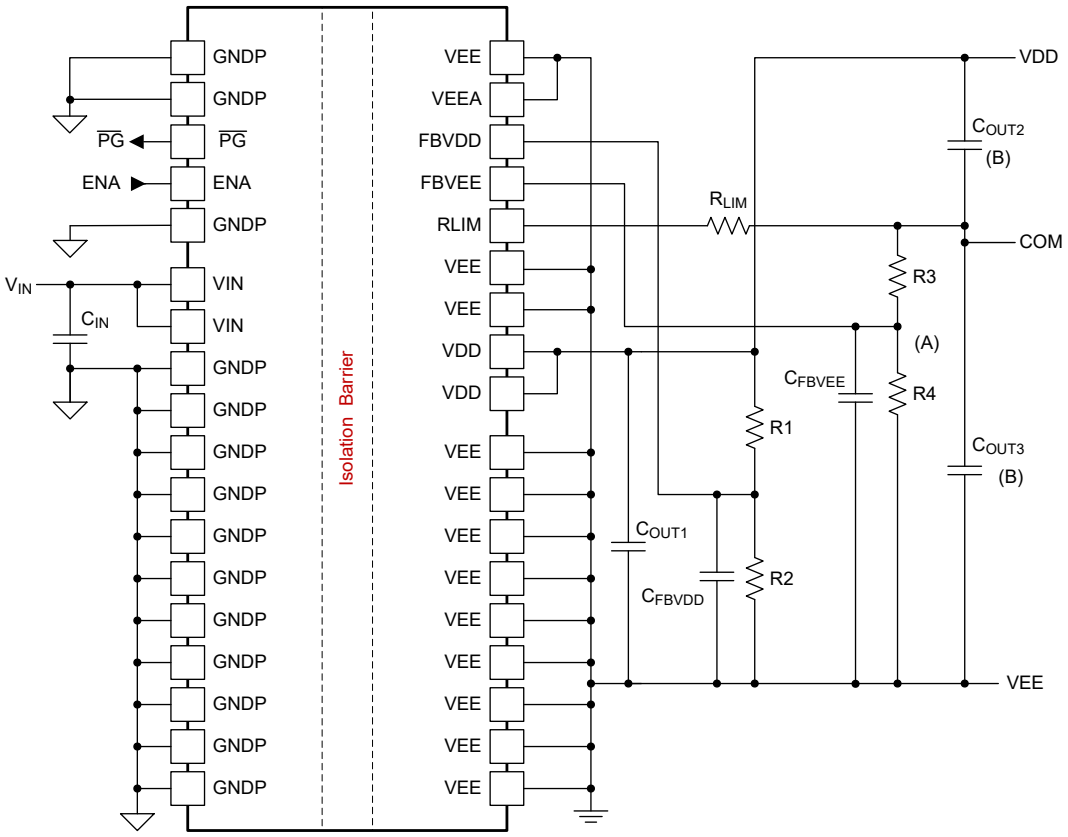


图 8-1. Dual Adjustable Output Configuration

ADVANCE INFORMATION

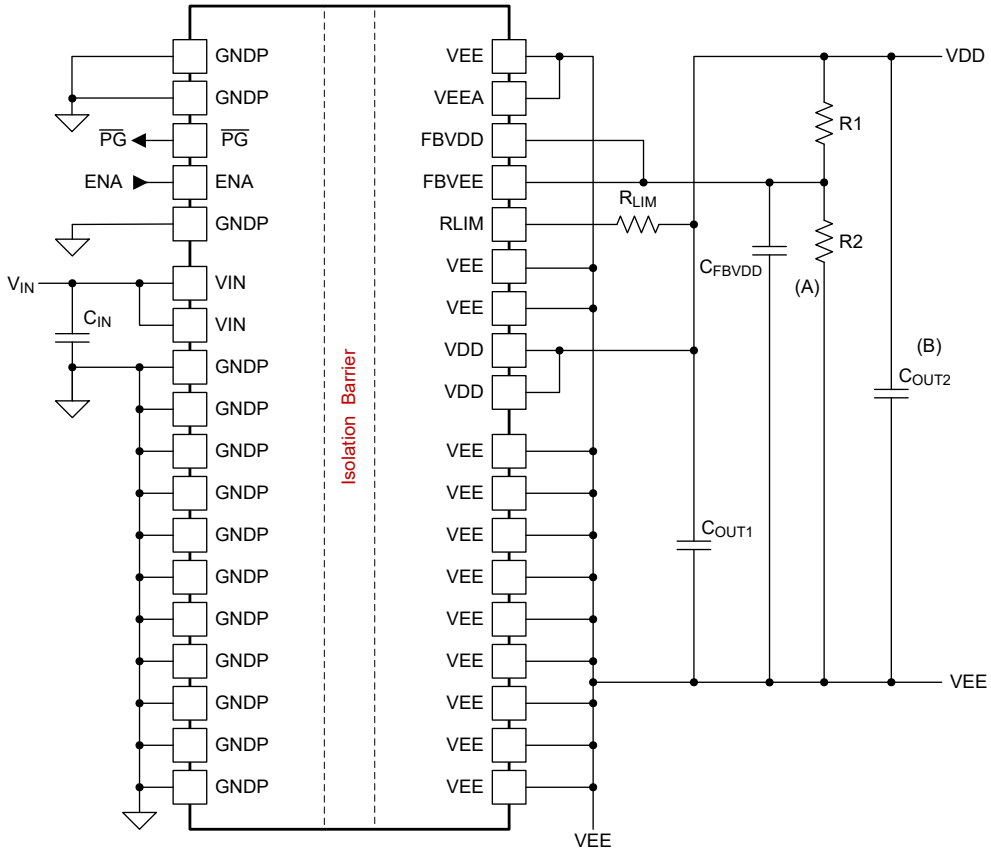


图 8-2. Single Adjustable Output Configuration

8.2.1 Design Requirements

Designing with the UCC14240-Q1 module is simple. First, choose single output or dual output. Determine the voltage for each output and then set the regulation through resistor dividers. The gate charge of the power device determines the amount of output decoupling capacitance needed at the gate driver input. Calculate the RLIM resistor value for regulating the (COM – VEE) voltage rail for a dual output. Finally, add the recommended input and output capacitors according to the procedure below.

8.2.2 Detailed Design Procedure

Place ceramic decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitors between pins 6 to 7 (VIN) and pins 8 to 9 (GNDP). For the isolated output supply, (VDD – VEE), place the capacitors between pins 28 to 29 (VDD) and pins 30 to 31 (VEE). For the isolated output supply, (COM – VEE), place an RLIM resistor between the RLIM pin and the gate driver COM supply input. Also place decoupling capacitors at the gate driver supply pins (COM and VEE) and at gate driver supply pins (VDD and VEE) with values according to the following component calculation sections. These locations are of particular importance to all the decoupling capacitors because the capacitors supply the transient current associated with the fast switching waveforms of the power drive circuits. Ensure the capacitor dielectric material is compatible with the target application temperature.

8.2.2.1 R_{LIM} Resistor Selection

The R_{LIM} resistor chosen can provide enough current for the load using the following equations, whichever has lower R_{LIM} value. 方程式 1 shows source current due to capacitor variation and IQ. 方程式 2 shows sink current due to capacitor variation and IQ.

$$R_{LIM\_MAX} = \frac{(VDD - COM)}{\left[\frac{C_{OUT3} \times (1 - \Delta C_{OUT3})}{C_{OUT2} \times (1 - \Delta C_{OUT2}) + C_{OUT3} \times (1 - \Delta C_{OUT3})} - \frac{C_{OUT3}}{C_{OUT2} + C_{OUT3}}\right] \times Q_{gtot} \times f_{SW} + \left(I_{Q\_DRIVER\_VEE} - I_{Q\_DRIVER\_VDD}\right)} - R_{LIM\_INT} \quad (1)$$

$$R_{LIM\_MAX} = \frac{(VEE - COM)}{\left[\frac{C_{OUT2} \times (1 - \Delta C_{OUT2})}{C_{OUT2} \times (1 - \Delta C_{OUT2}) + C_{OUT3} \times (1 - \Delta C_{OUT3})} - \frac{C_{OUT2}}{C_{OUT2} + C_{OUT3}}\right] \times Q_{gtot} \times f_{SW} + \left(I_{Q\_DRIVER\_VEE} - I_{Q\_DRIVER\_VDD}\right)} - R_{LIM\_INT} \quad (2)$$

where

- Q_{gtot} is the total gate charge of power switch.
- f_{SW} is the switching frequency of gate drive load.
- $I_{Q\_DRIVER\_VDD}$ is the maximum quiescent current of the gate driver from (VDD – COM), and any current pulled from VDD by external logic must be included.
- $I_{Q\_DRIVER\_VEE}$ is the maximum quiescent current of the gate driver from (COM – VEE), and any current pulled from VEE by external logic must be included.

R_{LIM} value determines response time of (COM – VEE) regulation. Too low an R_{LIM} value can cause oscillation and can overload (VDD – VEE). Too high an R_{LIM} value can give offset errors, due to slow response. If R_{LIM} is greater than above calculations, then there is not enough current available to replenish the charge to the output capacitors, causing a charge imbalance where the voltage is not able to maintain regulation, and eventually exceeds the OVP2 or UVP2 FAULT thresholds and shutting down the device for protection.

8.2.2.2 Capacitor Selection

表 8-1. Calculated Capacitor Values

CAPACITOR	VALUE (µF)	NOTES
C_{IN}	2.2	Place a 0.1- µ F high-frequency decoupling capacitor in parallel close to pins
C_{OUT1}	2.2	Add a 2.2- µ F and a 0.1- µ F capacitor for high-frequency decoupling of (VDD – VEE). Place close to pins.
C_{OUT2}	10	Required for bulk charge for gate drive, voltage divider, and balance
C_{OUT3}	40	

$$\frac{C_{OUT2}C_{OUT3}}{C_{OUT2}+C_{OUT3}} \geq \frac{Q_{gtot}}{V_{PP_{MAX}}} = \frac{4.4\mu C}{0.5V} = 8.8\mu F \quad (3)$$

$$C_{OUT3} = C_{OUT2}\frac{VDD - COM}{COM - VEE} \quad (4)$$

$$V_{PP_{MAX}} = Q_{gtot}\frac{C_{OUT2}+C_{OUT3}}{C_{OUT2}C_{OUT3}} = \frac{4.4\mu C}{8\mu F} = 0.55V \quad (5)$$

8.3 System Examples

The UCC14240-Q1 module is designed to allow a microcontroller host to enable it with the ENA pin for proper system sequencing. The /PG output also allows the host to monitor the status of the module. The /PG pin goes low when there are no faults and the output voltage is within ±10% of the set target output voltage. The output

ADVANCE INFORMATION

voltage is meant to power a gate driver for either IGBT or SiC FET power device. The host can start sending PWM control to the gate driver after the /PG pin goes low to ensure proper sequencing. Shown below is the system diagram for the dual-output configuration and a system diagram for the single output configuration.

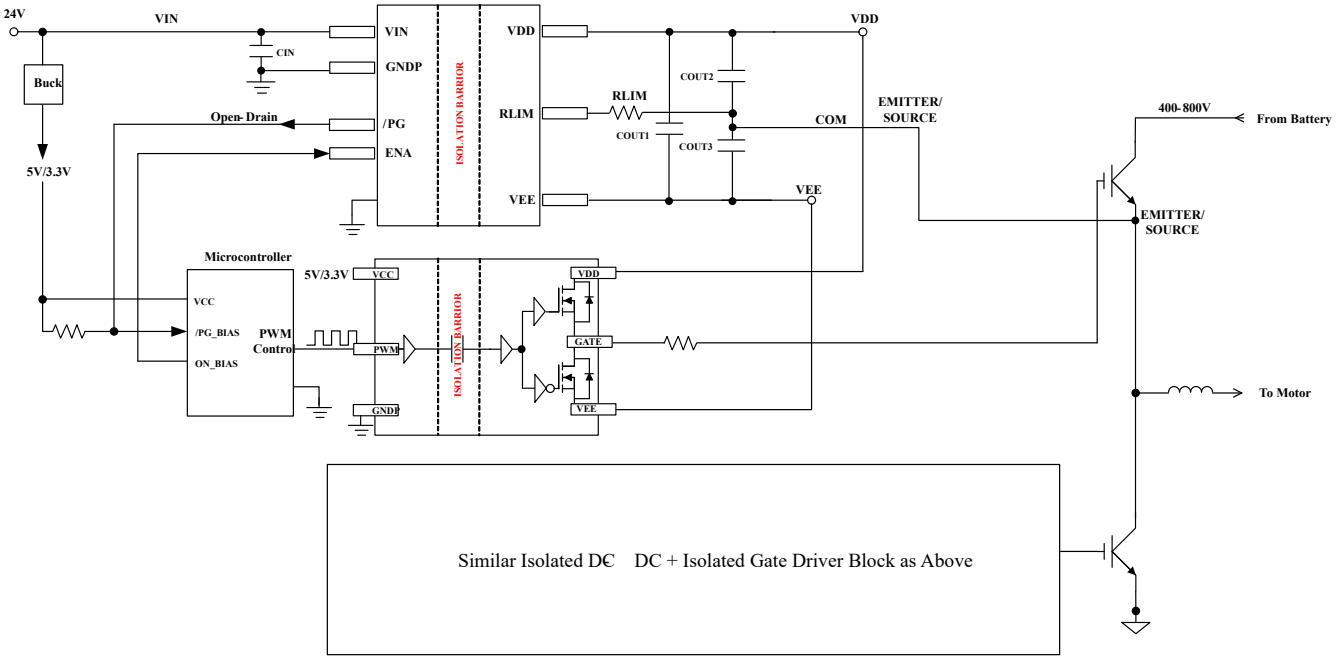


图 8-3. Dual Output System Configuration

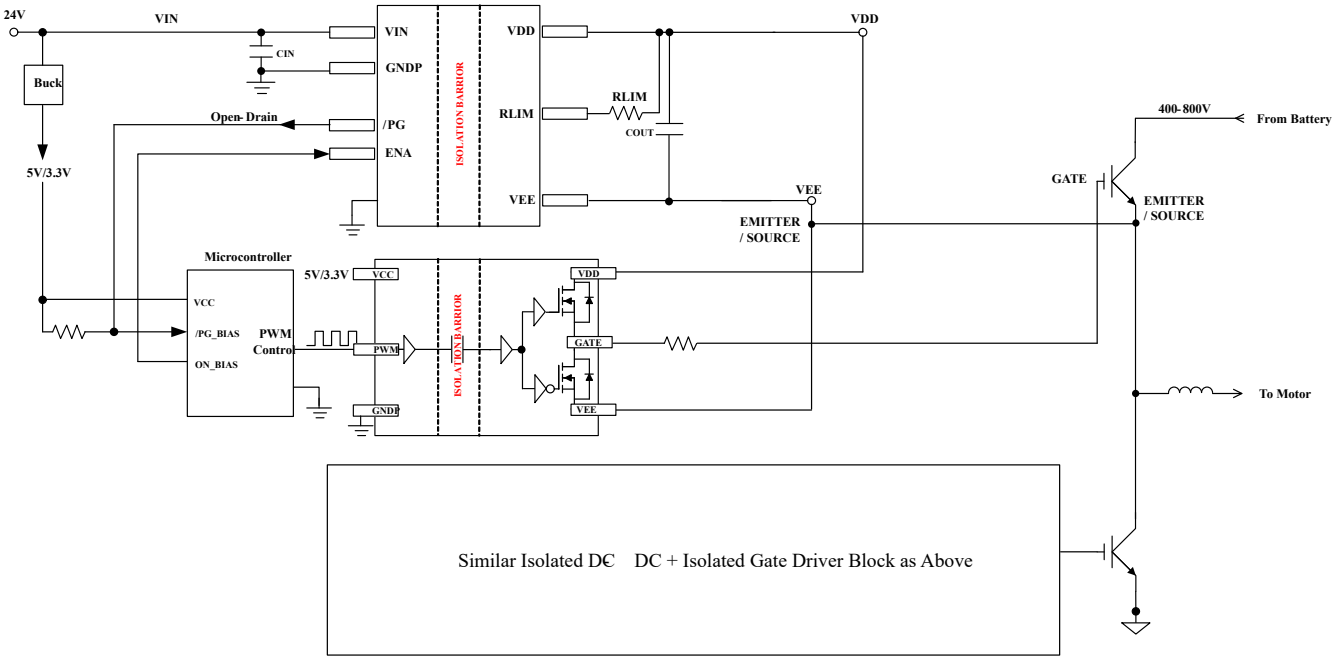


图 8-4. Single Output System Configuration

ADVANCE INFORMATION

9 Power Supply Recommendations

The recommended input supply voltage (VIN) for UCC14240-Q1 is between 21 V and 27 V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Local bypass capacitors must be placed between the VIN and GNDP pins at the input; between VDD and VEE at the isolated output supply; and COM and VEE at the lower voltage output supply. Low ESR, ceramic surface mount capacitors are recommended. TI further suggests placing two such capacitors: one with a value of 2.2 μF for supply bypassing and an additional 0.1-μF capacitor in parallel for high frequency filtering. The input supply must have an appropriate current rating to support output load required by the end application.

10 Layout

10.1 Layout Guidelines

The UCC14240-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimum performance.

- Place decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitors between pins 6, 7 (VIN) and pins 1, 2, 5, 8 – 18 (GNDP). For the isolated output supply, place the capacitors between pin 28, 29 (VDD) and pins 19 – 25, 30 – 31, 35 – 36 (VEE). This location is of particular importance to the input decoupling capacitor because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.
- Because the device does not have a thermal pad for heat-sinking, the device dissipates heat through the respective GND pins. Ensure that enough copper (preferably a connection to the ground plane) is present on GNDP and VEE pins for best heat-sinking.
- If space and layer count allow, TI recommends to connect the VIN, GNDP, VDD, and VEE pins to internal ground or power planes through multiple vias. Alternatively, make the traces that are connected to these pins as wide as possible to minimize losses.
- Minimize capacitive coupling between the RLIM pin and the FBVEE pin by separating the traces while routing, and if possible use a via near the FBVEE pin to route the feedback connection through a different layer.
- A minimum of four layers is recommended to accomplish a good thermal PCB design. Inner layers can be used to create a high-frequency bypass capacitor between GNDP and VEE, which in turn mitigates radiated emissions.
- Pay close attention to the spacing between primary ground plane (GNDP) and secondary ground plane (VEE) on the outer layers of the PCB. The effective creepage and or clearance of the system will be reduced if the two ground planes have a lower spacing than that of the UCC14240-Q1 package.
- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the UCC14240-Q1 module.

10.2 Layout Example

The layout example shown in the following figures is from the evaluation board UCC14240EVM-052 and based on the 图 8-1 design.

The component selection is as follows:

- C_{IN} = 0.1 µF (0603) + 2.2 µF (0805)
- C_{OUT1} = 0.1 µF (0603) + 2.2 µF (0805)
- C_{OUT2} = 0.1 µF (0603) + 2.2 µF (0805)
- C_{OUT3} = 0.1 µF (0603) + 3 × 3.3 µF (0805)
- R_{RLIM} = 1 kΩ (0805)

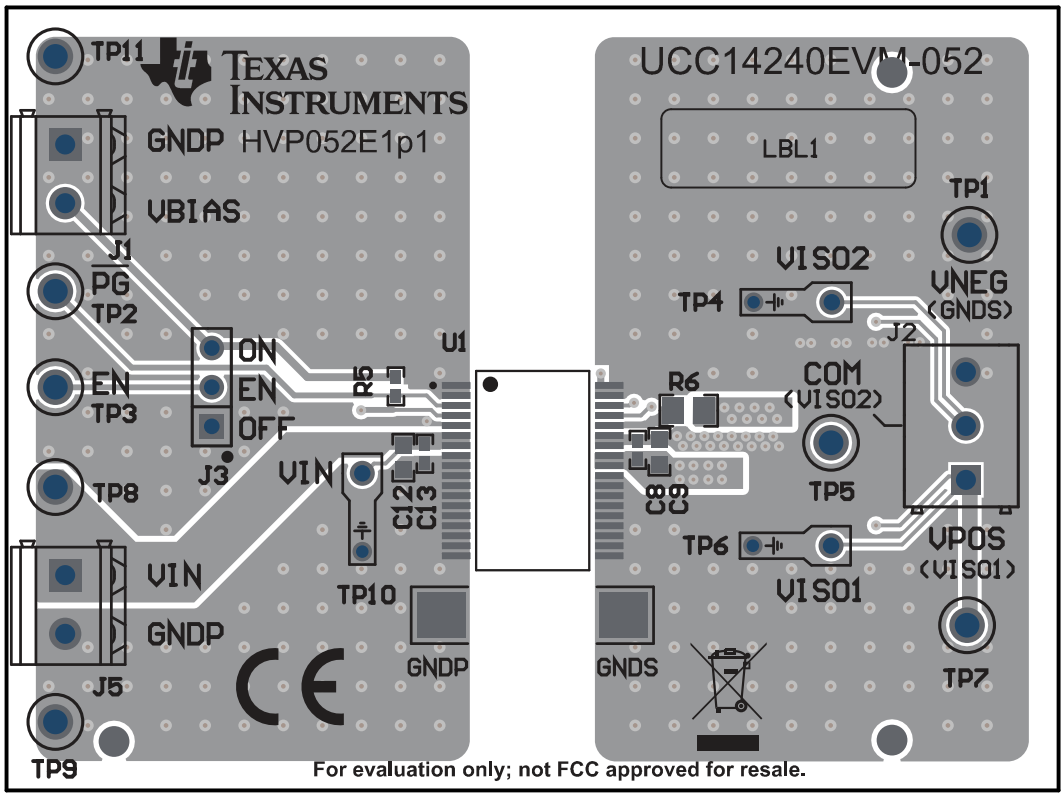


图 10-1. UCC14240EVM-052, PCB Top Layer, Assembly

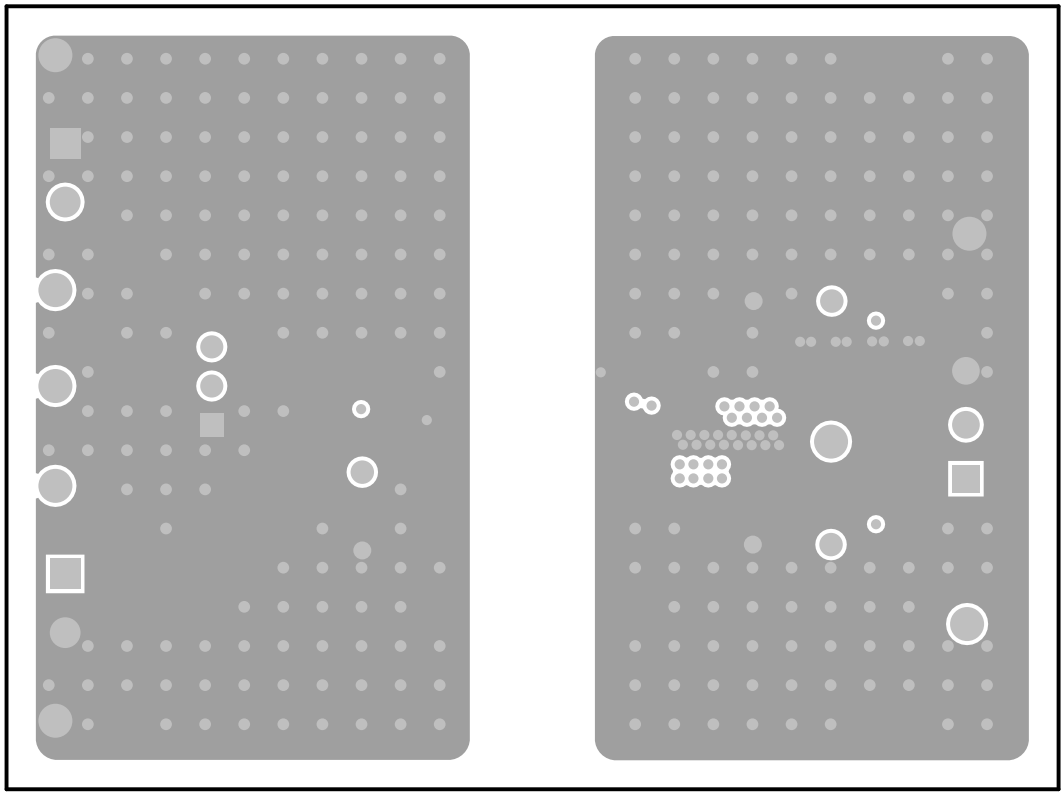


图 10-2. UCC14240EVM-052, Signal Layer 2 (Same as Layer 3)

ADVANCE INFORMATION

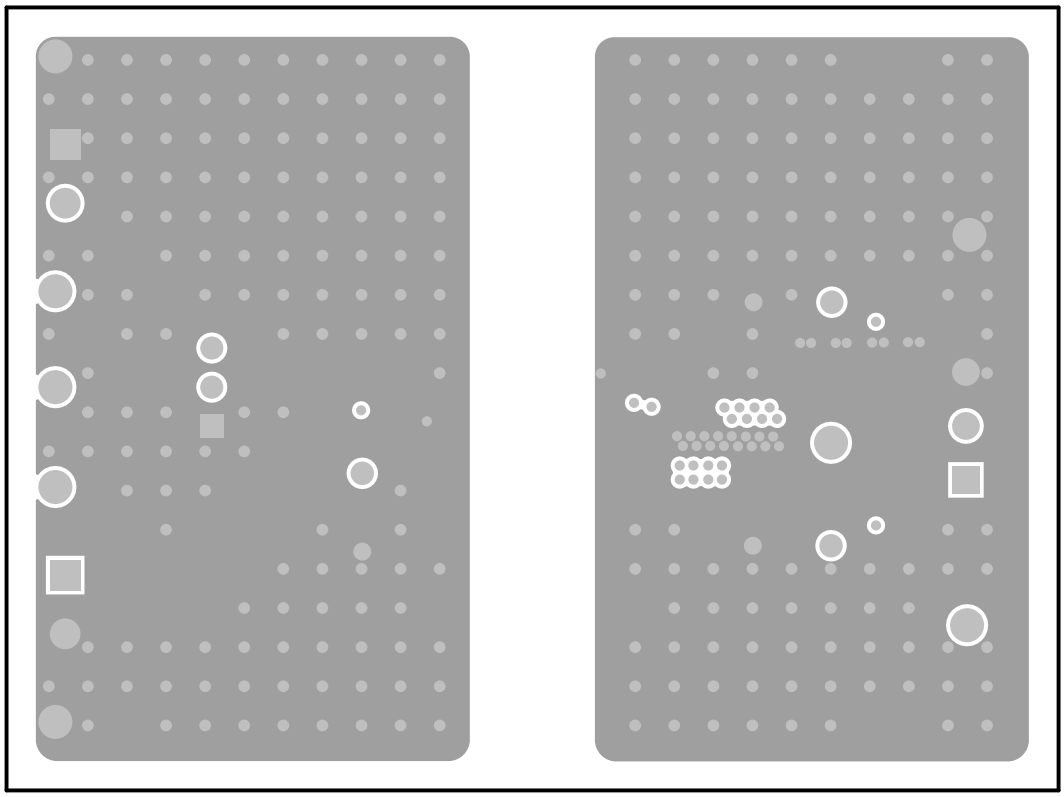


图 10-3. UCC14240EVM-052, Signal Layer 3 (Same as Layer 2)

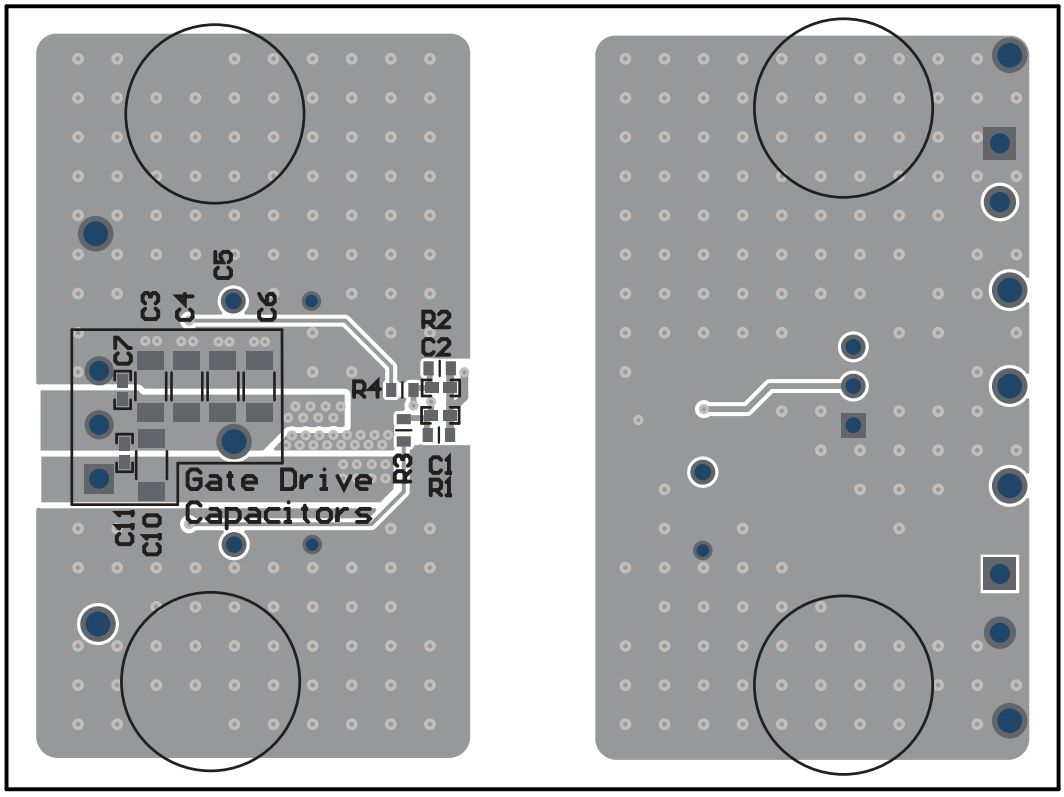


图 10-4. UCC14240EVM-052, PCB Bottom Layer, Assembly (Mirrored View)

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *User's Guide for Evaluation Module UCC14240EVM-052*
- *Isolation Glossary*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

ADVANCE INFORMATION

12 Mechanical, Packaging, and Orderable Information

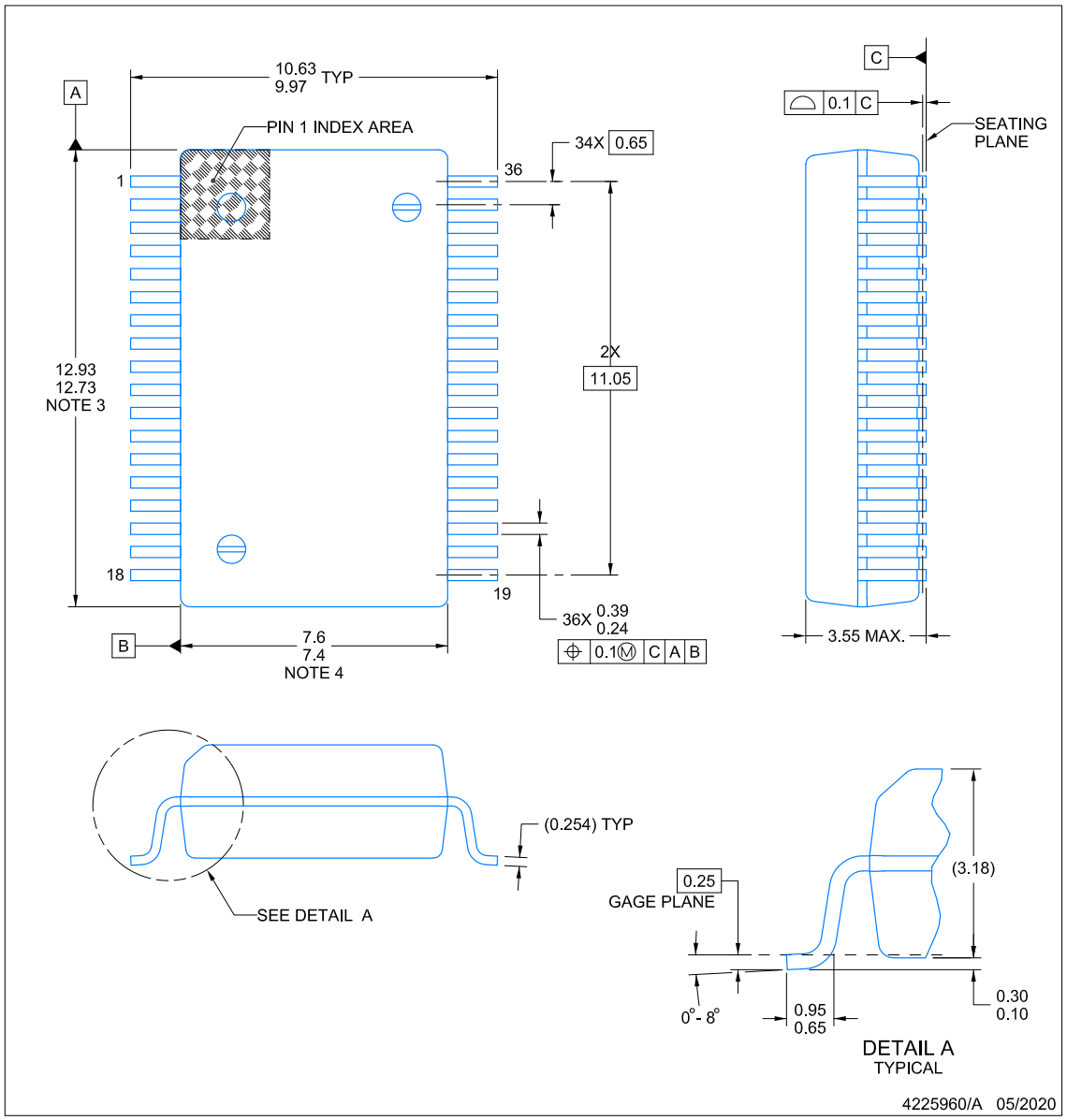
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DWN0036A

SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

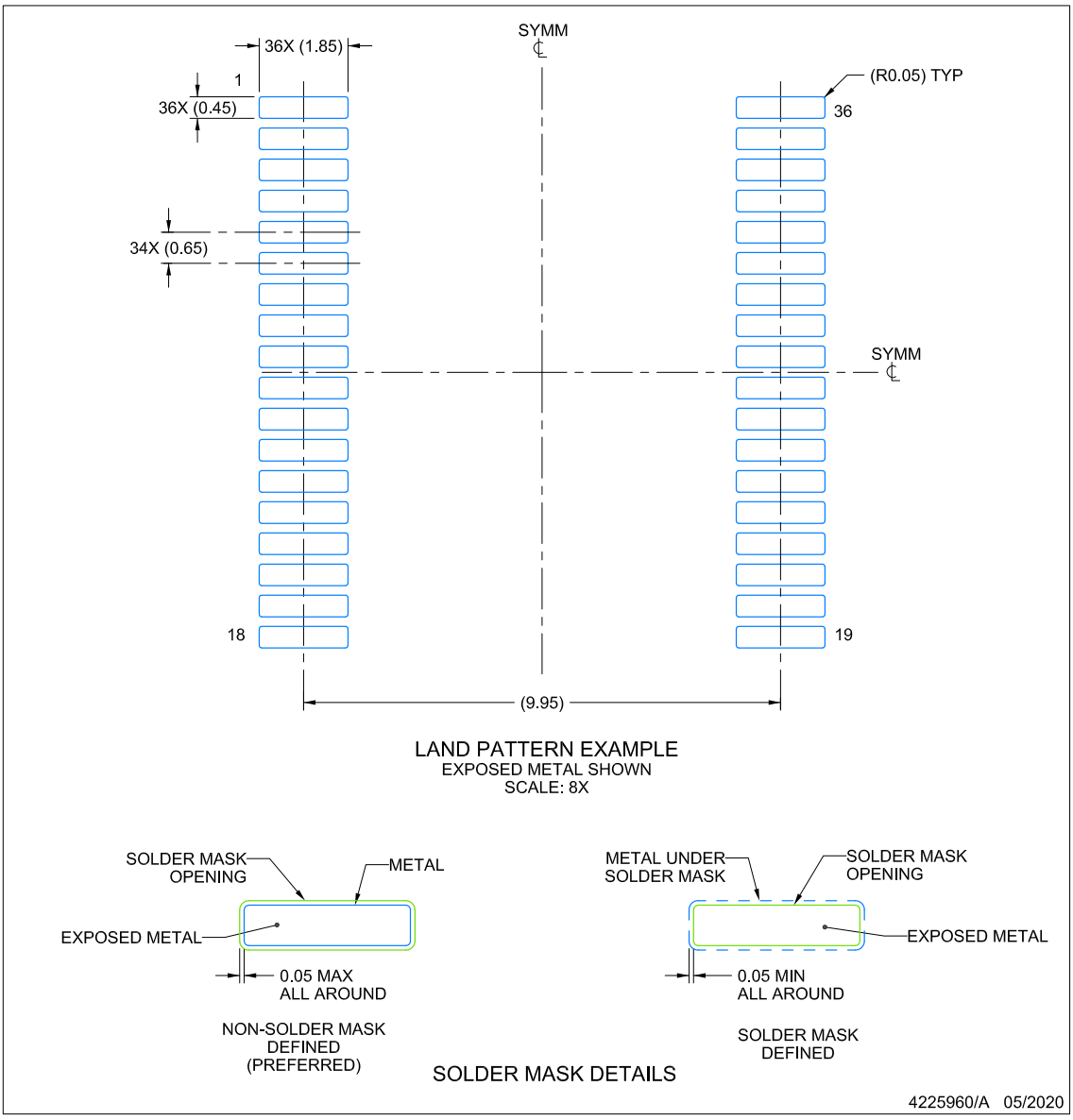
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

DWN0036A

SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE



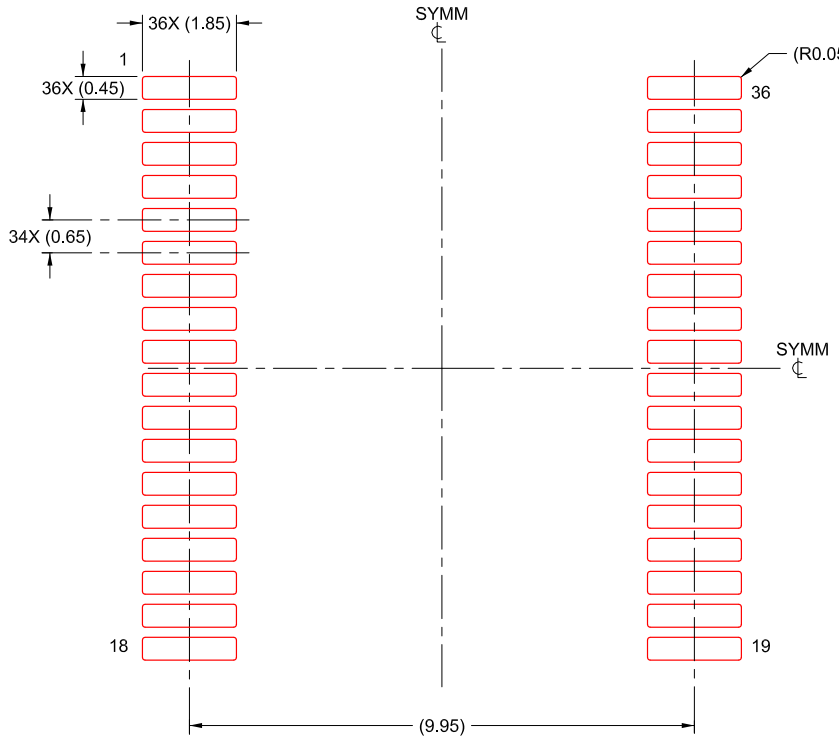
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DWN0036A — **SSOP - 3.55 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225960/A 05/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PUCC14240DWNQ1	ACTIVE	SO-MOD	DWN	36	25	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265